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A Novel Domino Logic Based on Floating-Gate MOS Transistors

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***Abstract*—** Domino logic finds a wide variety of applications in both static and dynamic random-access memories and in high-speed microprocessors. However, the main limitation of the domino logic-circuit family is the trade-off between the noise immunity and speed. In order to resolve such a trade-off, this paper proposes a domino logic that is based on floating-gate MOS (FGMOS) transistors. Compact-form expressions are derived for the noise margins for the low and high inputs as well as the propagation delays. The proposed scheme is verified by simulation adopting the 45 nm CMOS predictive technology model (PTM) with a power-supply voltage of 1 V. The obtained results unveil that the proposed domino logic outperforms the conventional domino logic in terms of the power-delay product and the energy-delay product when realizing wide fan-in OR gates. The realized, with the proposed scheme, 16-input OR gate has an average power consumption of 3.7 μW and a propagation delay of 51 ps.

***Keywords*—** Domino logic; Floating-gate MOS transistor; Noise margin; Time delay.

1. INTRODUCTION

CMOS technology is a widespread and mature technology that can find many applications in many analog and digital circuits [1, 2]. CMOS technology contains many logic-circuit families including static-complementary CMOS, dynamic CMOS, differential-cascode voltage switch logic, current-mode logic, pass-transistor logic, NMOS logic, and pseudo-NMOS logic [3, 4]. Compared to the static-complementary CMOS logic-circuit family, the dynamic logic has smaller area and higher speed especially for wide fan-in logic circuits [5, 6]. The dynamic logic can find applications in multiplexers, comparators [7], microprocessor circuits [8], and Schmitt triggers [9]. However, this logic-circuit family is sensitive to the leakage (especially the subthreshold-leakage current), the cross-talk, and the noise effects. The latter three effects become more detrimental with technology scaling [10, 11]. Also, its power consumption is relatively large due to the need to charge and discharge the dynamic-node capacitance [12]. In case of domino AND gates, the need arises to increase the size of the devices in the pull-down network (PDN) in order to obtain acceptable performance. The matter worsens with increasing the fan-in.

In this paper, a CMOS domino logic scheme is proposed that depends on using two floating-gate MOS (FGMOS) transistors; one of them acts as the keeper and the other one acts as a discharger. The latter transistor is connected in parallel with the PDN. A design

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procedure for the proposed domino logic is presented. The effects of the parameters of the FGMOS transistors on the time delay and noise immunity are investigated. Also, the effects of the fan-in, the fan-out, the power-supply voltage, the keeper size, and the PVT (process, voltage, and temperature) variations are investigated. As will be illustrated throughout the paper, unlike the conventional domino logic, the proposed FGMOS-based domino logic is suitable for application with both wide fan-in AND and OR gates with a moderate area.

The remainder of this paper is organized as follows: in Section 2, a brief review on the previous work on domino logic is given. In Section 3, the proposed FGMOS domino logic is presented. The quantitative analysis of the conventional and proposed domino logic is presented in Section 4. A design procedure for the proposed domino logic is presented in Section 5. The proposed domino logic is verified by simulation in Section 6. Finally, suitable conclusions are drawn and presented in Section 7.

2. LITERATURE REVIEW

In this section, a short literature review related to enhancing the performance of domino logic will be presented. Before delving into this survey, the operation of the standard domino logic is first discussed with the help of Figs. 1 and 2. Fig. 1 shows the circuit schematic of the standard domino logic while Fig. 2 shows the clock signal, *CLK*, as a function of time [13]. First, when the circuit is operating in the precharge phase, the *CLK* signal will be at logic "0." As a result, the header transistor, M_P, is activated while the footer transistor, M_N, is deactivated. So, the dynamic-node capacitance, C_L, is charged. Due to the deactivation of the footer transistor in this phase, the inputs have no effect on the status of the output. On the other hand, when the circuit is operating in the evaluation phase, the *CLK* signal will be at logic "1," thus both M_P and M_N will change their states. During the evaluation phase, the dynamic-node capacitance either discharges or remains charged depending on the status of the inputs. In case the status of the inputs is such that there is no discharging path existing through the PDN, the keeper will take the mission of keeping the dynamic-node capacitance charged at V_{DD}, thus compensating for the effects of the leakage current and charge sharing that inevitably occurs in the PDN. On the other hand, if the status of the inputs is such that a discharging path exists through the PDN, C_L will be discharged. However, the contention current of the PMOS keeper slows down the operation of the circuit during the discharging process. Thus, the keeper must be a weak one [13].

From the previous discussion, it is obvious that there is a trade-off between speed and noise immunity. Specifically, if the keeper size is increased to keep the dynamic node charged and enhance the noise immunity, its contention current increases and slows down the discharging process. The trade-off between speed and noise immunity in wide fan-in domino logic can be resolved by using a scheme of two main categories. The first category depends on rising the voltage at the source terminals of the PDN transistors [14] while the second type depends on properly controlling the strength of the keeper [15]. The first kind can be achieved by utilizing the stacking effect [16] or modifying the PDN [17]. On the other hand, the strength of the PMOS keeper can be controlled by appropriately changing its threshold voltage [18]. This can be achieved by double capacitive body biasing. By this scheme, both the leakage power can be reduced and the speed can be enhanced [19-21]. In [22, 23], the footer transistor is dispensed and a feedforward domino was adopted.

According to this technique, the speed is enhanced by a feedforward path; besides, the noise immunity is enhanced by adopting the self-reverse biasing [24]. In [25], a mirror version of the PDN is adopted in what is known as the "mirror technique" in order to enhance the noise immunity by raising the switching voltage of the upper PDN by virtue of the body effect.

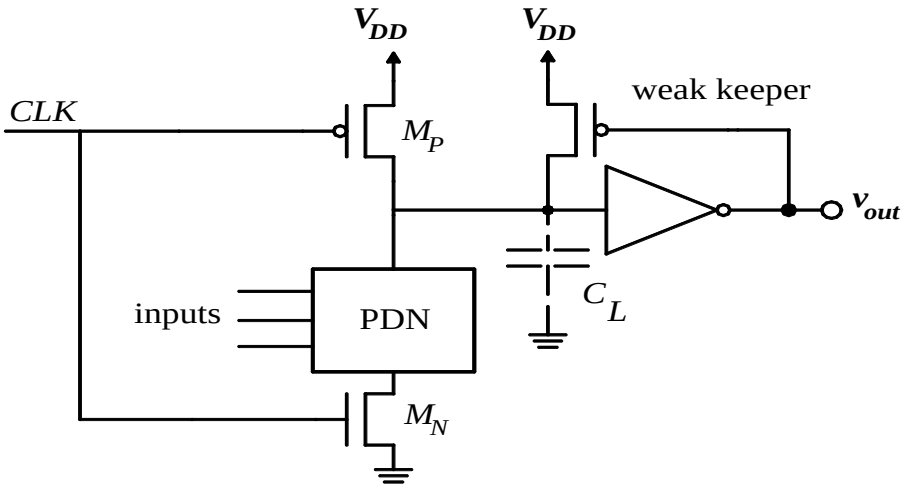

Fig. 1. Circuit schematic of the standard CMOS domino logic [13].

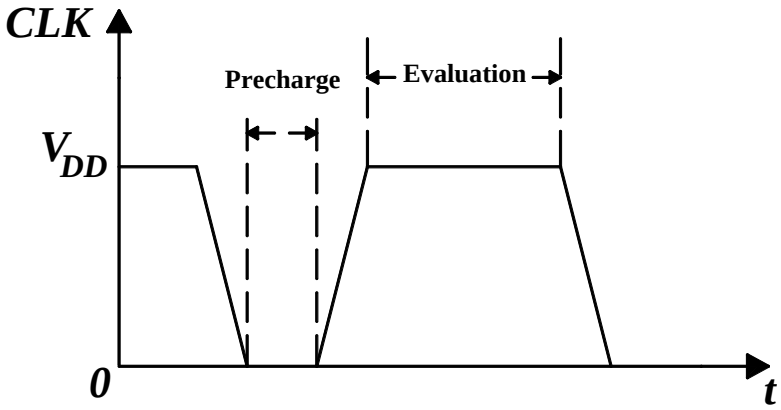

Fig. 2. The *CLK* signal as a function of time during the precharge and evaluation phases [13].

The dynamic power consumption can be reduced using a conditional keeper [26]. This reduction was achieved by both reducing the swing of the dynamic-node voltage and separating the dynamic node from the PDN by the virtue of an NMOS device; this results in reducing the parasitic capacitance. In [27], the dynamic-node voltage swing was controlled in wide fan-in gates. By this way, the power consumption was reduced without sacrificing speed, area, or noise immunity [28]. The dynamic-switching power consumption can also be reduced by reducing the swing at the output node, then restoring this swing to rail-to-rail with the aid of a sense amplifier [29, 30]. This technique seems attractive especially for heavy loads.

The performance of domino logic can be enhanced by isolating the dynamic-node parasitic capacitance and the PDN which results in a reduced contention current. Other improvements in keeper operations can be found in [19, 31-37]. The subthreshold-leakage current can be limited by serially connecting a diode-connected transistor to the PDN, thus utilizing the stack effect [38, 39]. According to this technique, the evaluation phase can be

sped-up also with the aid of a current mirror. The keeper's contention current can be reduced by both using a buffer to delay the keeper's operation and in turn limiting its current significantly and adopting a variation-coupled keeper [40]. The use of the variation-coupled keeper compensates for the leakage-current variation due to the PVT variations [41]. Also, the contention current can be reduced by serially connecting a diode-connected NMOS transistor with the PMOS keeper [42]. Using a current mirror can speed-up the operation during the evaluation phase by enlarging the discharging current of the dynamic-node capacitance [43].

In [44], a delay element along with the stack effect is utilized to reduce the contention current and enhance the noise immunity using FinFET devices. In [45], a comparison was performed between the largest leakage current and a mirrored version of the current of the PDN. As a result, the contention current of the keeper reduces, thus reducing the power consumption and the time delay. According to the scheme of [46], the output inverter was driven by the voltage difference between the lower and upper terminals of the PDN which causes the power consumption to reduce. In [47, 48], a dual keeper with clock control was adopted to reduce the delay variability. This was achieved by using a feedback circuitry with reduced loop gain. The clock-delayed dual-keeper technique was utilized in [49] to reduce the contention current.

In [50], a controlling network that consists of a PMOS device, a diode, and a delay element was added to control the keeper. According to this scheme, the power consumption and power-delay product are reduced by 31.42% and 31.91%, respectively, for 32-inputs OR gate. In [51], the keeper was modified by adding in series an NMOS device. As a result, the contention current is eliminated at the beginning of the evaluation phase, thus reducing the power consumption. Singhal et al. have proposed using a gated clock and revised keeper to reduce the power consumption in the circuit by adding a multiplexer for gating the clock signal [52].

In [53], negative-capacitance circuits have been developed to mitigate the effect of the PVT variations, thus reducing the delay variability. However, this comes at the expense of a power penalty. In [54], partial evaluation of the voltage in the computational block enhances the performance. Enhancing the power consumption and the noise immunity has been achieved in [55] by using voltage comparison in which the voltages of the upper and the lower nodes of the PDN were compared.

A comparator with a large bitwidth has been developed in [56] in which a parallel prefix structure was used. According to this design, local interconnection of a limited number of CMOS gates was used, thus avoiding unnecessary voltage transitions. In [57], a current-race circuit was used in which a current proportional to the number of the activated inputs was generated. This scheme has a better speed at the expense of a power penalty. In [58, 59], a dual keeper was adopted to reduce the delay variability. Finally, controlling the keeper current was achieved in [60] by using an odd number of inverters. Other schemes can be found in [61-65]. In the next section, the proposed domino logic is presented.

3. THE PROPOSED FGMOS-BASED DOMINO LOGIC

The proposed domino logic depends on using the floating-gate MOS (FGMOS) transistor. So, before presenting the proposed scheme, it is beneficial to give a short note

about the FGMOS transistor. The basic structure of an N-channel FGMOS transistor with n inputs is shown in Fig. 3(a) in which two types for the gate are shown; the floating gate and the control gates at which the inputs are applied. The adopted symbols for the N-channel and P-channel FGMOS devices are shown in Figs. 3(b) and (c), respectively [66]. The floating gate is surrounded by an oxide and is not physically connected to any external voltage. On the other hand, the control (also known as input) gates are connected to control voltages, v_1, v_2, …, and v_n [66]. So, the floating gate is capacitively coupled to the input voltages that are connected to the control gates. The equivalent circuit adopted for the FGMOS transistor is shown in Fig. 3(d) [67]. According to this equivalent circuit, the gate of the adopted NMOS transistor plays the role of the floating gate of the FGMOS transistor. C_i represents the input capacitance between the floating gate and the i^{th} input and C_G represents the capacitance between the floating gate and the substrate of the transistor which is connected to ground.

The control voltages determine the drain current by what are known as the input-capacitive coupling ratios [66]. It can be shown that the gate-to-source voltage, v_{GS}, of the FGMOS transistor in the saturation region is given by

$$v_{GS} = k_1(v_1 - v_S) + k_2(v_2 - v_S) + ... + k_n(v_n - v_S) \quad (1)$$

where k_i is the input-capacitive coupling ratio for the ith gate which is given by [66]

$$k_i = \frac{C_i}{\sum_{m=1}^{n} C_m + C_G} \quad (2)$$

For illustrating the proposed scheme, refer to Fig. 4. As shown in this figure, there are two modifications compared to the conventional domino logic. The first one is the replacement of the PMOS keeper by a P-channel FGMOS transistor, M_{PKP}, with its two control gates connected to the clock signal, *CLK*, and the output node. The second modification is the connection of an N-channel FGMOS transistor, M_{ND}, in parallel with the PDN with its two control gates also connected to the *CLK* signal and the output node.

The circuit operation proceeds as follows: During the precharge phase, the *CLK* signal is at 0 V, thus activating M_P and deactivating M_N with the result of charging C_L. The FGMOS keeper, M_{PKP}, turns on when the voltage at its floating gate becomes smaller than $V_{DD} - |V_{thp}|$, where V_{thp} is the threshold voltage of PMOS devices. By proper choice of the capacitive-coupling ratio associated with the keeper, M_{PKP} can be activated at a relatively early time compared to that of the activation of the conventional PMOS keeper, thus speeding-up the precharge phase.

During the evaluation phase, the *CLK* signal is at V_{DD}, thus acting to reduce the conductivity of M_{PKP} and increase the conductivity of M_{ND} waiting for the output voltage, v_{out}, to decide on the final voltage at the floating gate of each of these two devices. If the input-bit pattern is such that the PDN is activated, C_L will be discharged with a smaller contention current from the added FGMOS keeper compared to the conventional one and a larger discharging current due to the added FGMOS discharger. Thus, the speed-up according to the proposed scheme is twofold and the discharging time delay is certainly smaller than that of the conventional domino logic. The noise immunity, however, is not sacrificed as will be illustrated in Section 6.

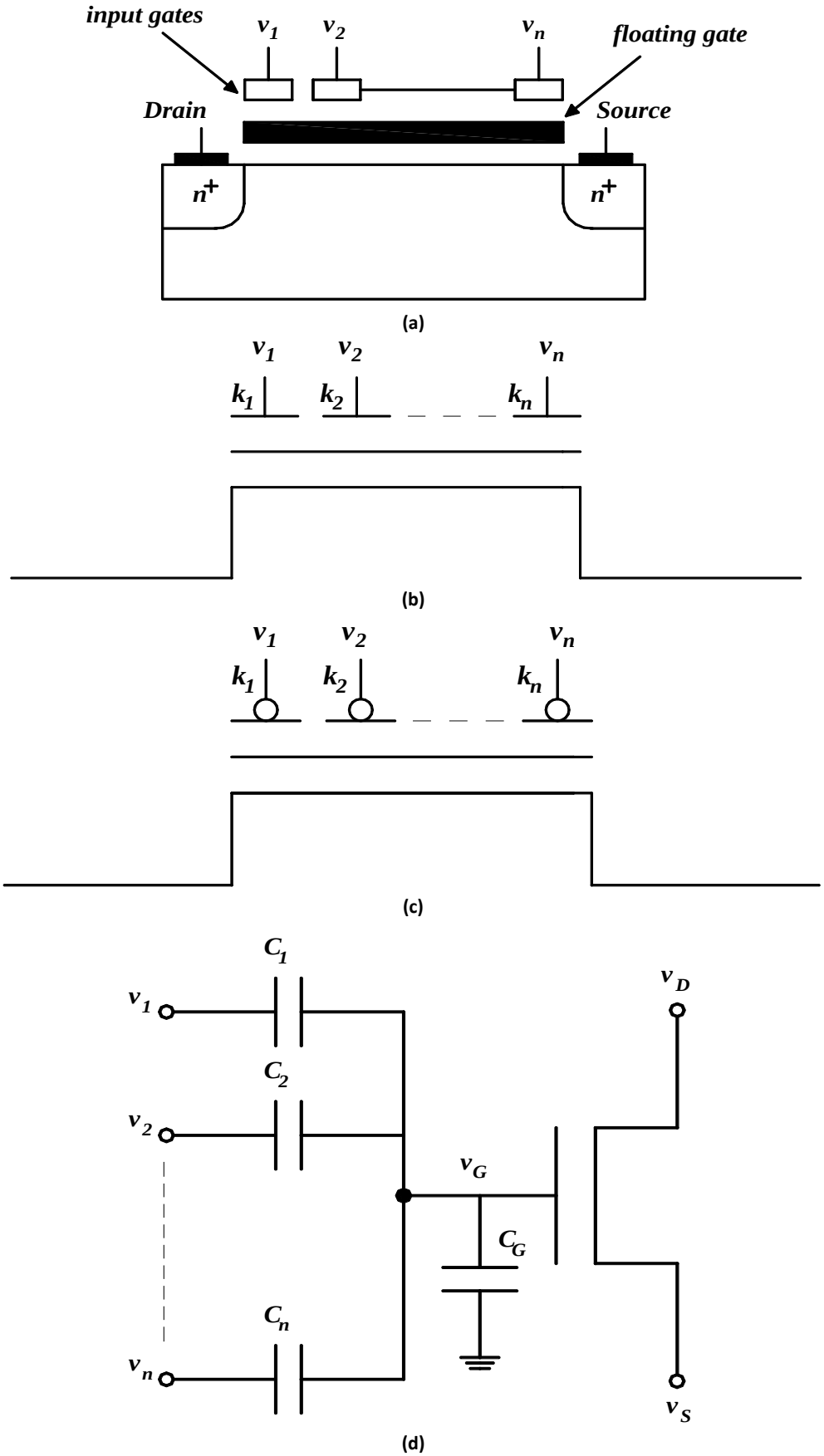

Fig. 3. a) Basic structure of an N-channel FGMOS transistor with the floating gate and the n–input control gates shown; b) the adopted symbol for the N-channel FGMOS transistor; c) the adopted symbol for the P-channel FGMOS transistor [66]; d) the adopted equivalent circuit of the FGMOS transistor [67] (v_D and v_S are the drain and source voltages, respectively).

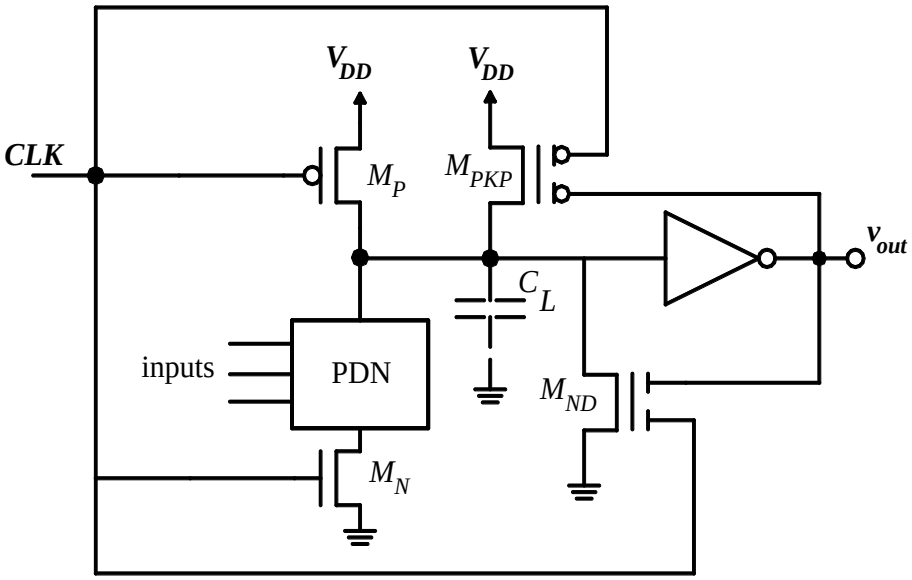

Fig. 4. Circuit schematic of the proposed domino logic (*K* and *D* in M_{PKP} and M_{ND} refer to keeper and discharger, respectively).

4. CIRCUIT DESIGN ISSUES

In this section, the proposed domino logic is investigated quantitatively and compared with the conventional domino logic. Specifically, compact-form expressions are derived for the noise margins for the low and high inputs and for the propagation delays. Due to its simplicity, the square–law MOSFET model is adopted in the derivation. The model of [68] is adopted here for the FGMOS transistors. Assume that the input-capacitive coupling ratios are defined as follows: k_1 is the input-capacitive coupling ratio associated with the *CLK* signal and the PMOS keeper, k_2 is the input-capacitive coupling ratio associated with the output node and the PMOS keeper, k_3 is the input-capacitive coupling ratio associated with the *CLK* signal and the NMOS discharger, and k_4 is the input-capacitive coupling ratio associated with the output signal and the NMOS discharger.

4.1. The Noise Margins

In this subsection, expressions of the critical points that determine the noise margins for the low and high inputs are derived. These critical points are the output-low voltage, V_{OL}, the output-high voltage, V_{OH}, the input-low voltage, V_{IL}, and the input-high voltage, V_{IH} [13]. The noise margins for the high and low inputs can thus be found from [13] as

$$NM_H = V_{OH} - V_{IH} \tag{3}$$

and

$$NM_L = V_{IL} - V_{OL}, \tag{4}$$

respectively. For the conventional domino logic, the values of V_{OL} and V_{OH} are 0 V and V_{DD}, respectively. Since the NMOS transistors of the PDN begin to conduct during the evaluation phase when v_{in} is equal to V_{thn}, V_{IL} can be taken equal to V_{thn}. Also, V_{IH} can be taken approximately equal to V_{IL} [13]. So, the noise margins for the low and high inputs are not equal.

This is in contrast to the proposed domino logic in which the noise margins for the low and high inputs can be equalized by proper choice of the input-capacitive coupling ratios and the aspect ratios as will be seen shortly. Toward finding V_{IL} and V_{IH} for the proposed domino logic, assume that the voltage across C_L is V_{C_L}. Also for simplifying the analysis, the PDN is represented by a single NMOS transistor and the series connection of this transistor and the footer is represented by a single NMOS transistor, M_{Neq}, with an aspect ratio that is given by

$$\left(\frac{W}{L}\right)_{neq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_{n}} + \frac{1}{\left(\frac{W}{L}\right)_{nF}}}, \tag{5}$$

where $(W/L)_n$, $(W/L)_{nF}$, and $(W/L)_{neq}$ represent the aspect ratios of the transistor equivalent to the PDN, the footer transistor, and the transistor equivalent to the PDN and the footer, M_{Neq}, respectively. For finding the expression of V_{IL}, note that when v_{in} is equal to V_{IL}, V_{C_L} is close to V_{DD}. So, M_{PKP} operates in the deep-triode region while both M_{Neq} and M_{ND} operate in the saturation region. Applying KCL at the dynamic node results in

$$\begin{aligned} &k_p'\left(\frac{W}{L}\right)_{pKP}\left(V_{DD}-k_1V_{DD}-|V_{thp}|\right)\left(V_{DD}-v_{C_L}\right) \\ &= k_n'\left(\frac{W}{L}\right)_{neq}\left(v_{in}-V_{thn}\right)^2\left(1+\lambda_n v_{C_L}\right)+k_n'\left(\frac{W}{L}\right)_{nD}\left(k_3V_{DD}-V_{thn}\right)^2\left(1+\lambda_n v_{C_L}\right) \end{aligned} \tag{6}$$

$(W/L)_{pKP}$, $(W/L)_{neq}$, $(W/L)_{nD}$, k_n', V_{thn}, and λ_n are the aspect ratio of M_{PKP}, the aspect ratio of M_{Neq}, the aspect ratio of M_{ND}, the process-transconductance parameter, the threshold voltage, and the channel-length modulation effect parameter of the NMOS devices, respectively. The corresponding parameters for the PMOS devices are represented by a subscript, p, instead of n. In writing Eq. (6), the term containing v_{SD} squared for the keeper transistor was neglected in the deep-triode region, where v_{SD} is the source-to-drain voltage. Differentiating Eq. (6) with respect to v_{in} results in

$$\begin{aligned} &k_p'\left(\frac{W}{L}\right)_{pKP}\left(V_{DD}-k_1V_{DD}-|V_{thp}|\right)\left(-\frac{dv_{C_L}}{dv_{in}}\right) \\ &= 2k_n'\left(\frac{W}{L}\right)_{neq}\left(v_{in}-V_{thn}\right)\left(1+\lambda_n v_{C_L}\right)+\lambda_n k_n'\left(\frac{W}{L}\right)_{neq}\left(v_{in}-V_{thn}\right)^2\frac{dv_{C_L}}{dv_{in}}+\lambda_n k_n'\left(\frac{W}{L}\right)_{nD}\left(k_3V_{DD}-V_{thn}\right)^2\frac{dv_{C_L}}{dv_{in}} \end{aligned} \tag{7}$$

Putting dvc_L/dv_{in} equal to -1, substituting v_{in} by V_{IL}, and approximating v_{C_L} by V_{DD} result in the following expression for V_{IL}

$$V_{IL} = \frac{-b-\sqrt{b^2-4ac}}{2a} \tag{8}$$

where a, b, and c are given by

$$a = \lambda_n k_n'\left(\frac{W}{L}\right)_{neq} \tag{9}$$

$$b = -2k_n'\left(\frac{W}{L}\right)_{neq}\left(1+\lambda_n V_{DD}\right) \tag{10}$$

and

$$c = k_p^{'}\left(\frac{W}{L}\right)_{pKP}\left(V_{DD} - k_1 V_{DD} - |V_{thp}|\right) + \lambda_n k_n^{'}\left(\frac{W}{L}\right)_{nD}\left(k_3 V_{DD} - V_{thn}\right)^2 \quad (11)$$

respectively. The expression of V_{IH} can be found in a similar manner. In this case, v_{C_L} will be close to 0 V, so both M_{ND} and M_{Neq} operate in the deep-triode region while M_{PKP} operates in the saturation region. Alternatively, assuming that the investigated inverter is symmetric with equal noise margins for low and high inputs, then V_{IH} can be written as

$$V_{IH} = V_{DD} - V_{IL} \quad (12)$$

Intuitively, increasing the aspect ratio of a certain device decreases its equivalent resistance. The dynamic-node voltage can be estimated in a voltage division between the upper equivalent resistance representing the PMOS keeper and the lower parallel combination of the equivalent resistance representing the NMOS discharger and that representing the PDN and the footer transistor. Also, increasing a certain input-capacitive coupling ratio weakens the strength of the associated P-channel FGMOS device and increases the strength of the associated N-channel FGMOS device. So, both V_{IL}, V_{IH}, and in turn the noise margins can be properly determined by suitably selecting the aspect ratios of the transistors and the input-capacitive coupling ratios with the aid of the equations derived above. Refer to Fig. 5 for the plots of the average noise margin of the proposed domino logic versus the various transistor sizes.

Finally, note that according to the performed analysis, the average noise margin of the proposed domino logic is approximately independent of both k_2 and k_4. This can be attributed to the fact that these two capacitive-coupling ratios are related to the inverter output. This output signal is certainly delayed by the propagation delay of the inverter, thus leading to weakening their effects on the strength of the two FGMOS devices.

4.2. The Propagation Delays

The discharging time delays of the dynamic-node capacitance are quantified in this subsection for the conventional and proposed domino logic with the 50% criterion adopted. Due to the transition of the devices between several regions of operation during the discharging process, the estimation of the propagation delays using the drain-current equations is in fact formidable. As an alternative way, the transistors are substituted by their equivalent resistances. The following expression is adopted for the equivalent resistance [13]:

$$R = \frac{1}{k_n^{'}\left(\frac{W}{L}\right)_n\left(v_{GS} - V_{thn}\right)} \quad (13)$$

where v_{GS} represents the gate-to-source voltage of the NMOS devices. Let R_{PKC} and R_{Neq} represent the equivalent resistances of the PMOS keeper according to the conventional scheme, M_{PKC}, and the transistor, M_{Neq}, respectively. Remember that M_{Neq} represents the equivalent transistor representing the transistors of the PDN and the footer transistor. The resulting circuit is an *RC* one and is shown in Fig. 6(a). This circuit is much simpler to analyze compared to the original one of Fig. 4. The other parasitic capacitances are much smaller than C_L and thus can be safely neglected.

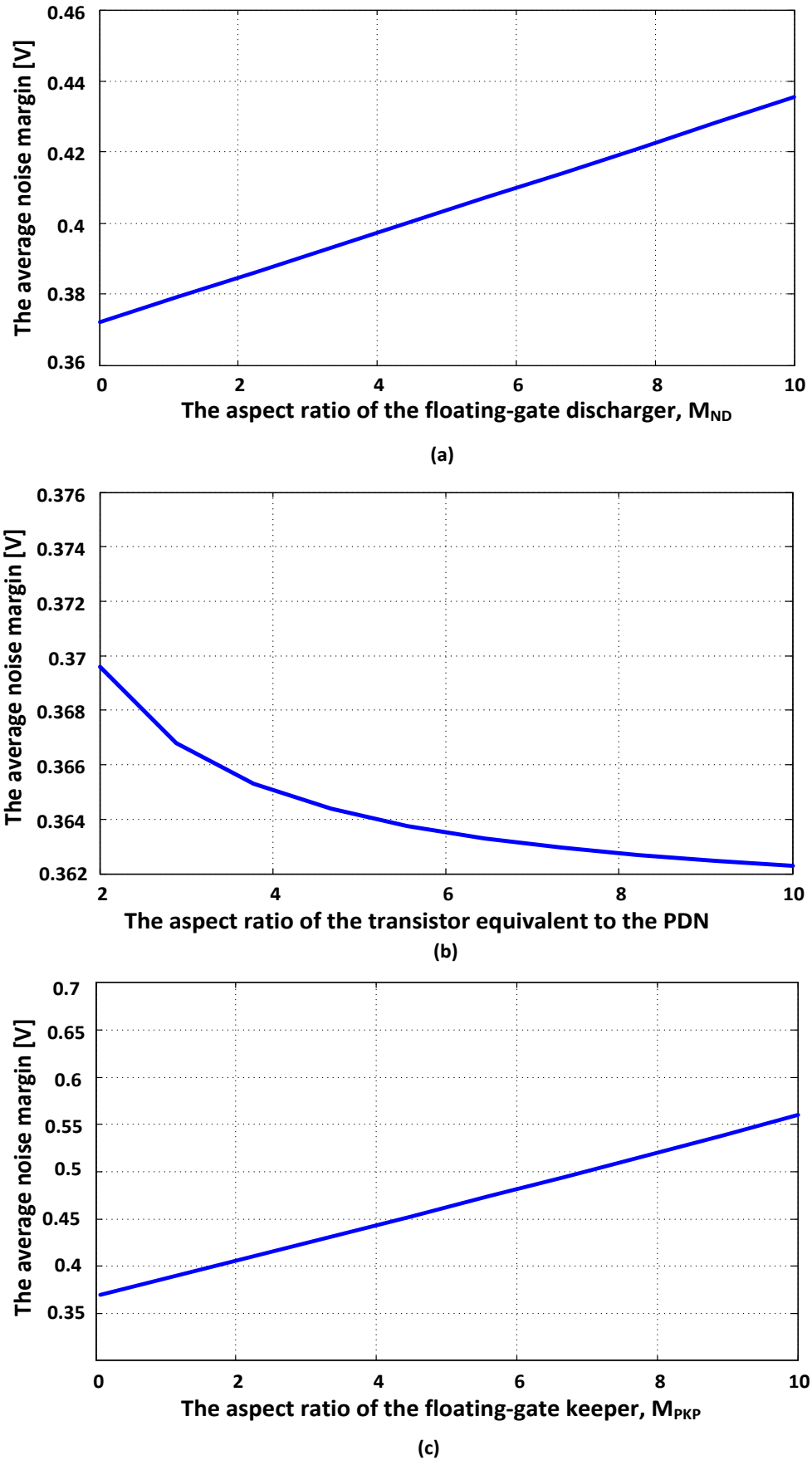

Fig. 5. Average noise margin of the proposed domino logic versus the: a) aspect ratio of the transistor, M_{ND}; b) aspect ratio of the transistor representing the PDN; c) aspect ratio of the keeper transistor.

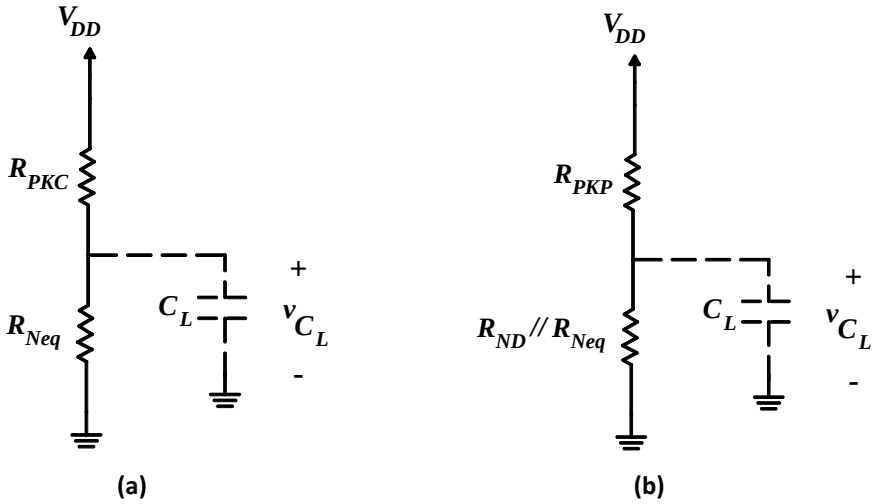

Fig. 6. Equivalent circuit of the: a) conventional; b) proposed domino logic (letters *N*, first *P*, second *P*, and *C* refer to NMOS, PMOS, proposed, and conventional, respectively).

For the conventional domino logic, during the time interval of interest v_{C_L} lies in the range between $V_{DD}/2$ and V_{DD} which is larger than the midpoint of the inverter. So, v_{out} is treated here as a constant and equal to 0 V. R_{PKC} is thus given by

$$R_{PKC} = \frac{1}{k_p'\left(\frac{W}{L}\right)_{pKC}\left(V_{DD} - |V_{thp}|\right)} \tag{14}$$

Similarly, R_{Neq} is given by

$$R_{Neq} = \frac{1}{k_n'\left(\frac{W}{L}\right)_{neq}\left(V_{DD} - V_{thn}\right)} \tag{15}$$

Now, applying KCL at the dynamic node of the equivalent circuit of Fig. 6(a), we get

$$-C_L\frac{dv_{C_L}}{dt} + \frac{V_{DD} - v_{C_L}}{R_{PKC}} = \frac{v_{C_L}}{R_{Neq}} \tag{16}$$

Taking into account that v_{C_L} is initially at V_{DD}, we get the solution of Eq. (16) as

$$v_{C_L}(t) = \frac{V_{DD}R_{Neq}}{R_{Neq} + R_{PKC}} + \frac{V_{DD}R_{PKC}}{R_{Neq} + R_{PKC}} e^{-\frac{t}{C_L}\left(\frac{1}{R_{PKC}} + \frac{1}{R_{Neq}}\right)} \tag{17}$$

The time delay according to the conventional scheme, t_c, is thus

$$t_c = \frac{C_L}{\left(\frac{1}{R_{PKC}} + \frac{1}{R_{Neq}}\right)} \ln\left[\frac{2R_{PKC}}{R_{PKC} - R_{Neq}}\right] \tag{18}$$

The equivalent *RC* circuit representing the proposed domino logic is shown in Fig. 6(b). R_{ND} represents the equivalent resistance of the FGMOS discharger and R_{PKP} represents the PMOS keeper according to the proposed scheme, M_{PKP}. The magnitudes of the gate-to-source voltages of M_{ND} and M_{PKP} are k_3V_{DD} and $V_{DD}(1 - k_1)$, respectively. The time delay according to the proposed scheme, t_p, is thus

$$t_p = \frac{C_L}{\left(\frac{1}{R_{PKP}} + \frac{1}{R_{Neq} // R_{ND}}\right)} \ln\left[\frac{2R_{PKP}}{R_{PKP} - \left(R_{Neq} // R_{ND}\right)}\right] \tag{19}$$

In order for M_{PKP} and M_{ND} to operate properly, the magnitudes of their gate-to-source voltages must be larger than the absolute value of their corresponding threshold voltages. Taking into account that v_{out} = 0 V in the time interval of interest, we get the maximum value of k_1 and minimum value of k_3 as

$$k_{1\max} = 1 - \frac{\left|V_{thp}\right|}{V_{DD}} \tag{20}$$

and

$$k_{3\min} = \frac{V_{thn}}{V_{DD}} \tag{21}$$

respectively. It must be noted that more accurate expressions can be adopted for the equivalent resistances such as [69]

$$R = \frac{v_{DS}}{k_n'\left(\frac{W}{L}\right)_n \left(v_{GS} - V_{thn}\right)^{\alpha}} + \frac{v_{DS}}{k_n'\left(\frac{W}{L}\right)_n \left[\left(v_{GS} - V_{thn}\right)v_{DS} - \frac{1}{2}v_{DS}^2\right]} \tag{22}$$

where α is a parameter that equals 2 for long-channel MOSFETs (with channel lengths larger than 10 μm) while its value is taken approximately equal to 1.3 for short-channel devices to account for the short-channel effects. Eq. (22) was based on the assumption that both v_{GS} and v_{DS} are equal to V_{DD} in order to combine the effects of both the triode and the saturation regions [69]. In the following graphs, both v_{GS} and v_{DS} are substituted by their average values during the region of interest. If the propagation delay is evaluated at the output node, the low-to-high propagation delay of the output inverter must be added.

Finally, refer to Fig. 7 for the plots of the discharging time delay of the proposed domino logic versus the various transistor sizes. Certainly, strengthening M_{ND} or the transistors of the PDN reduces the time delay. The opposite is true when strengthening the keeper due to increasing the keeper contention current. Also, the discharging time delay can be controlled with the proper choice of the input-capacitive coupling ratios except k_2 and k_4. k_2 and k_4 affect the discharging time delay slightly for the same reason discussed earlier.

5. DESIGN PROCEDURE

The compact-form expressions derived earlier provide the designer with first-order estimations for the desired performance metrics such as the noise margins and the propagation delays. More accurate values can of course be found from simulation. However, the most important benefit that can be obtained from the previous quantitative analysis is the trend of the change of the performance metrics with the design parameters such as the aspect ratios of the transistors including the FGMOS discharger and keeper as well as the four input-capacitive coupling ratios; the latter determine the amount of control of each of the control-gate voltages on the strength of the FGMOS devices. This trend helps the designer to decide either to increase or decrease a certain design parameter in order to optimize the performance.

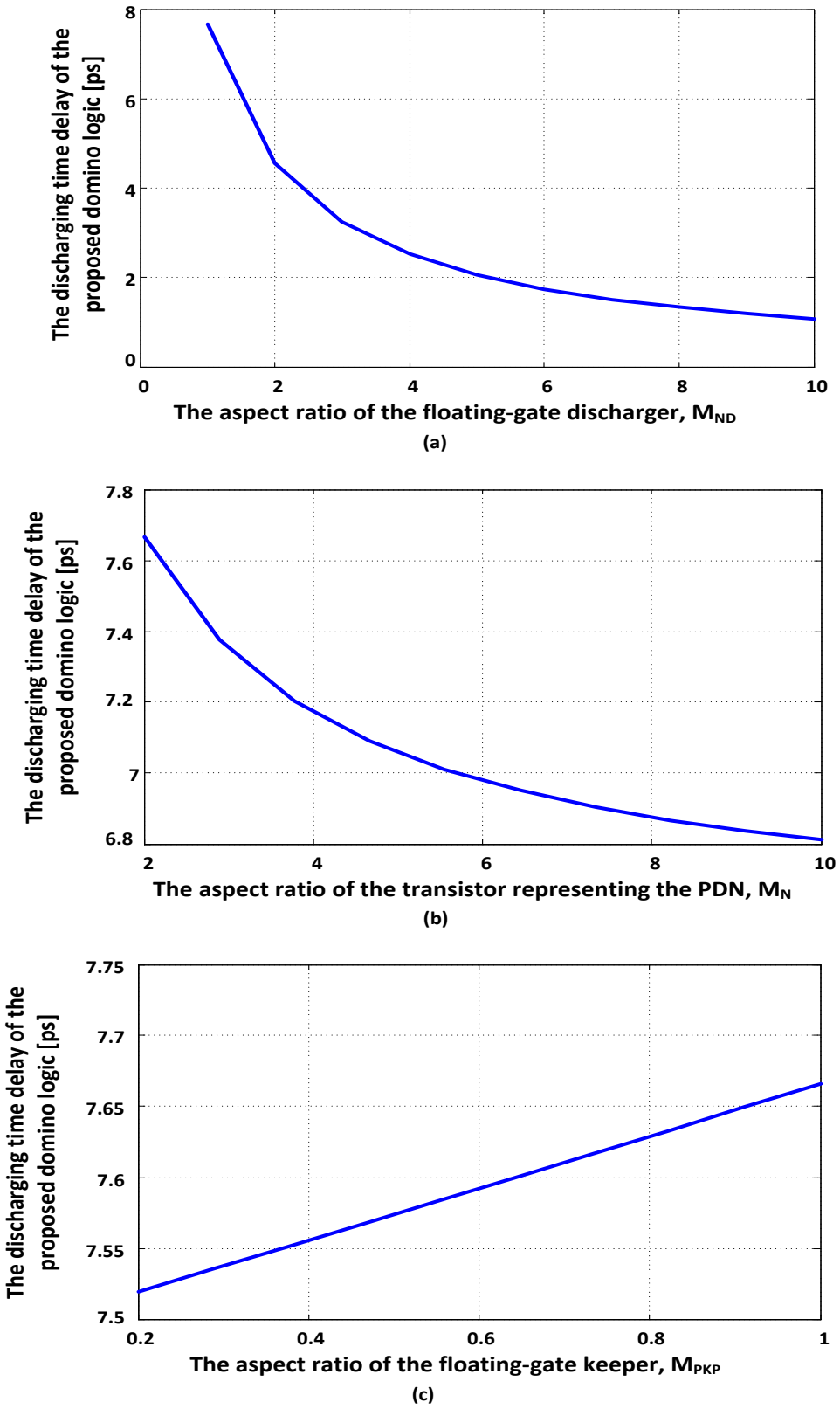

Fig. 7. Propagation delay of the proposed domino logic versus the: a) aspect ratio of the transistor, M_{ND}; b) aspect ratio of the transistor representing the PDN; c) aspect ratio of the keeper transistor.

The choice of the previous design parameters can proceed as follows:

1. Taking into account the type of connections of the transistors in the PDN, replace the PDN with a single NMOS device with an appropriate aspect ratio. The term

"appropriate" means that the equivalent resistance of the PDN is as close as possible to that of the equivalent device such that the time delay evaluated by simulation for the PDN is as close as possible to that evaluated for the equivalent device.

2. Choose the aspect ratio of the footer transistor to be the minimum acceptable value taking into account the effect of the process variations. According to Pelgrom's law, the mismatch of the threshold voltage between two adjacent identically drawn transistors is inversely proportional to the gate area [70, 71]. This is an obvious trade-off between the area overhead and the robustness of the designed circuit.
3. Unless otherwise required by the PDN, choose the keeper to have the minimum aspect ratio. Specifically, if the PDN contains a large number of parallelly connected devices and charge sharing plays an important role in its performance, the keeper size should be increased.
4. Decide on the optimum values of the input capacitive-coupling ratios associated with the two FGMOS devices by choosing appropriate values for the associated capacitances such that the propagation delay is at its minimum.
5. If there is a trade-off between the propagation delay and the average power consumption, the power-delay product or the energy-delay product may play as the deciding factor.
6. If the area limitation is not violated, the size of all the devices can be increased with a priority given to the device that is affecting the propagation delay more significantly.

6. RESULTS AND DISCUSSIONS

6.1. Simulation Setup

In this section, the proposed FGMOS-based domino logic is verified by simulation using the 45 nm CMOS predictive technology model with V_{DD} equal to 1 V [72]. Unless otherwise specified, the following parameters are adopted: The number of the inputs is equal to eight, the aspect ratios of all the devices are taken equal to two, and the fan-out capacitance according to each of the conventional and proposed domino logic is taken equal to 5 fF to mimic a heavy load. The dynamic-node capacitance, C_L, includes the wiring capacitance and the internal capacitances of the associated transistors of the PDN, the FGMOS discharger, the header, the keeper, and the output inverter. The wiring capacitance associated with each device is taken equal to 0.02 fF. The equivalent circuit of [68] is adopted here for the FGMOS transistor. The floating-gate capacitance as well as the control-gate capacitances associated with both the FGMOS transistors are taken equal to 0.1 fF. Both the rise and the fall times of the clock signal are taken equal to 50 ps. An 8-input OR gate is adopted and the simulation is performed at 27 ^{o}C.

In the following discussion, the effects of changing the input-capacitive coupling ratios on the noise margin and the time delay are investigated. The proposed domino logic is also compared with the conventional domino logic. The simulation is performed for AND (series connection of NMOS devices in the PDN) and OR (parallel connection of NMOS devices in the PDN) gates. Also, the effects of the load capacitance, the power-supply voltage, the fan-in, and the keeper size on the performance of the proposed domino logic are investigated. Finally, the effects of the PVT variations are investigated.

6.2. Effect of the Input-Capacitive Coupling Ratios on the Noise Margin

There are several performance metrics for estimating the noise immunity. The average noise margin, *NM*, is adopted here. For estimating the average noise margin, the voltage-transfer characteristics (VTC) between the input voltage and the dynamic-node voltage at steady state are plotted as in Fig. 8 for the conventional domino logic. For the conventional domino logic with parallelly connected devices in the PDN, we get the following values: V_{OL} = 0 V, V_{OH} = V_{DD}, V_{IL} = 0.65 V, and V_{IH} = 0.67 V for the case of one activated input and V_{OL} = 0 V, V_{OH} = V_{DD}, V_{IL} = 0.43 V, and V_{IH} = 0.45 V for the case of all activated inputs. If the noise margins for low and high inputs, NM_L and NM_H, are taken as the average of these two cases, we get NM_L = 0.54 V and NM_H = 0.44 V. For the case of the PDN with series connection, we get the following values: V_{OL} = 0 V, V_{OH} = V_{DD}, V_{IL} = 0.89 V, and V_{IH} = 0.91 V which correspond to NM_L = 0.89 V and NM_H = 0.09 V; a very poor noise margin for high input. Also, the two noise margins are far from equal in spite of the fact that the aspect ratios of the NMOS devices in the PDN are set equal to six. This implies that in order to obtain equal noise margins for the conventional domino logic in case of serially connected devices in the PDN, the area wasting is expected to be very large.

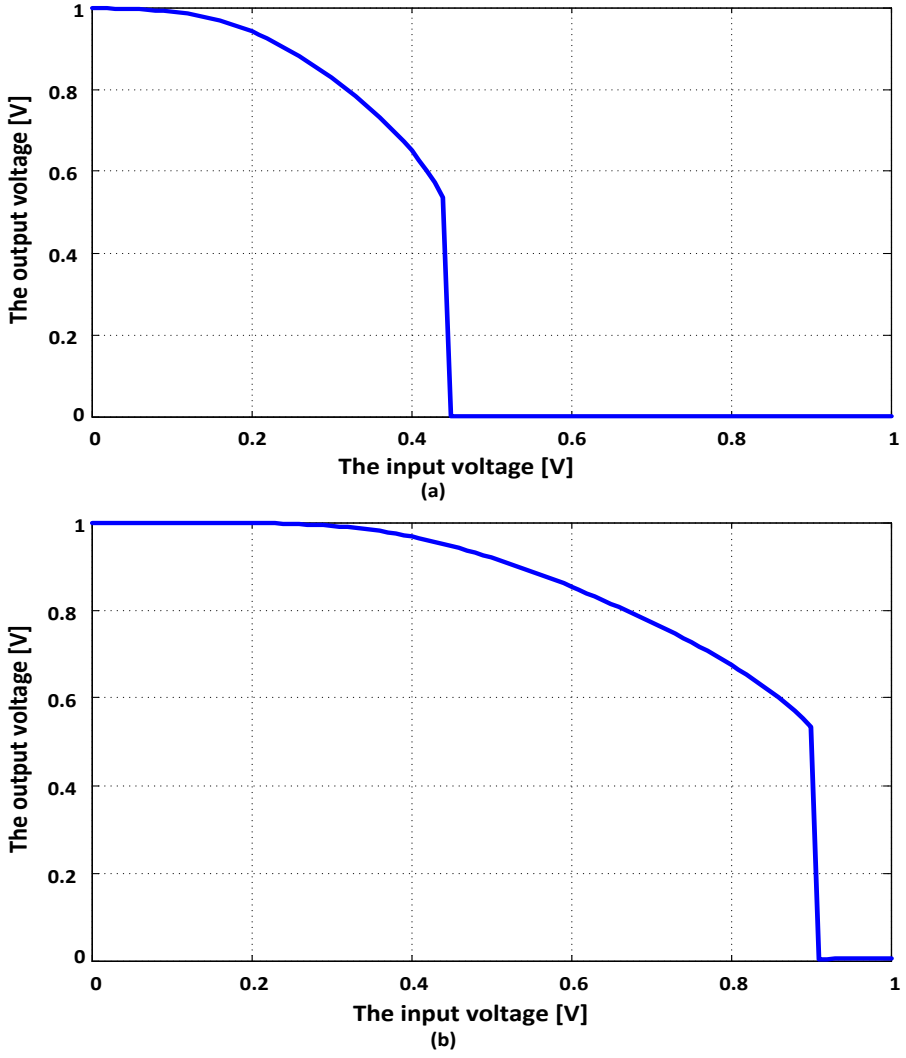

Fig. 8. Voltage-transfer characteristics of the conventional domino logic for the case of: a) parallelly connected devices with eight activated inputs; b) serially connected devices in the PDN.

For the proposed scheme, on the other hand, it is beneficial to decrease k_3 in order to increase the average noise margin as shown in Fig. 9 for the two cases of one and all activated inputs in case of parallelly connected devices. This is an expected result as reducing k_3 weakens the ability of the clock signal to discharge C_L during the evaluation phase. On the other hand, the output voltage will have an increased relative strength in controlling M_{ND} and in turn on the discharge of C_L and increasing the noise margin. There are two main advantages of the proposed domino logic; the first one is that the noise margins for both low and high inputs can be tailored by choosing appropriate values for the input-capacitive coupling ratios. They can also be equalized. The second advantage appears in case of the series connection for the PDN devices in which the aspect ratios of the PDN devices are equal to two. This aspect ratio must be compared with six for the conventional domino logic, thus there will be a significant saving in area. The effects of the other coupling ratios can be investigated similarly.

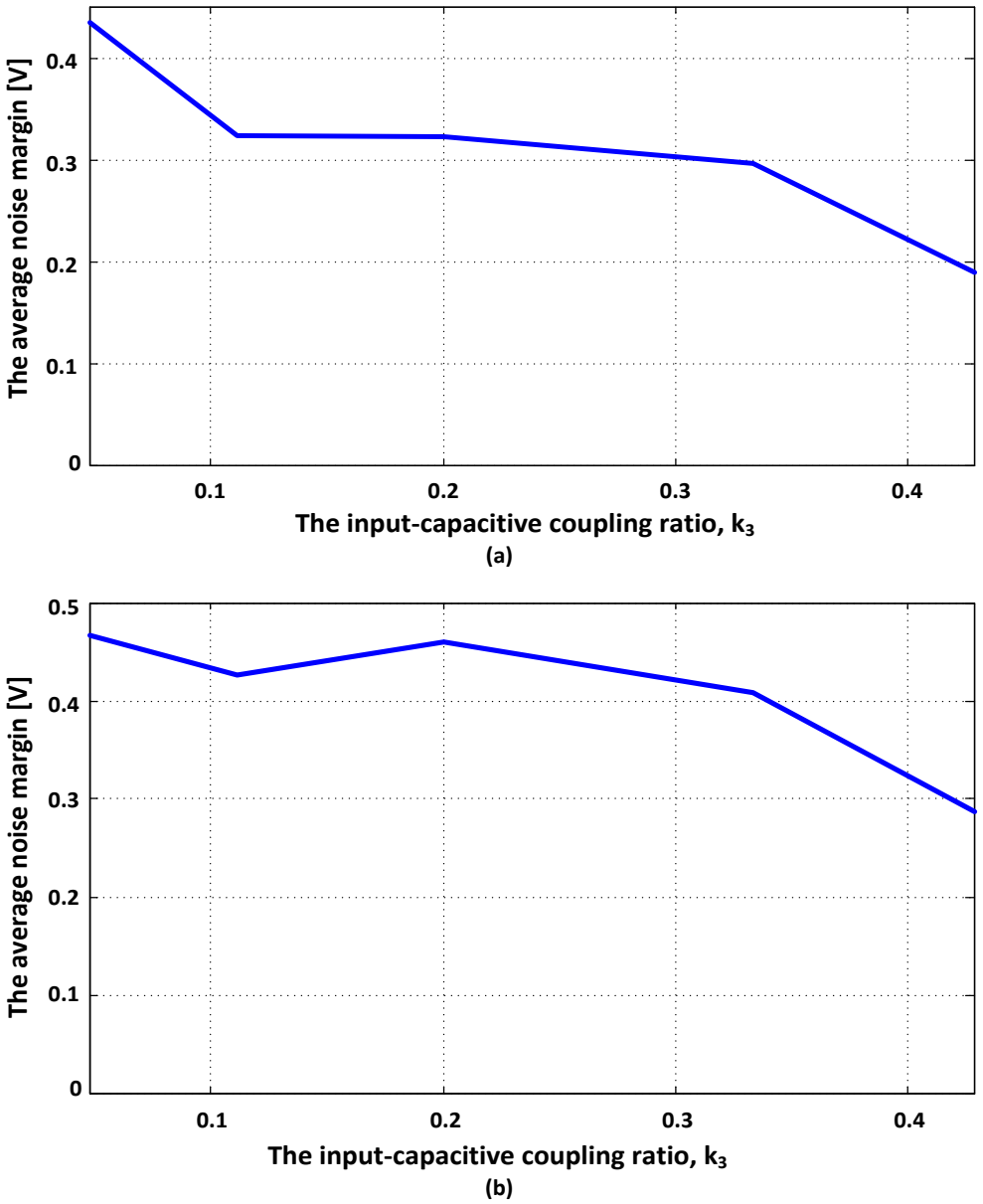

Fig. 9. Relationship between the input-capacitive coupling ratio, k_3, and the average noise margin for: a) one activated input; b) all activated inputs in case of parallelly connected devices.

6.3. Effect of the Input-Capacitive Coupling Ratios on the Time Delay

The 50% criterion is adopted for evaluating the time delay. For the OR gate, the time delay of the conventional domino logic varies from 139 ps (for eight activated inputs) to 142 ps (for one activated input). For eight serially connected devices, the minimum aspect ratio required for the PDN devices is six in order for the devices to be able to discharge C_L in spite of the contention current and thus obtain an acceptable noise margin. This is certainly an area penalty especially for increased number of inputs. The time delay associated with the latter case is 180 ps. In contrast to this, according to the proposed domino logic in case of the series connection of devices, there is no need to increase the aspect ratios of the devices above two in order to discharge C_L as in the case of the conventional domino logic; a significant saving in area. In addition, the rapid discharging of the dynamic-node capacitance results in a signal with a small fall time, thus reducing the short-circuit power consumption of the following inverter.

In the following, the performance of the proposed domino logic is verified with the effects of the input-capacitive coupling ratios on the time delay investigated. The input-capacitive coupling ratio can be simply adjusted by using suitable values for the corresponding input capacitance. Refer to Fig. 10 for the relationships between these coupling ratios and the discharging time delay of the dynamic-node capacitance according to the proposed scheme for the case of parallelly connected devices in the PDN. The worst-case scenario; that is, one activated input, is adopted. It is apparent that the time delay monotonically decreases with increasing k_3. This is certainly due to enhancing the strength of the FGMOS discharger, thus speeding-up the discharging process. However, this is not the case for the relationship with respect to k_4 in which the time delay shows a monotonic increase as shown in Fig. 10(b). This is due to the fact that the *CLK* signal is at V_{DD} at the beginning of the evaluation phase in contrast to the output node which is at 0 V at the beginning of the discharging process.

Concerning the effects of k_1 and k_2 on the time delay, it is beneficial to decrease the former and increase the latter as depicted in Figs. 10(c) and (d). Clearly, weakening the FGMOS keeper reduces the contention current, thus the time delay reduces. Similar statements can be said with respect to the case of serially connected devices in the PDN; the corresponding plots are shown in Fig. 11.

6.4. Effect of the Fan-Out Capacitance

Refer to Fig. 12 for the effect of the fan-out capacitance on the discharging time delay and the average power consumption for the conventional and proposed domino logic. The time delay is evaluated in this subsection at the output node in order to evaluate the effect of increasing the fan-out capacitance. The average power consumption, P_{avg}, is obtained from simulation using the transient analysis at a relatively large time interval. 100 ns is the adopted time interval here and the clock frequency is taken equal to 1 GHz. The monotonic increase of the time delay and the average power consumption of both the conventional and proposed domino logic with the fan-out capacitance is expected. It is clear that the proposed domino logic has a lower time delay and power consumption for all values of the load capacitances.

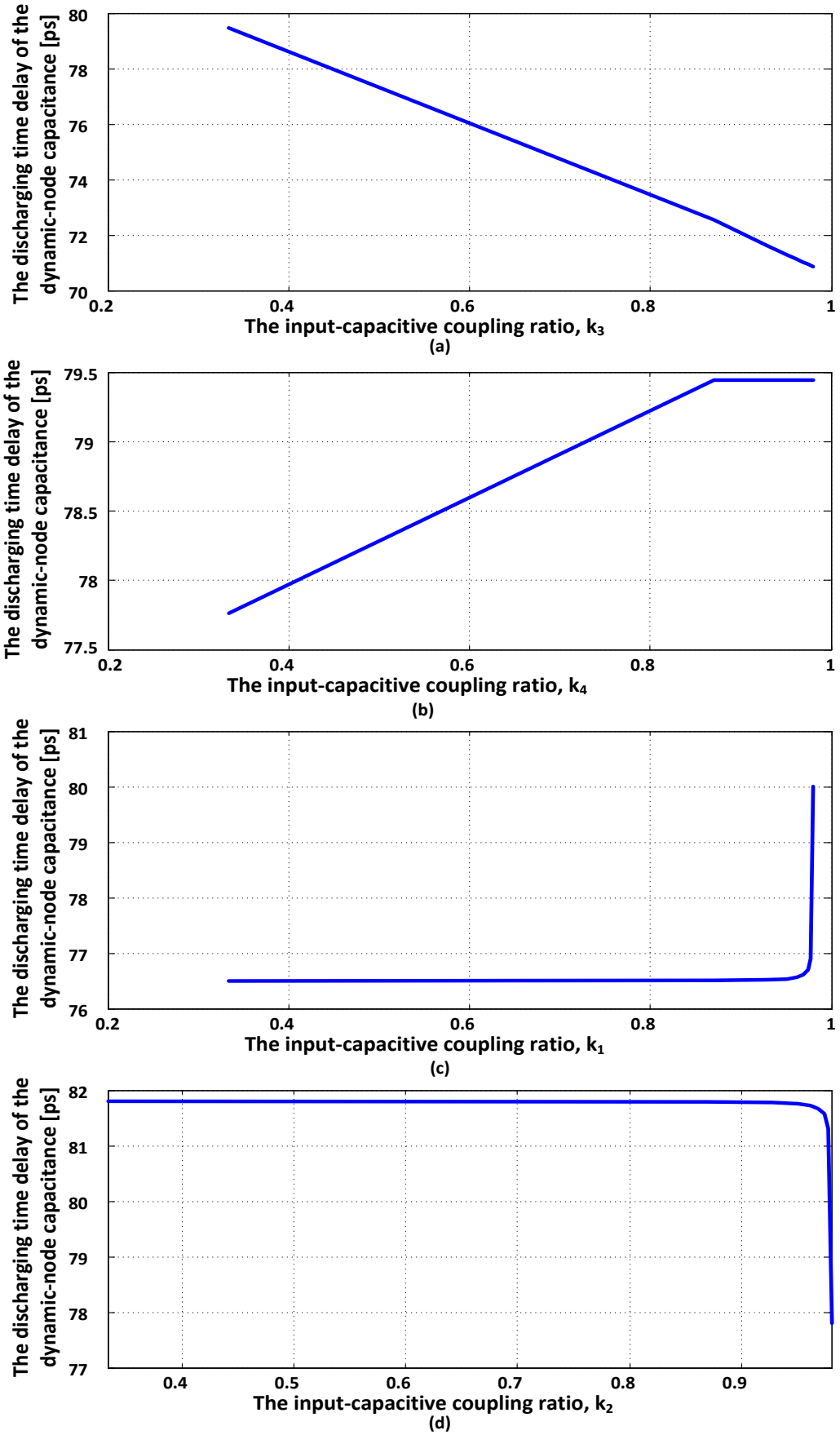

Fig. 10. Relationship between the discharging time delay of the dynamic-node capacitance and each of the following input-capacitive coupling ratios: a) k_3; b) k_4; c) k_1; d) k_2 for OR gates.

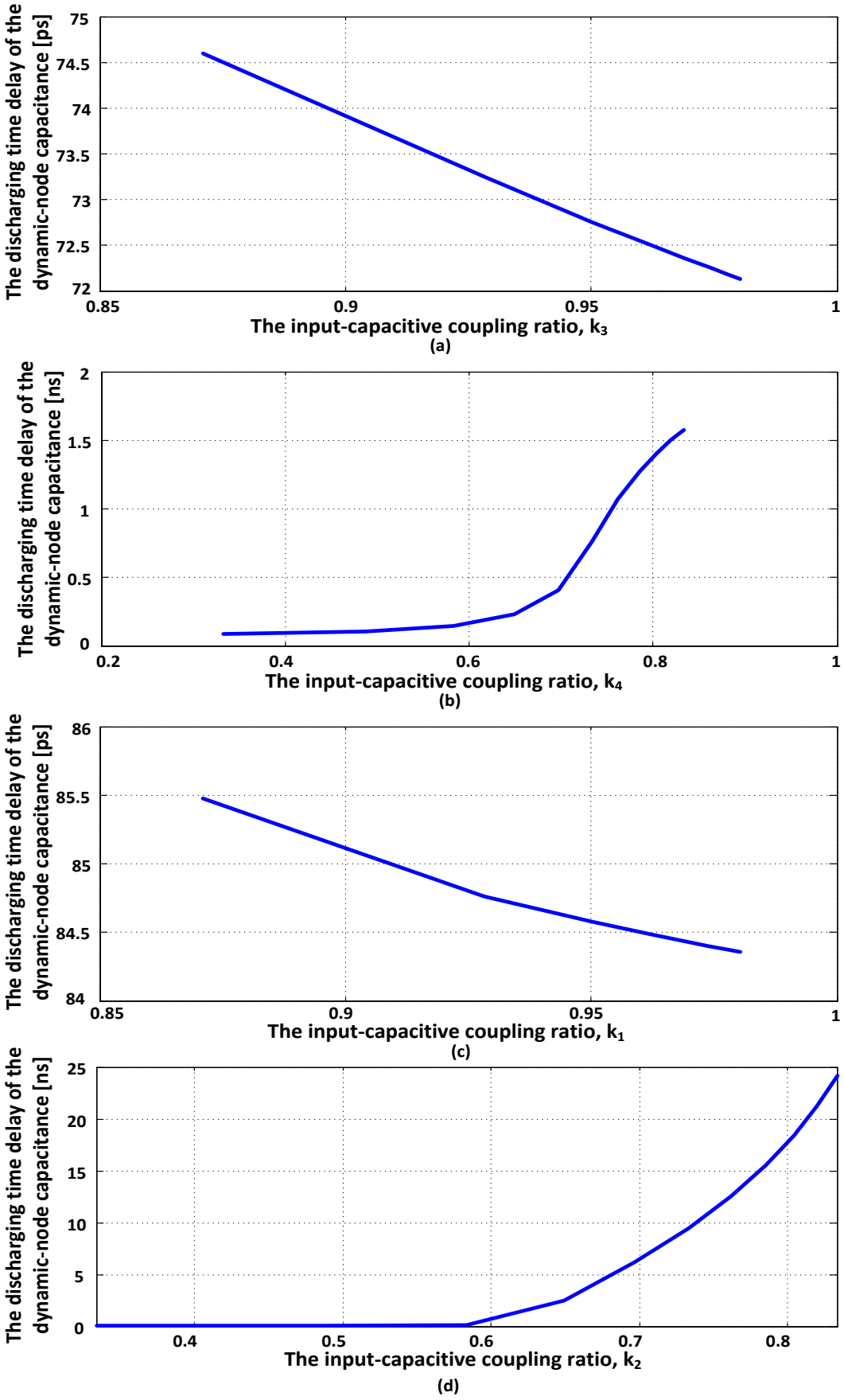

Fig. 11. Relationship between the discharging time delay of the dynamic-node capacitance and each of the following input-capacitive coupling ratios: a) k_3; b) k_4; c) k_1; d) k_2 for AND gates.

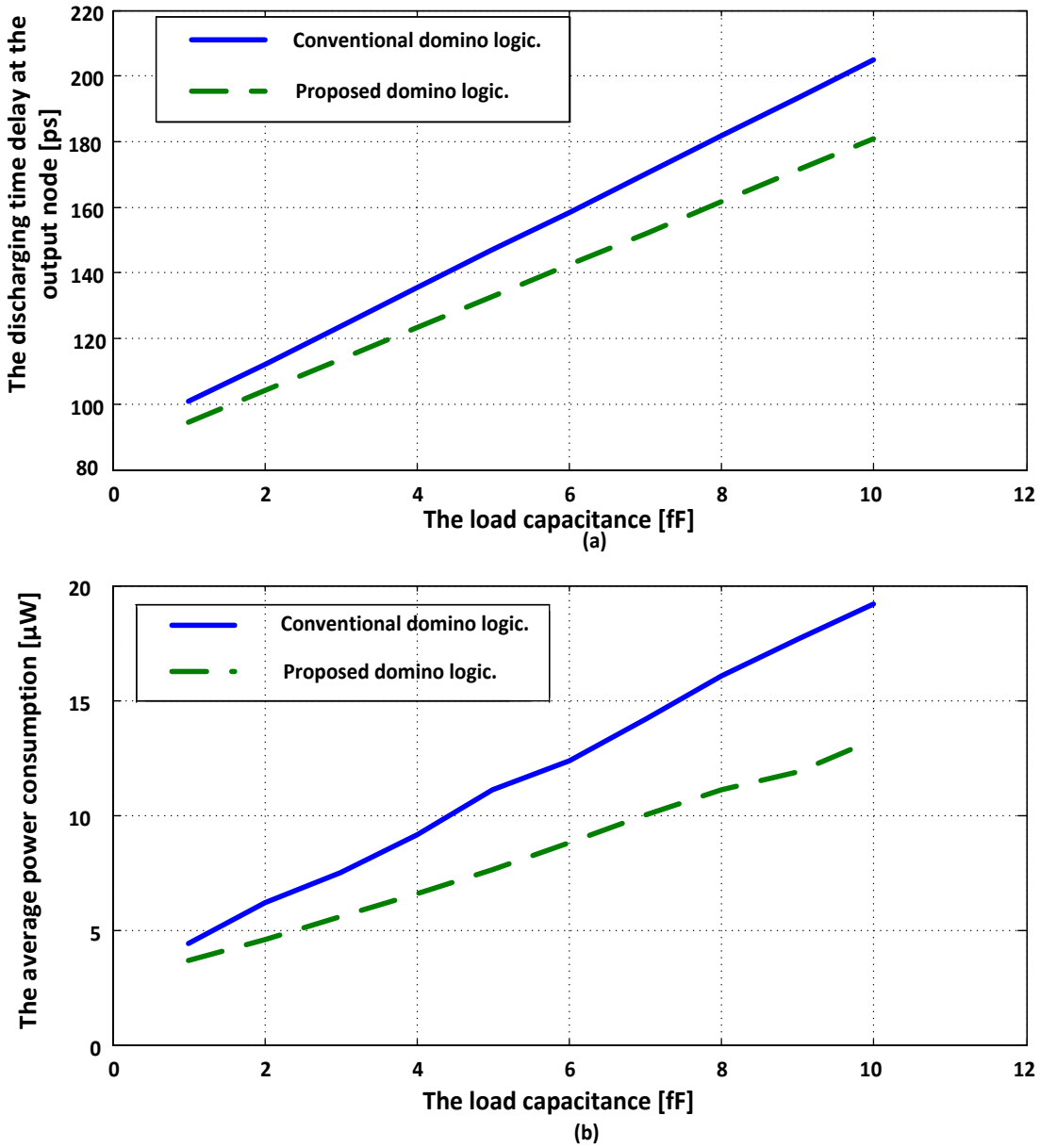

Fig. 12. Effect of the fan-out capacitance on the: a) discharging time delay; b) average power consumption.

6.5. Effect of the Power-Supply Voltage

The power-supply voltage scales down with scaling down the dimensions of the MOS transistors in order to obviate breakdown and reduce the dynamic-switching power consumption [73]. So, investigating the performance of the proposed domino logic when scaling down V_{DD} seems important. Fig. 13 is the counterpart of Fig. 12 but with the effect of the power-supply voltage on the discharging time delay and the average power consumption investigated. The reduction of the time delay and the increase of the average power consumption with increasing V_{DD} are axiomatic. The proposed domino logic shows superior performance also with V_{DD} reduction and thus the proposed domino logic seems attractive when applied on deep-submicron CMOS technologies.

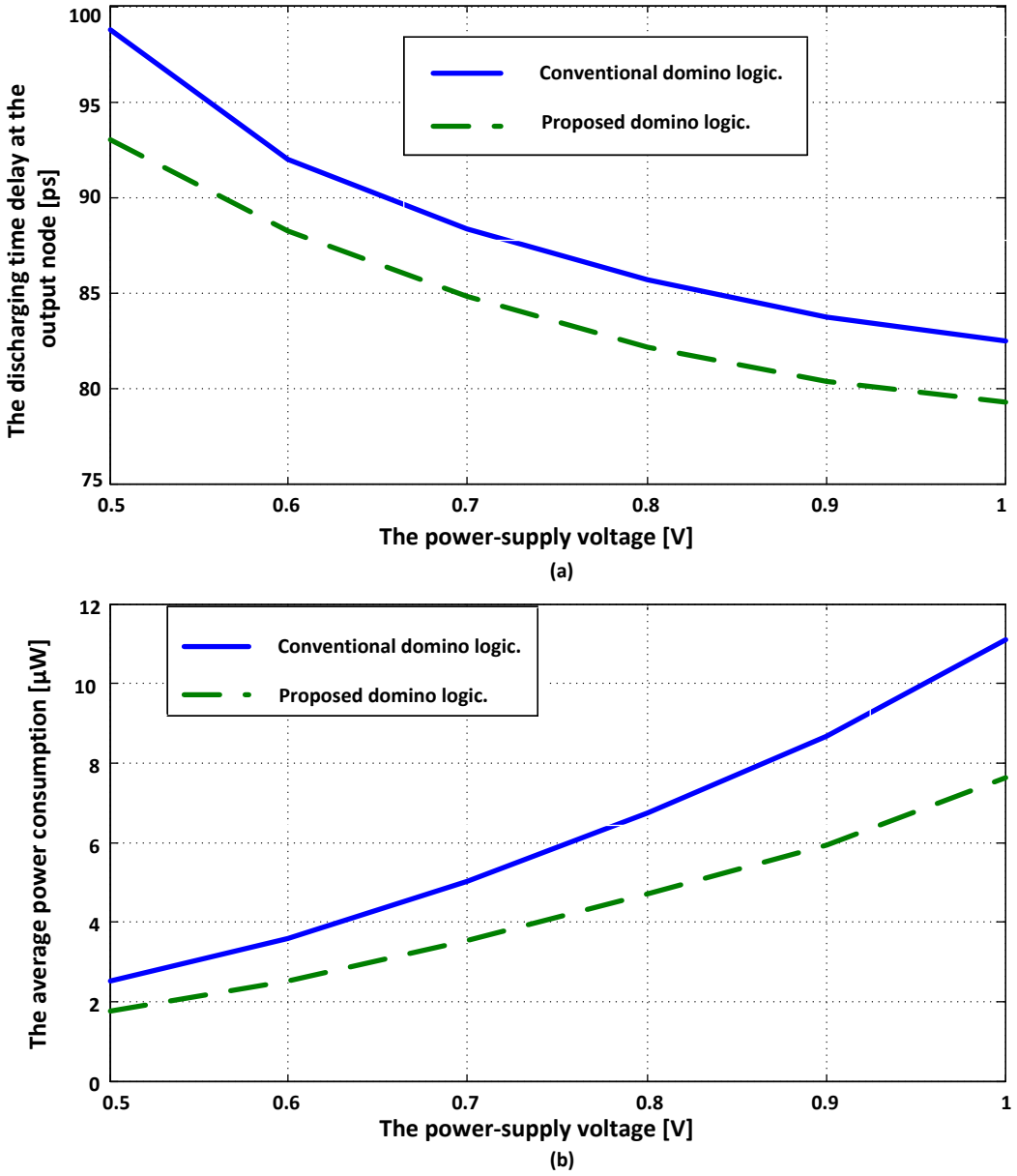

Fig. 13. Effect of the power-supply voltage on the: a) discharging time delay; b) average power consumption.

6.6. Effect of the Number of Inputs

Since the domino logic is suitable for application with wide fan-in OR gates, its investigation under several number of inputs is very important. Fig. 14 is the counterpart of Fig. 12 but with the effect of the number of inputs on the discharging time delay of C_L and the average power consumption investigated. The monotonic increase of the average power consumption of both the conventional and proposed domino logic with n is certainly due to the increase of the dynamic-node parasitic capacitance with increasing n. It is clear that the proposed domino logic has a lower power consumption for all the number of inputs. Although the dynamic-node capacitance according to the proposed domino logic is larger than that according to the conventional one, the reduction of the keeper current has the dominant effect.

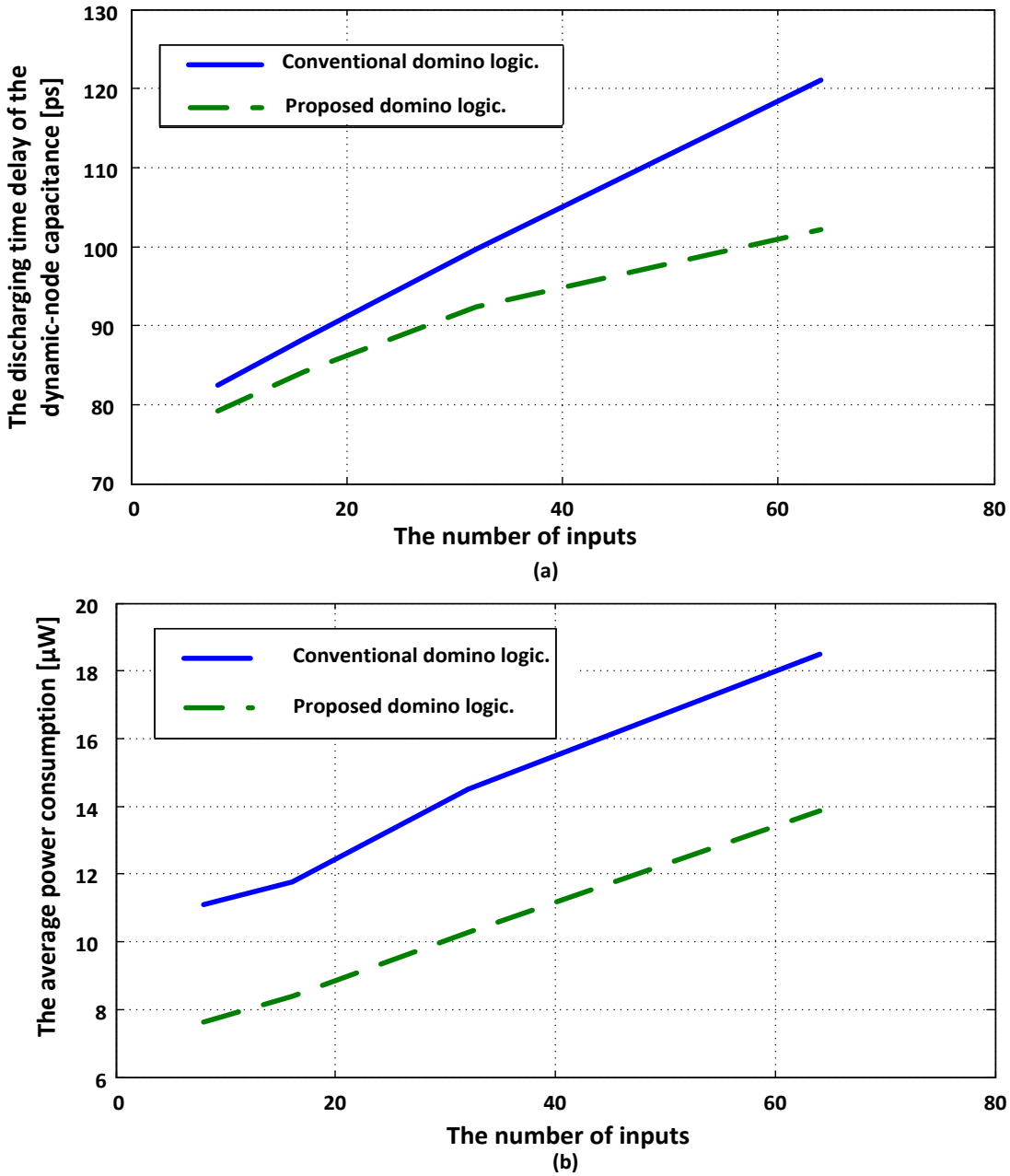

Fig. 14. Effect of the number of inputs on the: a) discharging time delay of the dynamic-node capacitance; b) average power consumption.

6.7. Effect of the Keeper Size

Keeper transistors with sizes larger than the minimum one can be adopted when there is a significant charge sharing and leakage currents. In this subsection, the effect of the keeper size on the performance of the proposed domino logic is investigated. Figs. 15(a) and (b) show the effect of increasing the keeper's size on the time delay and the average power consumption, respectively. According to the conventional domino logic, when the keeper's aspect ratio is increased above three, the dynamic-node capacitance does not discharge below $V_{DD}/2$ resulting in an erroneous output. Thus, the corresponding plots are shown up to three only for the keeper's aspect ratio. Besides, the discharging time delay increases significantly with increasing the keeper's size. In contrast, with the proposed domino logic, the dynamic-node capacitance can discharge below $V_{DD}/2$ even if the keeper's aspect ratio is increased

above ten and the discharging time delay increases at a much slower rate compared to that of the conventional scheme. However, this comes at the expense of a reduced noise margin as expected. Both the time delay and the average power consumption of the proposed domino logic are smaller than those of the conventional one for all sizes of the keeper. This is certainly due to the deactivation of the keeper by virtue of the use of the FGMOS device.

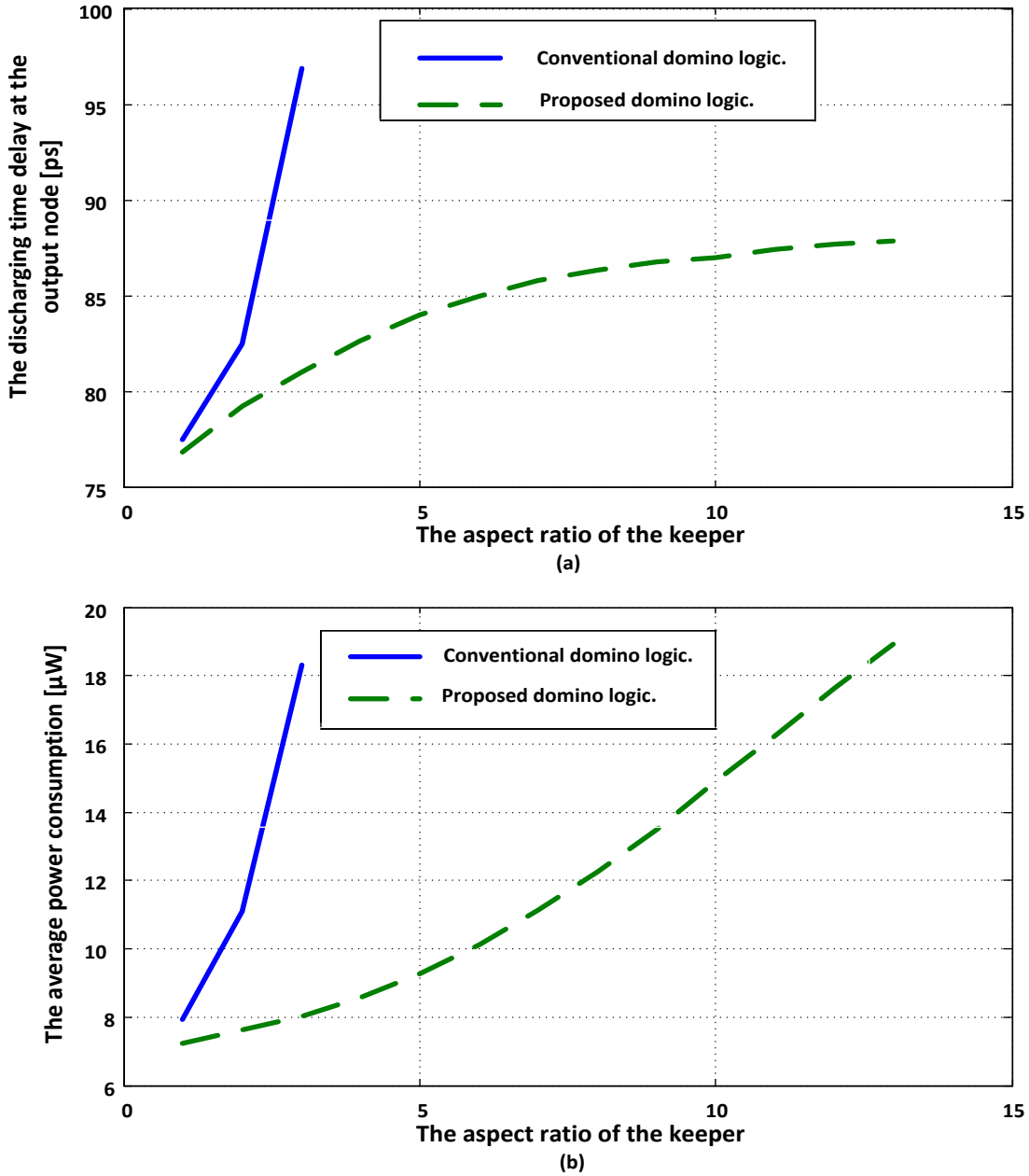

Fig. 15. Effect of the keeper size on the: a) discharging time delay; b) average power consumption.

6.8. Effects of the PVT Variations

In this subsection, the effects of the PVT variations on the effectiveness of the proposed domino logic are taken into account. This is performed in two ways; the corner analysis and Monte-Carlo analysis.

6.8.1. Corner Analysis

The three process corners corresponding to the fast-fast (FF), typical-typical (TT), and slow-slow (SS) cases are investigated according to the following power-supply voltages and temperatures: Best case (FF, 1.1 V, 0 °C), typical case (TT, 1 V, 27 °C), and worst case (SS, 0.9 V, 125 °C). The results of the corner analysis are shown in Table 1. The time delay is evaluated here at the output node in order to take into account the change of the current-driving capability of the output inverter with the PVT variations. The percentage change of the time delay between the SS and FF cases, referred to the typical case, is 11.6%. This represents a relatively small change with regard to the relatively wide temperature and power-supply voltage ranges between the SS and FF cases. This indicates the good robustness of the proposed domino logic with regard to the effect of the PVT variations.

The significant change of the average power consumption with the change of V_{DD} is axiomatic due to the direct proportion of the dynamic-switching power consumption, which represents the dominant part of the power consumption, with the square of the power-supply voltage [73]. It should be noted that since the average noise margin is proportional to V_{DD} and since the current-driving capabilities of the NMOS and PMOS devices change in the same way with temperature for both the conventional and proposed domino logic, the average noise margin will show the same trend of variation with these process corners in both types of domino logic.

Table 1. Results of the corner analysis.

Process corner	Time delay [ps]	Average power consumption [μW]
FF	184.1	12.08
TT	192.85	8.37
SS	206.46	6.15

6.8.2. Monte-Carlo Analysis

To perform Monte-Carlo analysis, 10% Gaussian variations are assumed in each of the channel length and the channel width of each device. 1000 simulation runs are performed. According to this analysis, the mean value of the output is 0.95 V and the standard deviation is 0.014.

6.9. A Figure of Merit

Finally, a figure of merit, *FoM*, that gathers several performance metrics is defined for both the conventional and proposed domino logic to show a fair comparison. The adopted figure of merit is defined as follows:

$$FoM = \frac{1}{At_d P_{avg}} \tag{22}$$

where A, t_d, and P_{avg} represent the area, the time delay, and the average power consumption, respectively. The area of the circuit was estimated as the transistor count. The area of the FGMOS device is taken proportional to the number of the control gates. Thus, each of the two FGMOS devices has an area equal to twice that of the conventional MOSFET. As indicated in Fig. 16, the proposed domino logic has a superior performance for all number of inputs.

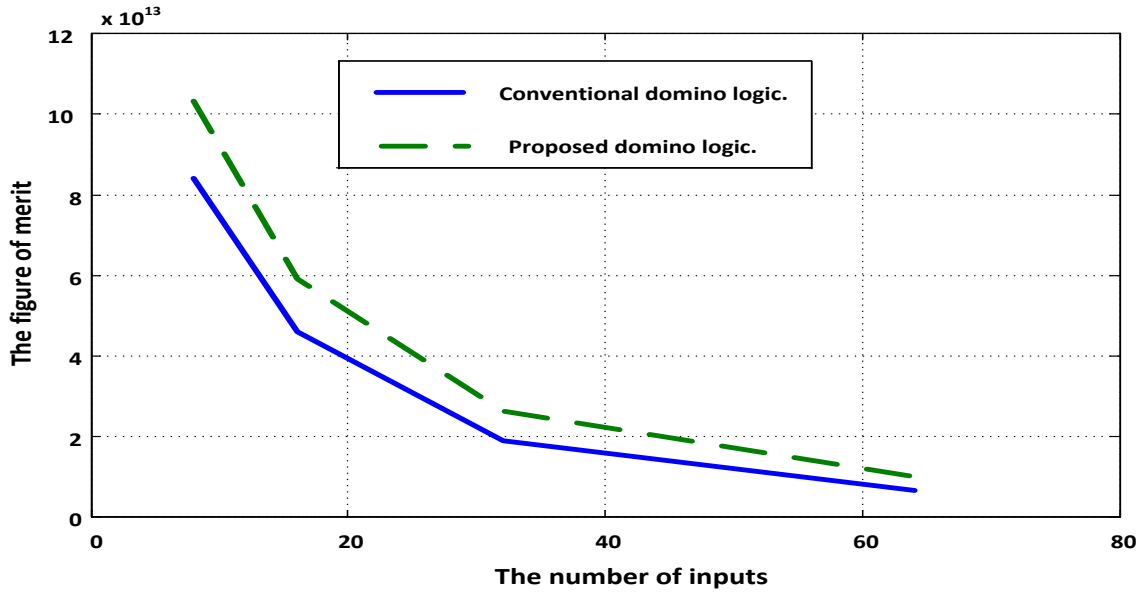

Fig. 16. The proposed figure of merit versus the number of inputs.

6.10. Comparison with Previous Works

A comparison is portrayed in Table 2 (where NA means not available) between the proposed domino logic and some of the previously proposed schemes from the literature review. The load capacitance is set equal to 1 fF as this value represents the load adopted with most of the previous works. The keeper size is put at it its minimum and a 16-input OR gate is adopted. As shown in this table, although the two schemes of [28, 47] have smaller power consumption, the proposed scheme has the lowest power-delay product because of its relatively low time delay. The area of the proposed domino logic is approximately the same as that of the schemes of [47, 49]. All these merits come at the expense of the increased cost of the FGMOS device due to the need to use the double-polysilicon CMOS process [67].

Table 2. Comparison between the proposed scheme and the reported domino logic schemes.

Parameter	Reference				Proposed scheme
	[28]	[46]	[47]	[49]	
Technology	32 nm CMOS	180 nm CMOS	90 nm CMOS	90 nm CMOS	45 nm CMOS
Power-supply voltage [V]	0.9	1.8	1	1	1
Average power consumption [μW]	1.3635	20	3.1	NA*	3.7
Time delay [ps]	452.5	180	70.92	≈ 70	51
Power-delay product [attoJoule]	743	3600	220	NA*	188.7
No. of transistors	11 + PDN = 27	14 + PDN = 30	8 + PDN = 24	8 + PDN = 24	8 + PDN = 24
Noise margin [V]	0.265	0.6	NA*	0.28	0.4

7. CONCLUSIONS

In this paper, a domino logic based on floating-gate MOS transistors was proposed. Unlike the conventional domino logic which is suitable for realizing wide fan-in OR gates only, the proposed FGMOS based domino logic is suitable for realizing both wide fan-in AND

and OR gates. The main advantage of the proposed FGMOS-based domino logic is that the input-capacitive coupling ratios of the added FGMOS devices can be properly chosen with regard to the shape of the PDN so as to get the optimum performance. This is in contrast to the conventional domino logic in which the main design parameters are the aspect ratios of the transistors in the PDN and the keeper. By suitable choice of the input-capacitive coupling ratios of the adopted FGMOS transistors, a significant saving in the area overhead can be achieved in wide fan-in AND gates to obtain a certain time delay. Finally, the proposed domino logic showed better performance compared to the conventional one for wide fan-in gates with various load capacitances, reduced power-supply voltages, and increased keeper sizes.

REFERENCES

[1] Z. Al-Tarawneh, "On metastability resilience of multi-gate MOSFETs," *Jordan Journal of Electrical Engineering*, vol. 1, no. 2, pp. 83-92, 2015.

[2] H. Rayat, R. Dastanian, "A fully MOSFET voltage reference with low power consumption and high power supply rejection ratio for IoT microsystems," *Jordan Journal of Electrical Engineering*, vol. 8, no. 2, pp. 102-113, 2022.

[3] K. Chu, D. Pulfrey, "A comparison of CMOS circuit techniques: differential cascode voltage switch logic versus conventional logic," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 4, pp. 528–532, 1987.

[4] J. Rabaey, A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, Second Edition, Pearson, 2002.

[5] E. Nowak, I. Aller, T. Ludwig, K. Kim, R. Joshi, C. Chuang, K. Bernstein, R. Puri, "Turning silicon on its edge [double gate CMOS/FinFET technology]," *IEEE Circuits and Devices Magazine*, vol. 20, no. 1, pp. 20-31, 2004.

[6] H. Wong, D. Frank, P. Solomon, C. Wann, J. Welser, "Nanoscale cmos," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 537-570, 1999.

[7] S. Ghimiray, P. Dutta, "Low leakage low power domino logic technique for wide fan-in applications, 40-bit tag comparator," *International Journal of Integrated Engineering*, vol. 14, no. 4, 2022.

[8] R. Tocci, N. Widmer, G. Moss, *Digital Systems: Principles and Applications*, Tenth Edition, Prentice-Hall, New Jersey, 2007.

[9] N. Singh, S. Shekhar, A. Angeline, K. Bhaaskaran, "Schmitt trigger designs using domino logic style," *The Electrochemical Society ECS Transactions*, vol. 107, no. 1, 2022.

[10] S. Tawfik, V. Kursun, "FinFET domino logic with independent gate keepers," *Microelectronics Journal*, vol. 40, no. 11, pp. 1531-1540, 2009.

[11] D. Hisamoto, W. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. King, J. Bokor, C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Transactions on Electron Devices*, vol. 47, no. 12, pp. 2320-2325, 2000.

[12] J. Ayers, *Digital Integrated Circuits: Analysis and Design*, CRC Press, 2018.

[13] A. Sedra, K. Smith, *Microelectronic Circuits*, Seventh Edition, Oxford University Press, New York, 2015.

[14] R. Singh, A. Kim, S. Kim, "Footer voltage feedforward domino technique for wide fan-in dynamic logic," *23rd IEEE International SOC Conference*, pp. 224–229, 2010.

[15] H. Mahmoodi-Meimand, K. Roy, "Diode-footed domino: a leakage-tolerant high fan-in dynamic circuit design style," *IEEE Transactions on Circuits and Systems I*, vol. 51, no. 3, pp. 495-503, 2004.

[16] H. Mahmoodi-Meimand, K. Roy, "Diode-footed domino: a leakage-tolerant high fan-in dynamic circuit design style," *IEEE Transactions on Circuits and Systems I*, vol. 51, no. 3, pp. 495 - 503, 2004.

[17] G. Balamurugan, N. Shanbhag, "The twin-transistor noise-tolerant dynamic circuit technique," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 2, pp. 273-280, 2001.

[18] H. Tung, J. Son, C. Kim, N. Wang, S. Kim, "Low power high speed domino logic based on double capacitive body biased keeper," *8th International Conference on Solid-State and Integrated Circuit Technology Proceedings*, pp. 1870–1872, 2006.

[19] A. Alvandpour, P. Larsson-Edefors, C. Svensson, "A leakage-tolerant multi-phase keeper for wide domino circuits," *Proceedings of the 6th IEEE International Conference on Electronics, Circuits and Systems*, vol. 1, pp. 209–212, 1999.

[20] L. Wang, R. Krishwamurthy, K. Soumyanath, N. Shanbhag, "An energy-efficient leakage-tolerant dynamic circuit technique," *Proceedings of 13th Annual IEEE International ASIC/SOC Conference*, pp. 221–225, 2000.

[21] F. Frustaci, P. Corsonello, S. Perri, G. Cocorullo, "High-performance noise-tolerant circuit techniques for CMOS dynamic logic," *IET Circuits, Devices and Systems*, vol. 2, no. 6, pp. 537–548, 2008.

[22] R. Singh, A. Kim, S. Kim, "Footer voltage feedforward domino technique for wide fan-in dynamic logic," *23rd IEEE International SOC Conference*, pp. 224–229, 2010.

[23] R. Singh, G. Hong, S. Kim, "Bitline techniques with dual dynamic nodes for low-power register files," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 4, pp. 965–974, 2013.

[24] K. Roy, S. Mukhopadhyay, H. Mahmoodi, "Leakage current mechanisms and leakage reduction techniques in deep submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305-327, 2003.

[25] L. Wang, N. Shanbhag, "An energy-efficient noise-tolerant dynamic circuit technique," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 11, pp. 1300–1306, 2000.

[26] W. Chiu, H. Lin, "A conditional isolation technique for low-energy and high-performance wide domino gates," *IEEE Region 10 Conference*, pp. 1–4, 2007.

[27] M. Nasseriana, M. Kangi, M. Nejad, F. Moradi, "A low-power fast tag comparator by modifying charging scheme of wide fan-in dynamic OR gates," *Integration, the VLSI journal*, vol. 52, pp. 129–141, 2016.

[28] A. Dadoria, K. Khare, T. Gupta, R. Singh, "A novel high-performance leakage-tolerant, wide fan-in domino logic circuit in deep-submicron technology," *Circuits and Systems*, vol. 6, pp. 103-111, 2015.

[29] M. Khellah, M. Elmasry, "Use of charge sharing to reduce energy consumption in wide fan-in gates," *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 9–12, 1998.

[30] M. Khellah, *Low-Power Digital CMOS VLSI Circuits and Design Methodologies,* Doctor of Philosophy Thesis, Waterloo, Ontario, Canada, 1999.

[31] K. Oh, L. Kim, "A clock delayed sleep mode domino logic for wide dynamic OR gate," *Proceedings of the International Symposium on Low Power Electronics and Design*, pp. 176–179, 2003.

[32] M. Allam, M. Anis, M. Elmasry, "High-speed dynamic logic styles for scaled-down CMOS and MTCMOS technologies," *Proceedings of the International Symposium on Low Power Electronics and Design*, pp. 155–160, 2000.

[33] S. Heo, K. Asanovic, "Leakage-biased domino circuits for dynamic fine-grain leakage reduction," *Symposium on VLSI Circuits*, pp. 316–319, 2002.

[34] F. Moradi, A. Peiravi, "An improved noise-tolerant domino logic circuit for high fan-in gates," *International Conference on Microelectronics*, pp. 116–121, 2005.

[35] S. Aiswarya, "CCD based new domino circuit using clamped bit line sense amplifier," *International Conference on Innovations in Information, Embedded and Communication Systems*, pp. 1–6, 2015.

[36] M. Manzoor, S. Verma, M. Manzoor, "Noise tolerant techniques in dynamic CMOS logic style: a review paper," *Fifth International Conference on Communication Systems and Network Technologies*, pp. 876–880, 2015.

[37] B. Fu, P. Ampadu, "Techniques for robust energy efficient subthreshold domino CMOS circuits," *IEEE International Symposium on Circuits and Systems*, pp. 1247–1250, 2006.

[38] H. Meimand, K. Roy, "Diode-footed domino: a leakage-tolerant high fan-in dynamic circuit design style," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 3, pp. 495–503, 2004.

[39] J. Kao, *Subthreshold Leakage Control Techniques for Low Power Digital Circuits*, Doctor of Philosophy Thesis, Massachusetts Institute of Technology, 2001.

[40] V. Mahor, A. Chouhan, M. Pattanaik, "A process variation tolerant low contention keeper design for wide fan-in dynamic OR gate," *International Symposium on Electronic System Design*, pp. 151–153, 2012.

[41] H. Dadgour, K. Banerjee, "A novel variation-tolerant keeper architecture for high-performance low-power wide fan-in dynamic or gates," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 18, no. 11, pp. 1567–1577, 2010.

[42] S. Mehrotra, S. Patnaik, M. Pattanaik, "Design technique for simultaneous reduction of leakage power and contention current for wide fan-in domino logic based 32:1 multiplexer circuit," *IEEE Conference on Information and Communication Technologies*, pp. 905–910, 2013.

[43] S. Sharroush, Y. Abdalla, A. Dessouki, E. El-Badawy, "A novel technique for speeding up domino CMOS circuits containing a long chain of NMOS transistors," *International Conference on Electronic Design*, pp. 1–9, 2008.

[44] A. Dadoria, K. Khare, U. Panwar, A. Jain, "Performance evaluation of domino logic circuits for wide fan-in gates with FinFET," *Microsystem Technologies*, vol. 24, no. 8, pp. 3341-3348, 2018.

[45] A. Peiravi, M. Asyaei, "Current-comparison-based domino: New low-leakage high-speed domino circuit for wide fan-in gates," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 21, no. 5, pp. 934-943, 2012.

[46] M. Asyaei, "A new low-power dynamic circuit for wide fan-in gates," *Integration*, vol. 60, pp. 263-271, 2018.

[47] A. Angeline, V. Bhaaskaran, "High speed wide fan-in designs using clock controlled dual keeper domino logic circuits," *ETRI Journal*, vol. 41, no. 3, pp. 383-395, 2019.

[48] A. Angeline, V. Kanchana Bhaaskaran, "Design impacts of delay invariant high-speed clock delayed dual keeper domino circuit," *IET Circuits, Devices and Systems*, vol. 13, no. 8, pp. 1134-1141, 2019.

[49] A. Angeline, V. Bhaaskaran, "Speed enhancement techniques for clock-delayed dual keeper domino logic style," *International Journal of Electronics*, vol. 107, no. 8, pp. 1239-1253, 2020.

[50] A. Pandey, S. Upadhyay, T. Gupta, P. Verma, "Low power, high speed and noise immune wide-OR footless domino circuit using keeper controlled method," *Analog Integrated Circuits and Signal Processing*, vol. 100, no. 1, pp. 79-91, 2019.

[51] A. Mehra, S. Singhal, and U. Tripathi, "A novel domino logic with modified keeper in 16nm CMOS technology," *Electronics*, vol. 23, no. 2, 2019.

[52] S. Singhal, A. Mehra, "Gated clock and revised keeper (GCRK) domino logic design in 16 nm CMOS technology," *IETE Journal of Research*, pp. 1-8, 2021.

[53] H. Mostafa, M. Anis, M. Elmasry, "Novel timing yield improvement circuits for high-performance low-power wide fan-in dynamic OR gates," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 8, pp. 1785–1797, 2011.

[54] A. Dev, R. Sharma, "An efficient design technique for low power dynamic feedthrough logic with enhanced performance for wide fan-in gates," *2nd International Conference on Signal Processing and Integrated Networks*, pp. 908–912, 2015.

[55] M. Asyaei, "A new leakage-tolerant domino circuit using voltage-comparison for wide fan-in gates in deep sub-micron technology," *Integration*, vol. 51, pp. 61–71, 2015.

[56] S. Hafeez, A. Ross, B. Parhami, "Scalable digital CMOS comparator using a parallel prefix tree," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 11, pp. 1989–1998, 2013.

[57] S. Sharroush, "A novel current-race fast CMOS circuit," *5th International Conference on Electronic Devices, Systems and Applications*, pp. 1–4, 2016.

[58] A. Angeline, V. Kanchana Bhaaskaran, "High speed wide fan-in designs using clock controlled dual keeper domino logic circuits," *ETRI Journal*, vol. 41, no. 3, pp. 383-395, 2019.

[59] A. Angeline, V. Kanchana Bhaaskaran, "Design impacts of delay invariant high-speed clock delayed dual keeper domino circuit," *IET Circuits, Devices and Systems*, vol. 13, no. 8, pp. 1134- 141, 2019.

[60] A. Pandey, T. Gupta, A. Gupta, D. Pandey, "Keeper effect on nano scale silicon domino logic transistors," *Silicon*, 2021.

[61] J. Kandpal, T. Pokhrel, S. Saini, A. Majumdera, "A variation resilient keeper design for high performance domino logic applications," *Integration*, vol. 88, pp. 1-9, 2023.

[62] D. Vaithiyanathan, R. Kumar, A. Rai, K. Sharma, "Performance analysis of dynamic CMOS circuit based on node-discharger and twist-connected transistors," *IET Computers and Digital Techniques*, vol. 14, no. 3, pp. 107–113, 2020.

[63] S. Garg, T. Gupta, "Low power domino logic circuits in deep-submicron technology using CMOS," *Engineering Science and Technology, an International Journal*, vol. 21, no. 4, pp. 625-638, 2018.

[64] A. Angeline, V. Bhaaskaran, "Domino logic keeper circuit design techniques: a review," *Journal of The Institution of Engineers (India) Series B*, vol. 103, no. 3, 2021.

[65] S. Garg, T. Gupta, A. Pandey, D. Pandey, "Impact of silicon stacked transistors on nano scale domino logic," *Silicon*, vol. 14, no. 14, pp. 8455-8465, 2022.

[66] S. Vlassis, S. Siskos, "Differential-voltage attenuator based on floating-gate MOS transistors and its applications," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 11, pp. 1372-1378, 2001.

[67] H. Venkata, *Ternary and Quaternary Logic to Binary Bit Conversion CMOS Integrated Circuit Design using Multiple Input Floating Gate MOSFETs*, Master Thesis, Louisiana State University, 2002.

[68] C. Lackey, *Applications of Quasi-Floating-Gate Transistors for Use in Low-Voltage Closed-Loop Amplifier Circuits*, Master of Science Thesis, New Mexico State University, 2003.

[69] J. Uyemura, *Chip Design for Submicron VLSI: CMOS Layout and Simulation*, First Edition, Thomson, New York, 2006.

[70] A. Sheikholeslami, "Process variation and Pelgrom's law [Circuit Intuitions]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 1, pp. 8–9, 2015.

[71] M. Pelgrom, C. Duinmaijer, A. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1440, 1989.

[72] *Predictive Technology Model*, <http://ptm.asu.edu/modelcard/45nm_MGK.pm>

[73] V. Kursen, E. Friedman, *Multi-Voltage CMOS Circuit Design*, John Wiley and Sons Ltd., Great Britain, 2006.