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# A Capacitance Model for Front- and Back-Gate Threshold Voltage Computation of Ultra-Thin-Body and BOX Double-Insulating Silicon-on-Diamond MOSFET

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***Abstract*—** In this paper, a capacitance model for near threshold voltage computation of Ultra-Thin-Body and BOX (UTBB) Double-Insulating (DI) Silicon-on-Diamond (SOD) MOSFET is proposed. The transistor has a second insulating layer on top of the first insulating layer of a conventional SOD MOSFET which partially covers the diamond layer. The device's simulation results of the front- and back-gate threshold voltages and the computed model's threshold voltages - in terms of gate oxide thickness, silicon film layer thickness, first and second insulating layer thicknesses - are compared. In addition, length of the source/drain overlap with the second insulating layer is varied and the device simulation results are compared with those of the model findings. Results of the aforesaid comparison are found to be promising; more than 20 mV change in front-gate threshold voltage is observed at the range of 5 nm to 43 nm. Moreover, the model is found to be applicable in computations of front- and back-gate threshold voltage of 22 nm DI UTBB SOD MOSFET for low drain voltages. Finally, the model's physical findings present insight on the device's parameters that directly influence the threshold voltage.

***Keywords*—** **Ca**pacitance model; Silicon-on-insulator; Threshold voltage; Double-insulating silicon-on-diamond MOSFET.

## 1. INTRODUCTION

Today, transistors have undoubtedly become one of the most important practical components of modern electronics, in such a way that it is practically impossible to imagine the world without the presence of these devices. All transistors are made of semiconductor elements such as silicon and germanium, and the first transistors were made of germanium semiconductors [1]. A very important goal in the design of integrated circuits is to reduce power consumption and achieve high speed and proper performance. In this industry, due to the need to increase the number of devices on the chip and increase their productivity, the process of reducing the dimensions of transistors has been continuously carried out for decades [2-5]. However, the miniaturization of bulk devices has reached its limit due to the appearance of problems such as short channel effects [6]. These effects, the most important of which include an increase in the sub-threshold slope, an increase in the gate tunneling current, and an increase in the drain-induced-barrier-lowering (DIBL), affect the threshold voltage and cause an increase in the leakage current in the off-state and thus increase the power dissipation [7].

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For this reason, the use of silicon-on-insulator (SOI) devices has increased significantly compared to the past, so that in the modern world of electronics, these devices are used as the core technology [8, 9]. The main difference between bulk technology compared to SOI devices, which are generally divided into two groups of fully-depleted (FD) devices and partially-depleted (PD) devices, is the presence of a buried insulating layer of silicon dioxide (SiO2) in their body, which is called (BOX) for short. In PD SOI devices, the thickness of the gate oxide silicon layer is more than twice the maximum width of the depletion layer. In these devices, when the silicon film is depleted, a neutral region is created in the silicon layer. These transistors are also called thick layer devices but, in FD SOI devices, the thickness of the silicon layer under the gate is smaller than the maximum value of the depletion layer, and the silicon layer is completely depleted. These transistors are also known as thin film devices [10]. The oxide buried in the substrate of SOI devices causes a decrease in the capacity of the source and drain the parasitic capacitor (due to the insulation of the top layer of silicon from the substrate) and increases the switching speed [11]. Also, increasing the resistance against radioactive radiations, reducing the short channel effects [12] and solving the latch up problem are other positive features of these devices [13].

However, the structure of these devices is not perfect and since silicon dioxide is a thermal insulator, it strongly prevents the transfer of heat from the device to the heat sink and its cooling [14]. As the temperature of the device increases, the speed of electrons decreases due to collisions with silicon atoms, which reduces the transistor current [15-18].

One of the solutions of semiconductor device manufacturing technology engineers to deal with the self-heating effects of these devices is to use a diamond layer with a thermal conductivity coefficient ($\kappa$=2000 W/K-m) instead of silicon dioxide ($\kappa$=1.4 W/K-m). By replacing these materials with each other, a new transistor called silicon-on-diamond (SOD) has emerged. In these devices, heat transfer is done vertically to the sub-layer and horizontally to the internal joints. For this reason, these devices can be mentioned as a suitable solution to eliminate the self-heating effects of SOI devices. This capability allows these devices to operate at higher power levels than SOI devices. Also, the experimental results show that the new structure has the ability to work with 10 times more power density than SOI devices.

However, when we use an insulator such as diamond with a greater dielectric constant than silicon dioxide, its parasitic capacitance increases, which can be seen from Eq. (1):

$$C_{BOX(SOI)\times} \times \frac{\varepsilon_{Diamond}}{\varepsilon_{SiO2}} = C_{BOX(SOD)} \quad (1)$$

As a result, the body capacitor inside the diamond layer is larger than the silicon dioxide layer capacitor, according to which, the drain in SOD transistors has a greater effect on the body than SOI, which causes an increase in DIBL and leakage current in these devices. For this reason, the need for a structure like silicon-on-diamond with double insulating-layer (DI SOD) is strongly felt to maintain the advantages of a silicon-on-diamond device [19, 20].

The structure of a DI SOD device as depicted in Fig. 1 includes a silicon substrate, a diamond insulating layer on the substrate, a second insulating layer ($SiO_2$) on the diamond (which does not cover all parts of the diamond), a silicone body on the second insulator, and finally a gate on the body. In the structure of these devices, there is a direct relationship between the thickness of the second insulating layer and the penetration of the field from the source and drain to the body.

Since the structure of DI SOD MOSFET includes a second insulating layer which partially covers the diamond layer, a new capacitance model is included to take into consideration the effects of capacitance related to this layer. Therefore, the source/drain overlap with the second insulating layer and the device body constitute a co-planar plate capacitance. In addition, perpendicular-plate capacitance associated with the second insulating layer sidewall to the back-body interface has substantial impact on the threshold voltage behavior of the device. The former influences the threshold voltage and is evident at larger second insulating layer lengths and the latter impacts the device threshold voltage on smaller second insulating layer lengths. The parallel-plate capacitance of the gate-oxide, the thin-body silicon-film, the second insulating layer, the diamond layer and the substrate depletion layer are included in the capacitance model to have their impacts on the front- and back-gate threshold voltages. The co-planar plate capacitance of the source/drain bottom region to the factious electrode at SiO2/diamond interface and diamond/substrate interface are also included. The comprehensive model, takes into account major DI UTBB SOD MOSFET parameter values for threshold voltage computation at low drain voltage.

This rest of the paper is organized as follows: section 2 explains the threshold voltage computation model, device simulation results are discussed in section 3, followed by conclusions in section 4.

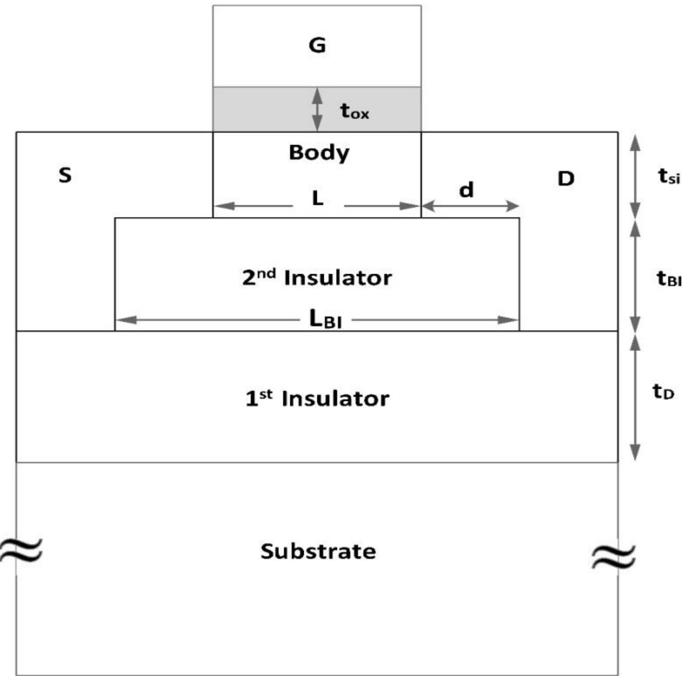


Fig. 1. Cross-sectional view of the DI UTBB SOD MOSFET.

## 2. THRESHOLD VOLTAGE COMPUTATION MODEL

### 2.1. Structure Capacitors

The existing circuit model for the DI SOD MOSFET qualitatively predicts the capacitance elements that influence the body of the device. However, a more comprehensive circuit model is required to compute the front- and back-channel surface potentials. For this reason, the need for a more complete circuit model to accurately predict the device's behavior

is strongly felt. Fig. 2 is a generalized circuit model of the device. In this part, we will examine the capacitors of the circuit model. $C_{OX}$ and $C_{si}$ capacitors, which are related to the oxide gate and silicon film capacitors, mainly represent body capacitors. However, the capacitor $C_{D1}$ represents the capacitor in the middle of the body area up to the overlapping part of the drain with the second insulating layer, which is shown in Fig. 1 by the parameter d. The capacitor $C_{D2}$ corresponds to the capacitor of the middle region of the body with the side edge of the second oxide layer, which is shown by $t_{BI}$ in Fig. 1. $C_{S1}$, $C_{S2}$ capacitors have exactly the same relations for their calculation and they are located only on the source side of the transistor. $C_{ins}$ is also the capacitor in the middle of the body of the device, whose plates are placed in parallel in the body and the second insulator. $C_{D3}$ and $C_{S3}$ capacitors correspond respectively to capacitors whose plates are placed in the second insulating layer and the bottom of the drain and source regions. $C_{inst}$ is a capacitor with parallel plates of the first insulating layer which is made of diamond in Fig. 1. In transistors with very thin buried insulation, a region depleted of carriers and the reverse layer is formed under the first insulation layer. The $C_{ins1}$ capacitor is related to the formation of the capacitor between the source and the drain with the same reverse layer. Finally, the capacitor $C_{sub}$, which is related to the capacitor of the said depletion region in the substrate, is modeled in this way. The voltages of different nodes of the circuit model are shown in Fig. 2.

To calculate the capacitors of parallel and vertical plates, the relationships obtained in [21] and [22] have been used. In this method, which is calculated using elliptic integral functions of capacitors with angled plates along with the marginal electric field, the capacitors mentioned in Fig. 2 can be calculated accurately.

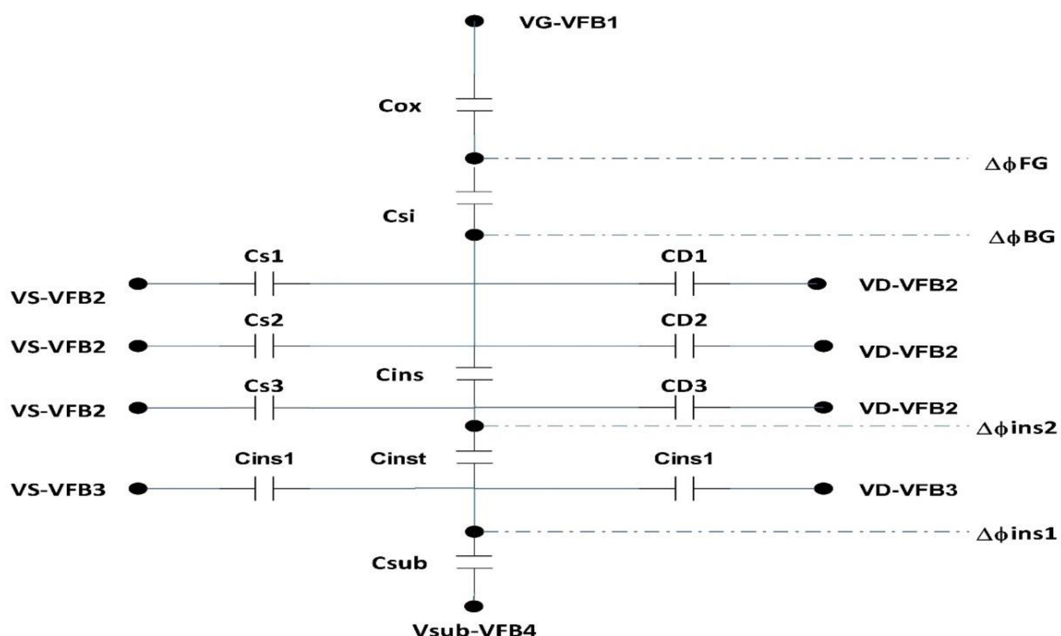


Fig. 2. The proposed capacitance model near threshold voltage of DI UTBB SOD MOSFET.

## 2.2. Threshold Voltage Calculation

By calculating the capacitors of the structure, it is possible to formulate the threshold voltage for the DI SOD device. For this purpose, with the help of Ohm's law, a model should

be developed based on the analytical solution of the node matrix for the back-gate (on the buried oxide/body boundary) and front-gate (on the gate/body oxide boundary).

The back channel is important in devices that have a short channel or have a thick buried insulator, because of the connection between the source and the drain through the buried insulation. Due to this connection of the source and the drain, the inversion of the channel can happen at the back border of the channel region. Therefore, in the same conditions, the surface potential of the back-gate may overcome the surface potential of the front-gate, and in this way, it is possible to create an inversion in it before the front-gate.

### *2.2.1. Node Equations*

In order to calculate the threshold voltage of DI SOD devices, we use the solution of the node matrix in the circuit model of Fig. 2 [23, 24] and by applying these rules and converting the voltage sources into current, the matrix Eq. (2) is obtained.

$$[A]\cdot[B]=[C]\rightarrow[B]=[A]^{-1}\cdot[C] \tag{2}$$

where the matrix [A] is the admittance matrix and the matrices [B] and [C] are the node matrix and the current source matrix, respectively:

$$[A]=\begin{bmatrix} C_{ox}+C_{si} & -C_{si} & 0 & 0 \\ -C_{si} & C_{si}+C_{D1}+C_{D2}+C_{S1}+C_{S2}+C_{ins} & -C_{ins} & 0 \\ 0 & -C_{ins} & C_{ins}+C_{S3}+C_{D3}+C_{inst} & -C_{inst} \\ 0 & 0 & -C_{inst} & 2C_{ins1}+C_{sub}+C_{inst} \end{bmatrix}$$

$$[B]=\begin{bmatrix} \Delta\varphi_{FG} \\ \Delta\varphi_{BG} \\ \Delta\varphi_{ins2} \\ \Delta\varphi_{ins1} \end{bmatrix} \tag{3}$$

$$[C]=\begin{bmatrix} (V_G-V_{FB1})C_{ox} \\ (V_S-V_{FB2})C_{S1}+(V_S-V_{FB2})C_{S2}+(V_D-V_{FB2})C_{D1}+(V_S-V_{FB2})C_{D2} \\ (V_S-V_{FB2})C_{S2}+(V_D-V_{FB2})C_{D3} \\ (V_S-V_{FB3})C_{ins1}+(V_D-V_{FB3})C_{ins1}+(V_{Sub}-V_{FB4})C_{sub} \end{bmatrix}$$

From the above equation, we can see that $\Delta\varphi_{FG}$ is the surface potential of the front-gate and $\Delta\varphi_{BG}$ is the potential of the back-gate.

### *2.2.2. Calculation of Front-Gate Threshold Voltage*

In order to calculate the threshold voltage of the front-gate, that value of the gate voltage can be considered optimal where the minimum surface potential $\Delta\varphi_{FG}$ is twice the Fermi-potential $2\Psi_B$ [1]. So, by solving the node matrix obtained in the previous part and substituting $2\Psi_B$ instead of $\Delta\varphi_{FG}$, the front-gate threshold voltage equation is calculated as in Eq. (4):

$$V_{th-FG}=\frac{2\Psi_B\,(C_{ox}+C_{si}-C_{si}^2/X)}{Cox}-\frac{C_{si}}{C_{ox}}\left(\frac{YC_{ins}+Z}{X}\right)+V_{FB1} \tag{4}$$

A, B, X, Y and Z are determined from Eqs. (5) to (9):

$$A=\frac{(V_S-V_{FB3})C_{ins1}+(V_D-V_{FB3})C_{ins1}+(V_{Sub}-V_{FB4})C_{sub}}{2C_{ins1}+C_{inst}+C_{sub}} \tag{5}$$

$$B=C_{ins}+C_{S3}+C_{D3}+C_{inst}-\frac{C_{inst}^2}{2C_{ins1}+C_{inst}+C_{sub}} \tag{6}$$

$$X=C_{si}+C_{D1}+C_{D2}+C_{S1}+C_{S2}+C_{ins}-\frac{C_{ins}^2}{B} \tag{7}$$

$$Y = \frac{(V_S - V_{FB2})C_{S3} + (V_D - V_{FB2})C_{D3} + AC_{inst}}{B} \quad (8)$$

$$Z = (V_S - V_{FB2})C_{S1} + (V_D - V_{FB2})C_{D1} + (V_S - V_{FB2})C_{S2} + (V_D - V_{FB2})C_{D2} \quad (9)$$

*2.2.3. Calculation of Back-Gate Threshold Voltage*

In order to calculate the threshold voltage of the back-gate, that value of the gate voltage should be taken into account as the threshold voltage when the minimum potential of the back-gate surface $\Delta\varphi_{BG}$ is equal to $2\Psi_B$. So, by solving matrix in Eq. (2) and substituting $2\Psi_B$ instead of $\Delta\varphi_{BG}$, the back-gate threshold voltage equation is obtained as in Eq. (10):

$$V_{th-BG} = \frac{2\Psi_B(X-Q) - C_{ins}(Y) - (V_S - V_{FB2})(C_{S1}) - (V_D - V_{FB2})(C_{D1}) - (V_S - V_{FB2})C_{S2} + (V_D - V_{FB2})C_{D2}}{U} + V_{FB1} \quad (10)$$

Q and U are determined from Eqs. (11) and (12):

$$Q = \frac{C_{si}}{C_{ox} + C_{si}} \quad (11)$$

$$U = \frac{C_{ox} \cdot C_{si}}{C_{ox} + C_{si}} \quad (12)$$

## 3. DEVICE SIMULATION RESULTS

In this section, we compare the threshold voltage results computed by the model with the device simulation findings.

Fig. 3 shows the results of the modeling and simulation of the threshold voltage of the front-gate in relation to the thickness of the gate oxide. The thickness range of oxide insulation varies from 1.2 nm to 4 nm. As shown, it can be seen that the extracted model follows the capacitor model with an approximate error of 20 mV in the entire range of gate oxide changes.

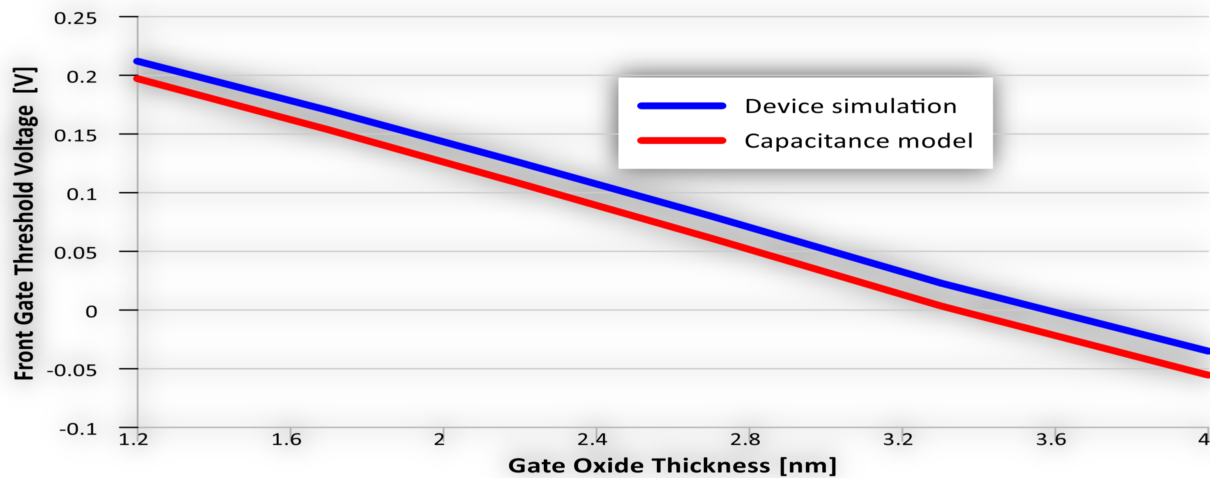


Fig. 3. Front-gate threshold voltage versus gate oxide thickness ($t_{BI}$ =20 nm, $N_{channel}$=$10^{15}$ $cm^{-3}$, $N_{Asub}$=$10^{15}$ $cm^{-3}$, $t_D$=20 nm, $N_{S-D}$=$10^{20}$ $cm^{-3}$, d=43 nm, $V_{DS}$=0 V, T=300 K).

Fig. 4 also shows the results of the simulation and the threshold voltage model of the back-gate of the device in relation to the thickness of the gate oxide in the range of 1.2 to 4 nm. This difference is 1.5 mV at its lowest value in the gate oxide thickness of 1.3 nm and 20 mV in the gate oxide thickness of 4 nm.

The decrease in the front- and back-gate threshold voltages with the increase of oxide thickness, is as a result of losing the impact of gate electrode voltage on the body of the device. Therefore, the back-gate electrostatic affects the device body as the gate-oxide thickness increases. The electric fields initiates from the n+ source/drain regions through the

second insulating layer act as the back gate and invert the un-doped body stronger as the gate-oxide thickness increases.

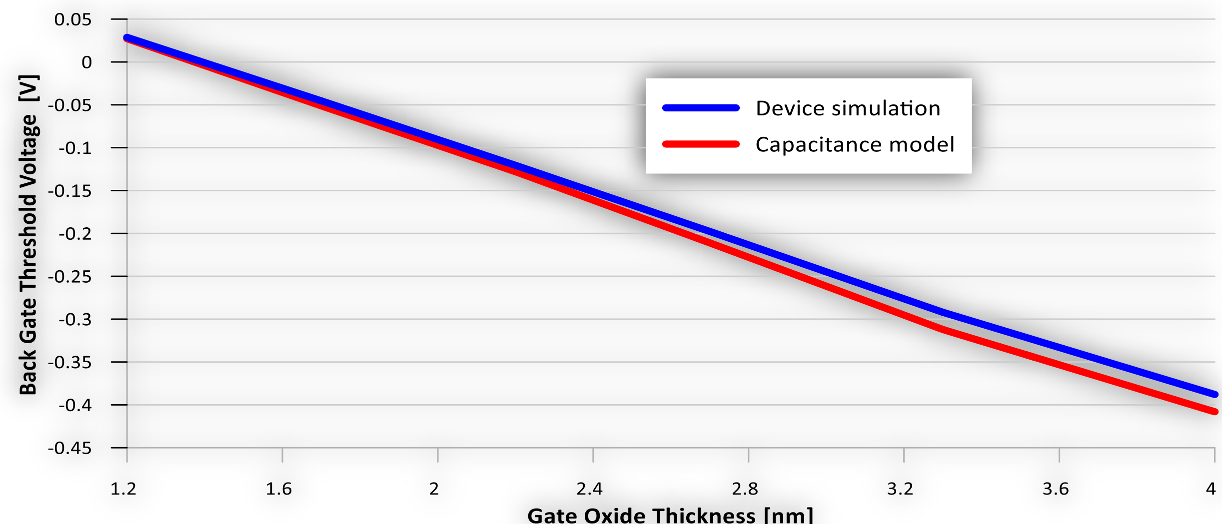


Fig. 4. Back-gate threshold voltage versus gate oxide thickness ($t_{BI}$ =20 nm, $N_{channel}$=$10^{15}$ $cm^{-3}$, $N_{Asub}$=$10^{15}$ $cm^{-3}$, $t_D$=20 nm, $N_{S-D}$=$10^{20}$ $cm^{-3}$, d=43 nm, $V_{DS}$=0 V, T=300 K).

Fig. 5 depicts the simulation diagram and the threshold voltage model of the front-gate in relation to the thickness changes of the silicon layer under the gate in the range of 5 to 9 nm. In this diagram, the extracted model follows the simulation results with a relatively consistent approximation (about 22 mV).

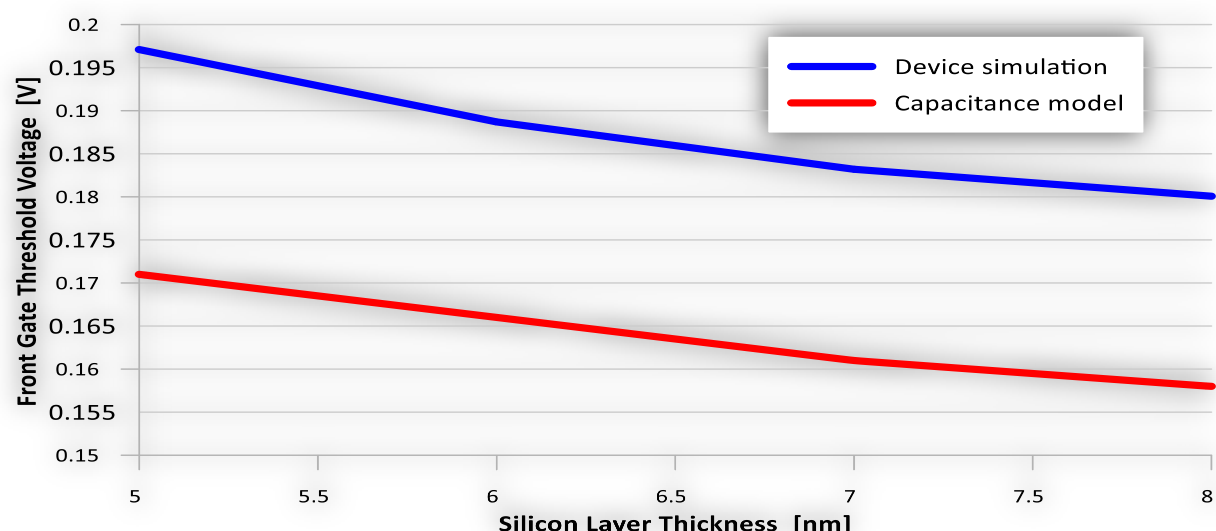


Fig. 5. Front-gate threshold voltage versus silicon film thickness ($t_{BI}$ =20 nm, $N_{channel}$=$10^{15}$ $cm^{-3}$, $N_{Asub}$=$10^{15}$ $cm^{-3}$, $t_D$=20 nm, $N_{S-D}$=$10^{20}$ $cm^{-3}$, d=43 nm, $V_{DS}$=0 V, T=300 K).

Fig. 6 depicts the simulation diagram and model of the back-gate threshold voltage in relation to the changes in the silicon layer thickness ($t_{si}$). As shown, with the increase of silicon thickness, the decreasing trend of both computed values follows each other with a close approximation.

The strong dependency of the front- and back-gate threshold voltage on the silicon film thickness, depicts the role of silicon-film surface-roughness on the threshold voltages of the

device. Obviously, precise control of the silicon-film thickness and/or methods to control the threshold voltage are required. This is done through the gate-stack work-function engineering. In DI UTBB SOD MOSEFT, an additional option as second insulating layer length is provided to well-tune the threshold voltage.

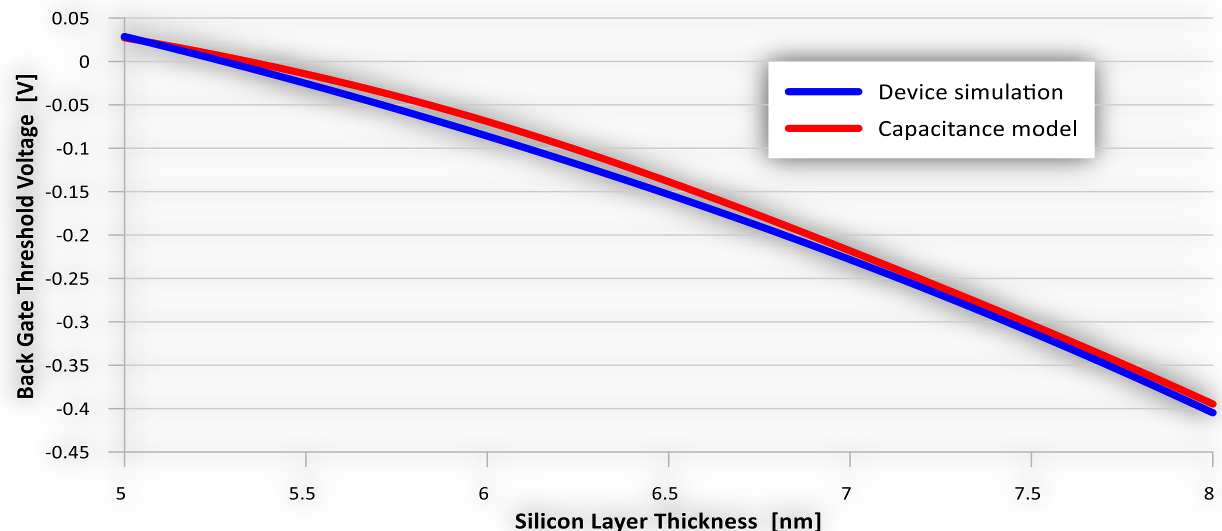


Fig. 6. Back-gate threshold voltage versus silicon film thickness ($t_{BI}$ =20 nm, $N_{channel}$=$10^{15}$ cm$^{-3}$, $N_{Asub}$=$10^{15}$ cm$^{-3}$, $t_D$=20 nm, $N_{S-D}$=$10^{20}$ cm$^{-3}$, d=43 nm, $V_{DS}$=0 V, T=300 K).

Figs. 7 and 8 are the results of the simulation and the threshold voltage model for the front- and back-gate in relation to the variations in the thickness of the buried dioxide layer, respectively. It can be seen from Fig. 7 that reducing the thickness of the second insulating layer in the range of 15 to 40 nm does not have significant changes in the threshold voltage of the front-gate. Also, the difference between the results of the extracted model and the simulation is a relatively constant value and is close to 25 mV.

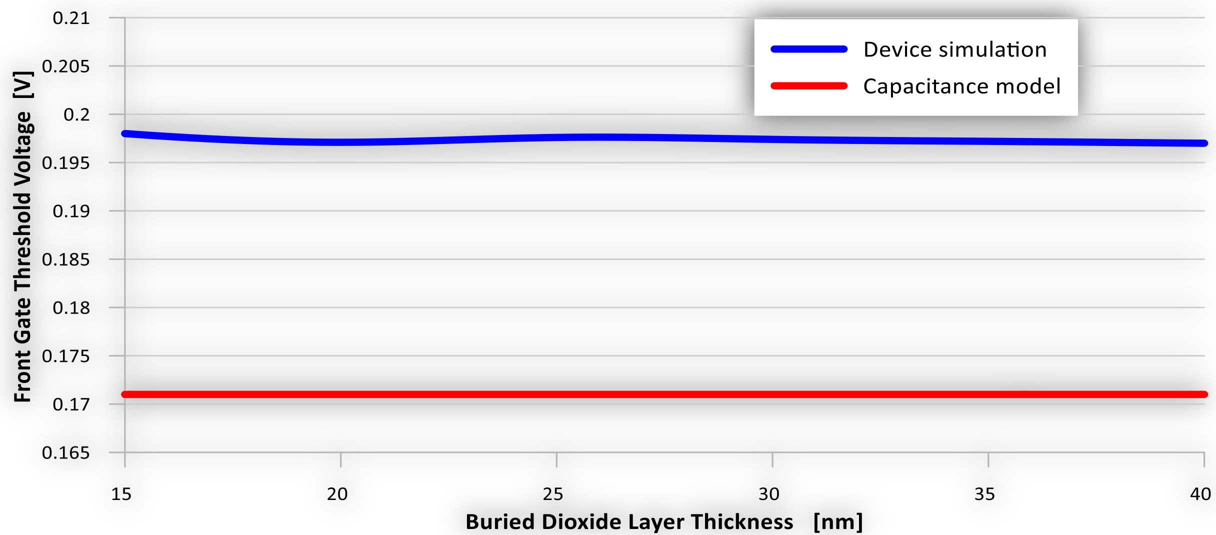


Fig. 7. Front-gate threshold voltage versus thickness of the buried dioxide layer ($t_{si}$ =5 nm, $N_{channel}$=$10^{15}$ cm$^{-3}$, $N_{Asub}$=$10^{15}$ cm$^{-3}$, $t_D$=20 nm, $N_{S-D}$=$10^{20}$ cm$^{-3}$, d=43 nm, $V_{DS}$=0 V, T=300 K).

It can be seen in Fig. 8 that the values calculated in the extracted model for the back-gate threshold voltage with an error of about 3 mV to 5 mV follow the simulation results.

The smaller dependency of the front- and back-gate threshold voltage on the second insulating layer thickness, lifts-up inflexible requirement on the layer thickness. It, therefore, is deposited on the diamond layer for the diamond layer surface roughness reduction. The second insulating layer thickness is greater than the root mean square diamond layer surface roughness. Thus, a chemical mechanical polishing can be used to have a smooth $SiO_2$ surface.

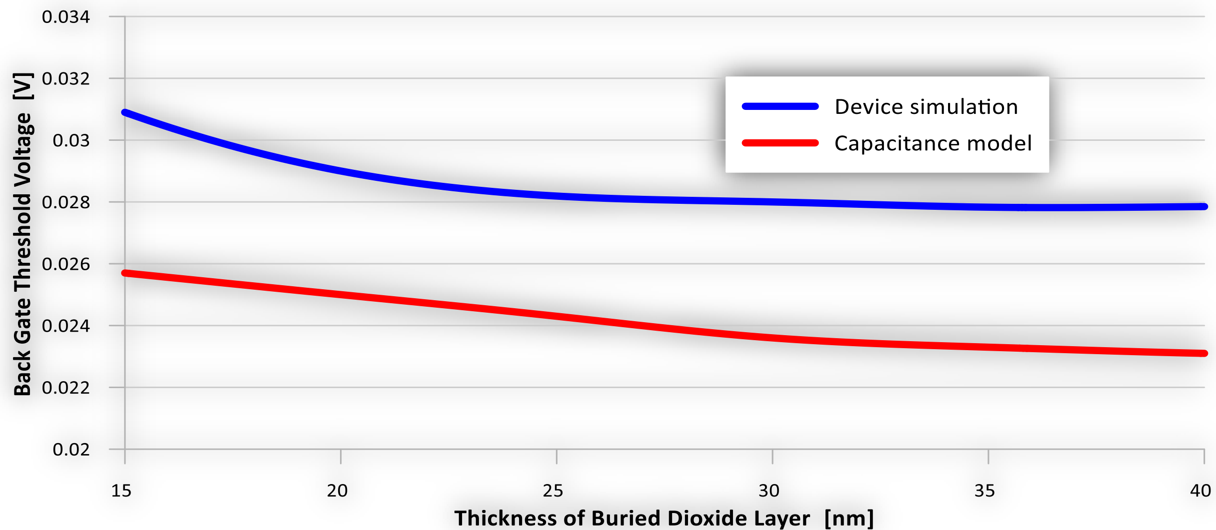


Fig. 8. Back-gate threshold voltage versus thickness of the buried dioxide layer ($t_{si}$ =5 nm, $N_{channel}$=$10^{15}$ $cm^{-3}$, $N_{Asub}$=$10^{15}$ $cm^{-3}$, $t_D$=20 nm, $N_{S\text{-}D}$=$10^{20}$ $cm^{-3}$, d=43 nm, $V_{DS}$=0 V, T=300 K).

Fig. 9 depicts the graph of the front-gate threshold voltage in relation to the increase in the thickness of the buried diamond layer in the range of 20 nm to 40 nm. It can be seen that the derived model of the threshold voltage of the front-gate is almost unvaried, but in the simulation, this value is reduced by 3 mV. The difference between these two graphs in the thickness range of 20 nm to 40 nm is relatively constant and equal to 2.5 mV.

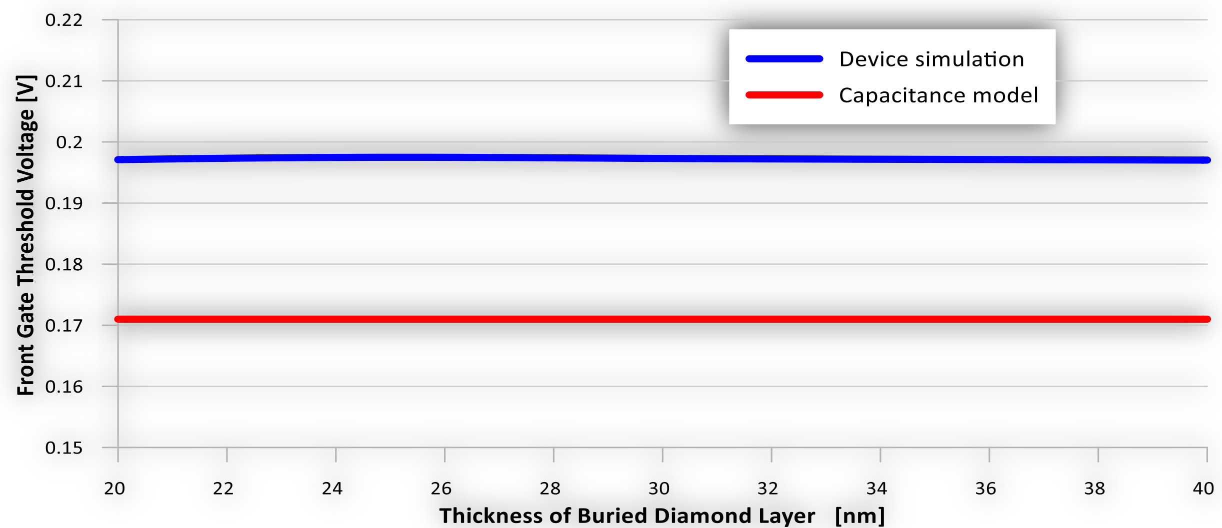


Fig. 9. Front-gate threshold voltage versus thickness of the buried diamond layer ($t_{BI}$ = 20 nm, $N_{channel}$=$10^{15}$ $cm^{-3}$, $N_{Asub}$=$10^{15}$ $cm^{-3}$, $t_{si}$ =5 nm, $N_{S\text{-}D}$=$10^{20}$ $cm^{-3}$, d=43 nm, $V_{DS}$=0 V, T=300 K).

In Fig. 10, the back-gate threshold voltage is depicted in a 20 nm to 40 nm thickness range of the diamond layer. It can be seen that as the thickness of the diamond layer increases,

the difference between the two threshold voltages obtained from the simulation and the model decreases. This difference is equal to 5 mV at the thickness of 20 nm and 2 mV at the thickness of 40 nm.

The small dependency of the front- and back-gate threshold voltage on the diamond layer thickness, allows incorporating thick diamond layer. Thermal conductivity of the diamond layer decreases as the diamond layer thickness reduces. The excellent thermal conductivity of the bulk diamond significantly lowered at thin thicknesses. Therefore, in DI SOD MOSFET, a thick diamond layer can be incorporated to maintain the heat spreading mechanism of the SOD substrate.

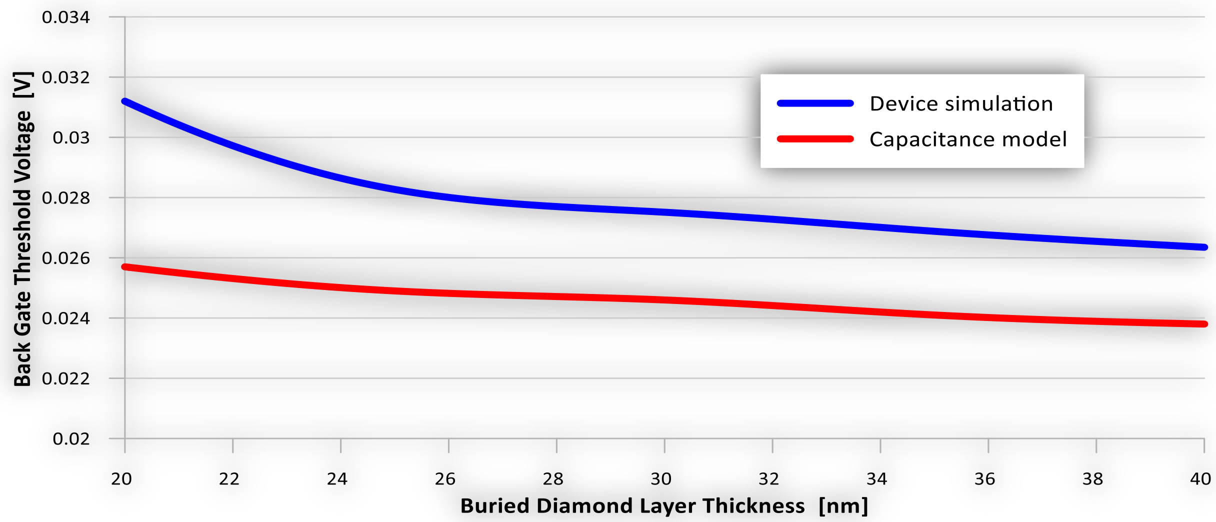


Fig. 10. Back-gate threshold voltage versus thickness of the buried diamond layer ($t_{BI}$ =20 nm, $N_{channel}$=$10^{15}$ $cm^{-3}$, $N_{Asub}$=$10^{15}$ $cm^{-3}$, $t_{si}$ =5 nm, $N_{S-D}$=$10^{20}$ $cm^{-3}$, d=43 nm, $V_{DS}$=0 V, T=300 K).

Fig. 11 illustrates the front-gate threshold voltage where the source/drain overlap with the second insulating layer length is varied from 5 nm to 43 nm. A change of more than 0.02 V in front-gate threshold voltage is observed. This dependency is important to the fabrication procedure involved in the device-threshold-voltage-adjust process.

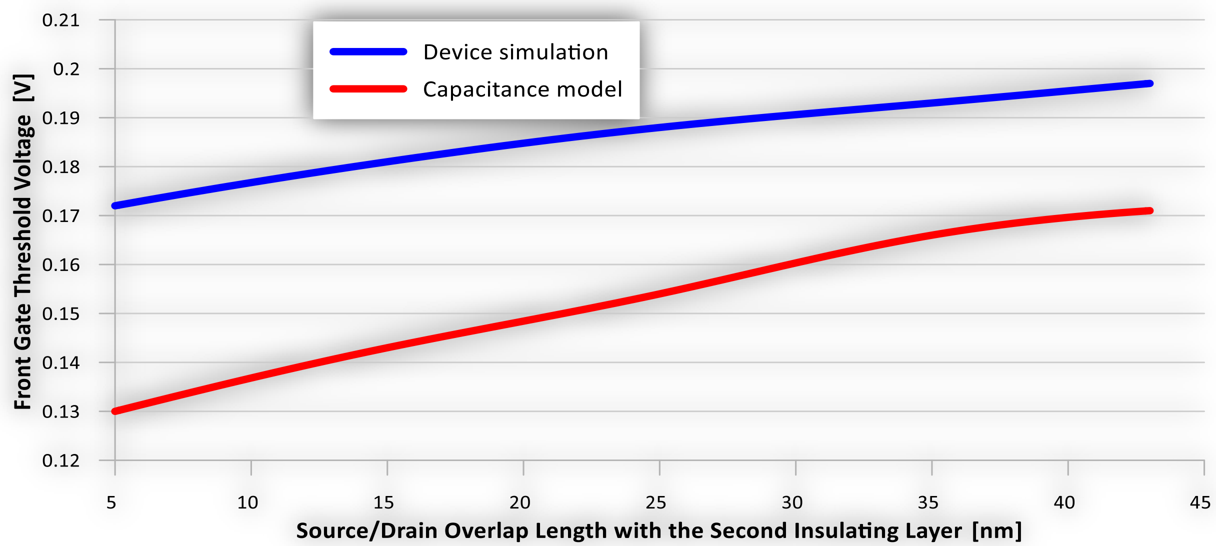


Fig. 11. Front-gate threshold voltage versus the source/drain overlap length with the second insulating layer ($t_{BI}$ =20 nm, $N_{channel}$=$10^{15}$ $cm^{-3}$, $N_{Asub}$=$10^{15}$ $cm^{-3}$, $t_{si}$ =5 nm, $N_{S-D}$=$10^{20}$ $cm^{-3}$, d=43 nm, $V_{DS}$=0 V, T=300 K, $t_D$=20 nm).

In addition, Fig. 12 shows the back-gate threshold voltage when source/drain overlap length with the second insulating layer is varied from 5 nm to 43 nm. As it can be seen, the trend of the graph is upward with increasing source/drain overlap length. A difference between the model findings and simulation results of less than 0.005 V is shown at this range.

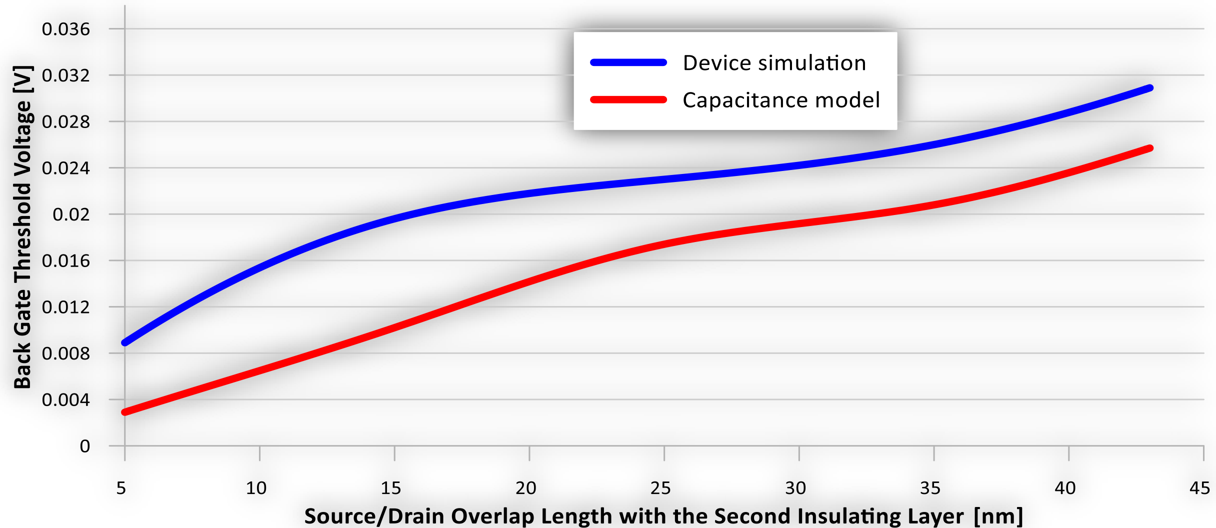


Fig. 12. Back-gate threshold voltage versus the source/drain overlap length with the second insulating layer ($t_{BI}$ =20 nm, $N_{channel}$=$10^{15}$ $cm^{-3}$, $N_{Asub}$=$10^{15}$ $cm^{-3}$, $t_{si}$ =5 nm, $N_{S\text{-}D}$=$10^{20}$ $cm^{-3}$, d=43 nm, $V_{DS}$=0 V, T=300 K, $t_D$=20 nm).

## 4. CONCLUSIONS

In this article, an advanced circuit model for DI UTBB SOD MOSFET is obtained. To show the accuracy of the model, the front- and back-gate threshold voltages calculated by the node matrix equations were compared with those of the device simulation results in various device parameters, and the findings were found to be promising. The model provides physical insight on the device threshold voltage dependency with the critical structure dimensions. The device fabrication procedure must be sensitive to the drain/source overlap length with the second insulating layer. This parameter can be used for DI UTBB SOD MOSFET threshold voltage tuning in addition to the adjustment applied by gate work-function engineering.

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