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Optimal Integration of PV-Based Distributed Generators and Shunt Capacitors for 69 Bus System using Imperialist Competitive Algorithm and ETAP Software

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Abstract – Optimal deployment of photovoltaic-based distributed generators (PVDG) and shunt capacitor units is a perilous task in modern power system planning. This work presents an effective Imperialist Competitive Algorithm (ICA) based on social political process for selecting the best locations and sizes for PVDGs and shunt capacitor units. Three different load patterns, i.e., nominal, decremented and incremented are taken into account while installing PVDG and shunt capacitor units in the typical radial distribution systems of 69-bus. The primary objective of this work is to reduce active power losses and to significantly improve the voltage pattern after positioning of PVDG and capacitor units. The results show that the losses are reduced significantly by integrating the PVDG and capacitor units simultaneously at the optimum position in the test system. Furthermore, results of simulating the 69 bus system (with the integrated PVDG and capacitors) prove to be promising and authentic.

Keywords - Imperialist competitive algorithm; ETAP software; Photovoltaic-based distributed generators.

1. INTRODUCTION

Over the years, Distribution Systems (DS) underwent a number of changes. Due to the increasing demand, regulatory bodies mandate that utilities' services exhibit an ever-higher level of reliability and a high quality standard [1]. The integrated power system's distribution system is the last step in supplying electricity to large loads including commercial, industrial, and residential buildings [2]. In recent decades, raising distribution system performance is a key issue because of variable characteristic of load, high R/X ratio, employing renewable energy sources and accelerated distribution of electrical loads. Approximately 50% of all power system losses and low voltage profile are attributed to the distribution system [3].

Installing distributed generations (DGs) and shunt capacitors on system buses to inject additional active and reactive powers might ease these difficulties and produce technical and financial advantages. Consequently, the ideal positioning of DGs and capacitors can be framed as a restricted optimization problem [2].

On the basis of nature of power supply, the DGs are classified into four different categories [2].

- a) Injection of active power (Category 1)
- b) Injection of reactive power only (Category 2)

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- c) Injection of both active and reactive power (Category 3)
- d) Injection of active and consumption of reactive power (Category 4)

In a power system, distributed energy resources must be planned as efficiently as possible [4].

Due to the computational complexity of these resources, their siting and sizing have spurred a lot of research over the past 20 years [5, 6].

Metaheuristics and bio-inspired algorithms are two widely utilised AI strategies that can address issues with a high combinatorial character. Furthermore, because random parameters are used in the recombination and selection of the candidate solutions, Evolutionary Algorithms (EA) have a strong probabilistic aspect [5].

Heuristic and bio-inspired approaches have recently been widely adopted by authors. DS optimization uses a variety of algorithms, which are documented in the literature: Genetic Algorithm and cuckoo optimization algorithm [7], Particle Swarm Optimization (PSO) [8–10], Genetic Algorithm [11–14], Improved Whale Optimization methodology [15], Grey Wolf [16], Water Cycle Algorithm [17], Social Media Optimization (SMO) [18], Ant Lion Optimizer (ALO) [19], and Some of the mentioned articles will be emphasized since they are more closely related to the theme put out in the present work. Furthermore, author in [20] considered HOMER PRO for solving sizing problem of PV system for a specified location.

In order to allocate DGs in a way that minimizes active losses and achieves voltage regulation, a new PSO approach was developed in [8]. The technique combines PSO and GA in the same population to benefit from both algorithms' advantages. To boost voltage security in DS, researchers in [18] use GA and SMO to determine the ideal placements and sizes for DGs. The same weaknesses identified in [8] are present in this work, which does not address the initial population. In order to discover the best positioning and DG size for reducing the overall actual power loss in an active distribution network (ADN) with many soft open points (SOPs), authors in [21] employed a generalized methodology based on PSO but just one OF was taken into consideration.

The swarm moth flame optimization algorithm (SMFO) was used in [22] to identify the best placement and size of DGs in radial distribution networks while taking into account integrated power losses, voltage profile, and pollution emission. But, just one kind of DGs was taken into account.

In addition to Voltage Regulators, DG units and Capacitors are allocated in [16] using an upgraded GWO. Minimizing losses and energy acquisition costs was the key goal. Again, only three load variations were applied, and large-scale systems were not used to test the methods.

Utilizing PSO, various DG types were used to address the placement issue in the distribution system [23].

The literature exhibits various analytical and hybrid approaches to solve the allocation and sizing problem. Fuzzy logic is an effective method to manage the DGs' reactive power [24]. A gradient is used to optimize the fuzzy system descent algorithm. A blend of GA and fuzzy is applied to optimize different parameters of DG coetaneously [25]. A proficient hybrid approach is applied in solving multi objective parameters under changing loading conditions. The 38 bus network is opted to evaluate the performance of the approach in [26]. Authors in [27] have projected a composite technique (PSO and analytical) for positioning of multiple DGs. This technique is tested on conventional IEEE 33 and 69 node networks.

In a big power system network, congestion management is a significant issue that can be resolved by employing a hybrid strategy with the suitable placement of DGs. The differential evaluation and firefly approach were implemented as hybrid technique in [28].

From the literature review, it can be concluded that:

- a) Metaheuristic techniques are more popular in solving complex nature problem of allocating DG units. The health of these algorithms is better in comparison to analytical based techniques.
- b) The results of algorithms are not compared with the results obtained from simulation platform, as simulation platform considers numerous real time parameters while integrating compensation units in tested topology.
- c) Very few papers have tested their applied techniques on different scenarios. All aforesaid critical reviews are considered and implemented in this paper.

1.1. Our Contribution

This paper exhibits application of Imperialist Competitive algorithm; a social political process based metaheuristic technique, to identify the globally optimal solution to the nonconvex, discrete DG and capacitor allocation issue. The major contributions of this work are: Integration of PVDG and shunt capacitor units at three different load patterns, evaluating the health of algorithm by portraying the convergence characteristics and simulation of test system on ETAP. The IEEE 69 bus system is chosen for testing the effectiveness of ICA.

1.2. Organization of Paper

Section 2 contains the optimization problem's mathematical formulation, objective function and constraints. The ICA is described in section 3. Details of test system chosen along with scenarios taken into consideration are provided in section 4. Section 5 discusses the results obtained through ICA. Section 6 exhibits simulation results of ETAP. The conclusive statement of the paper is presented in section 7.

2. PROBLEM FORMULATION

An illustration of single line diagram of the distribution network is shown in Fig. 1. The set of iterative equations used to calculate power flows are:

$$P_{loadi+1} = P_i - P_{loadi+1} - R_{I,I+1} * \left(\frac{P_{I,I+1}^2 + Q_{I,I+1}^2}{|V_I^2|}\right)$$
(1)

$$Q_{loadi+1} = Q_i - Q_{loadi+1} - X_{I,I+1} * \left(\frac{P_{I,I+1}^2 + Q_{I,I+1}^2}{|V_I^2|}\right)$$
(2)

$$\left|V_{I+1}^{2}\right| = \left|V_{I}^{2}\right| - 2*\left(R_{I,I+1}*P_{I} + X_{I,I+1}*Q_{I}\right) + \left(R_{I,I+1}^{2} + X_{I,I+1}^{2}\right)*\left(\frac{P_{I,I+1}^{2} + Q_{I,I+1}^{2}}{\left|V_{I}^{2}\right|}\right)$$
(3)

where P_{I, I+1}: Real power flowing between line segment I and I+1;

Q_{I, I+1:} The flow of reactive power between line segment I and I+1;

P_{laodI}: Active load at bus I;

Q_{laodI}:Reactive load at bus I;

R_{I,I+1} :Resistance between line segment I and I+1;

X_{I, I+1}:Reactance between line segment I and I+1;

The primary issue is determining the most suitable location and configuration for PVDG and shunt capacitor units in the distribution network. Allocating compensation units is a nonlinear combinatorial optimization problem with a goal of reducing losses and improving voltage.



Fig. 1. Single line diagram of radial distribution system.

The real power loss and reactive power loss between line sections 1 and 1+1 are represented in Eqs. (4) and (5), respectively.

$$P_{I,I+1}^{Loss} = \frac{P_{I,I+1}^2 + Q_{I,I+1}^2}{\left|V_I^2\right|} R_{I,I+1}$$
(4)

$$Q_{I,I+1}^{Loss} = \frac{P_{I,I+1}^2 + Q_{I,I+1}^2}{\left|V_I^2\right|} X_{I,I+1}$$
(5)

The primary objective is to lower line losses by installing DG units in the ideal position and with the suitable dimensions. The objective function is given by:

$$MinimiseP^{TotalLoss} = \sum_{I=1}^{N_{BR}} \frac{P_{I,I+1}^2 + Q_{I,I+1}^2}{\left|V_I^2\right|} R_{I,I+1}$$
(6)

By placing a constant multiplier with active and reactive power injection and allocating a unit to the l+1 bus, Eq. (6) can be changed. The equation is represented as:

$$P_{DG}^{TotalLoss} = \sum_{I=1}^{N_{BR}} \frac{(P_{I,I+1} - \lambda_{DG} P_{DG,I+1})^2 + (Q_{I,I+1} - \lambda_{DG} Q_{DG,I+1})^2}{|V_I|^2} R_{I,I+1}$$
(7)

Constraints:

To achieve the goal of minimizing power loss, a number of equality and inequality criterias must be satisfied. The criteria are listed below:

1. Variations in nodal voltage shall not exceed the tolerance level. The tolerance limit is set at +/- 10% of the rated voltage.

$$V_{\min} \le V_I \le V_{\max} \tag{8}$$

2. The power balance equation must be satisfied.

$$P_{G,I} - P_{D,I} = \sum_{n=1}^{n} V_{I} V_{I+1} \Big[G_{I,I+1} \cos(\delta_{I-} \delta_{I+1}) + B_{I,I+1} \sin(\delta_{I-} \delta_{I+1}) \Big]$$
(9)

$$Q_{G,I} - Q_{D,I} = \sum_{n=1}^{\eta} V_I V_{I+1} \Big[G_{I,I+1} \sin(\delta_{I-} \delta_{I+1}) - B_{I,I+1} \cos(\delta_{I-} \delta_{I+1}) \Big]$$
(10)

$$P_{injection} = P_{G,I} - P_{D,I} \tag{11}$$

$$Q_{injection} = Q_{G,I} - Q_{D,I} \tag{12}$$

3. Each line's apparent power flow must be lower than its maximum power flow limit.

$$\left|S_{apparent}\right| \le \left|S_{apparent}^{\max}\right| \tag{13}$$

4. The Capacitor's size must fall within the permitted range.

$$Size_{capacitor,\min} \le Size_{capacitor} \le Size_{capacitor,\max}$$
 (14)

5. The PVDG size must fall within the permitted range.

$$Size_{DG,\min} \leq Size_{DG} \leq Size_{DG,\max}$$
 (15)

3. IMPERIALIST COMPETITIVE ALGORITHM

Gargari and Lucas were the first to introduce ICA, which was motivated by the socio political process of imperialist competition [29]. Analogous to other evolutionary algorithms, the suggested ICA method takes into account an initial population of countries. The best countries are chosen to be imperialists. These imperialists establish colonies among the remaining people. According to imperialist strength, all the colonies from the generated beginning population are distributed among the imperialists. The steps involved in the process are as follows:

3.1. Generation of Initial Empires

The countries are initialized at the commencement of the process. The position of the nth countries in an M-dimensional optimization problem is described as:

 $Country_n = [population_n^1, population_n^2, population_n^3, \dots, population_n^m]$

where m is the total number of countries.

The nth country cost is represented by $Cost_n$ as:

 $Cost_n = f(Country_n) = f(population_n^1, population_n^2, population_n^3, population_n^m)$ The empire initialization process is depicted in Fig. 2.



Fig. 2. Initialization of empires.

3.2. Colonies Movement towards Imperialist

The colonies movement is depicted in Fig. 3, where the colony begins to migrate by x unit in the direction of the appropriate imperialist. A vector represents the colony's movement in the imperialist direction. Fig. 3(a) depicts the procedure for changing the position between an imperialist and a colony. The new position of the colony is exhibited red color.



3.3. Interchanging the Position of Colony and Imperialist

It is conceivable for a colony to obtain a position at a low-cost than the imperialist during the march of colonies in the imperialist direction. The imperialist and colony positions were switched for a better one. Fig. 4(a) depicts the procedure for changing the position between an imperialist and a colony. Red color represents the empire's best colony. Due to its reduced cost value when compared to that imperialist, this colony was regarded as the best colony. The updated empire is shown in Fig. 4(b) following the best colony and imperialist position exchange.



a. Exchange process Fig. 4. Exchange process between colony and imperialist.

3.4. Computation of Total Power of Empire

The sum of power of imperialist and colonies comprises total power of the empire. The contribution of colonies to total power is quite small as compared to the power of the imperialists.

 $TOC_m = \text{cost of } m^{\text{th}} \text{ empire} + \xi * \text{mean}(\text{cost of } m^{\text{th}}\text{colony})$

The value of ξ is taken as less than 1. The cumulative power of the empire depends upon ξ . TOC_m is the absolute cost of the mth empire.

3.5. Imperialist Competition

With the commencement of Imperialist competition, powerful empire will take possession of the feeble colonies of the feeblest empire. By seizing control of these colonies, imperialistic rivalry eventually boosts the power of a strong empire and weakens the might of the feeblest one. Imperialist competition is portrayed in Fig. 5.



Fig. 5. Portrayal of imperialist competition.

Each empire's likelihood of possession is initially determined based on its level of power. The normalized cost is evaluated as:

 $NTC_m = TOC_m - \max(TC_n)$

 NTC_m : Normalized cost (mth) empire

 TOC_m : Absolute cost (mth) empire.

3.6. Excluding the Empire Having Less Power

In an imperialist competition, the empires with the least amount of power will be removed, and the colonies from these empires will be given to other empires. According to this process, an empire is eliminated if it either loses all of its colonies or doesn't have any at all. The flowchart for allocation of PVDG and shunt capacitors using ICA is depicted in Fig. 6.



Fig. 6. Flowchart of ICA for allocation of PVDG and shunt capacitor.

4. TEST SYSTEM

A well-known, conventional IEEE 69 bus system is taken as test system in evaluating the effectiveness of Imperialist Competitive Algorithm. The system operates on 12.66 kV. System's line data and load data is fetched from [30]. The system load of 69 bus system accounts for 3802 kW (active power load) and 2694 kVAr (reactive power load). Under

nominal load pattern without compensation, real power losses accounts for 225 kW and reactive power losses for 102 kVAr. The system minimum voltage is observed as 0.9092 pu. Single line layout of 69 bus radial network is shown in Fig. 7.



4.1. Scenario Considered

Three scenarios are considered. Under each scenario, three instances – the nominal load pattern, decremented load pattern (50% of the nominal load) and incremented load pattern (150% of the nominal load) have been taken into account. The details are as follows:

A. Scenario 1: Positioning of PVDG unit only

- 1. Nominal Load Pattern
- 2. Decremented Load Pattern
- 3. Incremented Load Pattern
- B. Scenario 2: Positioning of Shunt Capacitor unit only
 - 1. Nominal Load Pattern
 - 2. Decremented Load Pattern
 - 3. Incremented Load Pattern
- C. Scenario 3: Positioning of PVDG and Shunt Capacitor
 - 1. Nominal Load Pattern

- 2. Decremented Load Pattern
- 3. Incremented Load Pattern

The types of distributed generation units taken into consideration for injecting active and reactive power into the network are as follows:

Type 1: DG injects only active power into the distribution network while operating at unity power factor (p.f.).

Type 2: Capacitor supplying reactive power into the distribution network.

5. **RESULTS OF ICA**

ICA has been applied on conventional IEEE 69 bus system. The ICA parameters considered for solving placement and sizing problem of PVDG and capacitor for the opted test system are listed in Table 1.

Table 1. ICA parameters for the 69 bus system.	
Parameter	Value
NPar (dimension of the optimization problem)	6
NDG (number of compensation units)	2
Nbus (number of buses)	69
Number of countries	100
Number of initial imperialists	10
Number of decades	300
Revolution rate	0.9
Assimilation coefficient	2
Assimilation angle coefficient	0.5
Zeta	0.02
Damp ratio	0.99
Uniting threshold	0.02

Scenario 1: Results of PVDG placement are shown in Table 2. Parameters such as losses (active and reactive), size and position of PVDG, loss reduction percentage are exhibited in result section. Before placement of PVDG unit in nominal load pattern, the losses account for 224.6 kW (active power loss) and 102 kVAr (reactive power loss). The active power losses reduced to 76.6 kW, 19.6 kW and 165.1 kW from 224.6 kW, 51.5 kW and 560.4 kW for nominal, decremented and incremented load pattern. The ICA gives optimal location for positioning of PVDG at 61 and 16 with size of 1500 kW and 350 kW, respectively. A spurt reduction of 65.89% in power losses is observed at nominal load pattern. Furthermore, an outstanding improvement in voltage can be observed in Table 2, the voltage is increased from 0.9092 pu to 0.9680 pu in nominal load pattern.

The comparison of ICA results for Scenario 1 is exhibited in Table 3. It can be observed in the table that ICA outperformed other hybrid and analytical techniques in finding best position and size of PVDG. The size of PVDG identified by ICA is quite less as compared with other techniques. Although other methods giving slight more loss reduction than ICA but the size of PVDG is quite less in case of ICA. Fig. 8 depicts a graphical representation of the sizes of PVDG identified by various algorithms.

Table 2. Results of 69 bus system (Scenario 1).							
Parameter	Nominal load nattern		Decremented load		Incremented load		
	i voiminui i	oud puttern	pat	pattern		tern	
i arameter	Before	After	Before	After	Before	After	
	PVDG	PVDG	PVDG	PVDG	PVDG	PVDG	
Active Power Losses [kW]	224.6	76.6	51.5	19.6	560.4	165.1	
Reactive Power Losses	102	38.4	23 5	07	253	87.6	
[kVAr]	102	36.4	23.5	9.1		82.0	
BVDC size [kW] (Bus No.)		1500(61)		700(61)		2600(61)	
		350 (16)		200(16)		850 (16)	
Total PVDG Size [kW]		1850		900		2450	
Minimum Voltage [pu]	0.9092	0.9680	0.9566	0.9876	0.8693	0.96512	
(Bus No)	(65)	(65)	(65)	(65)	(65)	(65)	
Active power Loss	(E 90		61.04			70 53	
Reduction percentage		65.89		01.74		70.55	
Reactive power loss		(0.25		58 73		67 35	
reduction percentage	62.33		56.72			07.00	

Table 3. Comparison of results of ICA (Scenario 1).							
Technique	Size of DG Size of DG [kW/Location] [Kw]	Size of DG	Results Obtained				
		[Kw]	Active power	Reactive power loss	V7		
			loss [kW]	[kVAr]	V min		
ICA	1500(61), 350 (16)	1850	76.6	38.4	0.968		
ILFSA [30]	530(17), 1770(61)	2300	73	37	0.9714		
HGWO [31]	531(17), 1781(61)	2312	73	37	0.9715		
HHO [32]	532(17), 1780(61)	2312	73	37	0.9715		
TLBO [32]	531(17),1781(61)	2313	73	37	0.9715		
KHA [33]	972(51),1726(61)	2699	80	39	0.9711		



Fig. 8. PVDG size by various techniques.

Scenario 2: Table 4 shows the results of shunt capacitors only for three different load patterns. The positioning of capacitor at optimum location and optimum size (bus no 61 (1040 kVAr) and 16 (300 kVAr)) identified by ICA exhibits a considerable reduction in power losses from 224.6 kW to 148.72 kW. At nominal load pattern, reduction of 33.78% and 32% is

noted in active and reactive power losses. The size of 665 kVAr (Bus no 61 (500 kVAr) and Bus no 16 (165 kVAr)) is identified by ICA for placement of capacitors in decremented load pattern, which reduces the power losses by 32.8% and increases the minimum voltage profile from 0.956 pu to 0.9628 pu at bus no 65. Analogously in incremented load pattern, the size of 1800 kVAr (Bus no 61 (1500 kVAr) and Bus no 16 (300 kVAr)) is identified by ICA for placement of capacitors in decremented load pattern, which reduces the power losses significantly by 37.36% and increases the minimum voltage profile from 0.869 pu to 0.8859 pu at bus no 65. Furthermore, decline in reactive power losses is also seen at all load patterns in Table 4.

Table 4. Results of 69 bus system (shunt capacitor placement (SCP)).							
	Nominal load		Decremented load		Incremented load		
Parameter	pat	pattern		tern	pattern		
i uluitetei	Before	After	Before	After	Before	After	
	SCP	SCP	SCP	SCP	SCP	SCP	
Active Power Losses [kW]	224.6	148.72	51.5	34.6	560.4	351	
Reactive Power Losses	102	102 69.36	23.5	16.1	253	167 60	
[kVAr]	102		25.5	10.1		102.09	
Capacitor size [kVAr] (Bus		1040(61)		500(61)		1500(61)	
No.)		300 (16)		165 (16)		300(16)	
Total Capacitor Size [kVAr]		1340		665		1800	
Minimum Voltage [pu] (Bus	0.9092	0.9220	0.9566	0.9628	0.8693	0.8859	
No)	(65)	(65)	(65)	(65)	(65)	(65)	
Active power Loss Reduction	22.78		32.8			37 36	
percentage		55.70		52.0		57.50	
Reactive power loss		32		31.48		35 69	
reduction percentage		32		51.40		55.07	

The comparison of results for Scenario 2 is shown in Table 5. The capacitor size identified by ICA is smaller in size (1340 kVAr) for same percentage of loss reduction as compared to other techniques mentioned in table. Latest techniques such as ILFSA, HHO, TLBO, and HGWO are compared with ICA in terms of losses (active and reactive) and minimum voltage. Fig. 9 depicts a graphical representation of the sizes of capacitors identified by various algorithms.

Table 5. Comparison of results of ICA (Scenario 2).

	Size of	Size of Size of DG		Results Obtained			
Technique	DG(kVAr)/Location	[kVAr]	Active power	Reactive power	17		
		[· · ·]	loss [kW]	loss [kVAr]	V min		
ICA	1040(61), 300 (16)	1340	148.72	69.36	0.922		
ILFSA [30]	330(17),1220(61)	1550	148	69	0.9277		
HHO [32]	353(17),1280(61)	1633	148	69	0.9285		
TLBO [32]	360(17),1274(61)	1634	148	69	0.9285		
HGWO [31]	364(17),1227(61)	1641	148	69	0.9285		



Fig. 9. Capacitors' sizes identified by various techniques.

Scenario 3: The outcome of simultaneous placement of PVDG and SC is presented in Table 6. After positioning PVDG of 1850 kW and shunt capacitor of 1340 kVAr in 69 bus test system under nominal load pattern, the losses reduced to 12.6 kW from 224.6 kW, which accounts a declination of 94.39% in active power losses. The voltage profile is also raised to 0.9227 from 0.9092 pu after integration of PVDG and SC in system. Additionally, in case of decremented and incremented load pattern the losses (active) are scaled down to 3.5 kW and 24.2 kW from 51.5 kW and 560.4 kW, respectively. Table 6 clearly indicates that the maximum active power losses reduction percentage is under incremented load pattern. The ICA convergence characteristics for all scenarios are showcased in Fig. 10. The figure clearly indicates that optimum solution is attained in minimum number of iterations. Voltage state at each bus for all scenarios is depicted in Fig. 11.

Table 6. Results of 69 bus system (Scenario 3).								
	Nominal load pattorn		Decreme	nted load	Incremented load			
	Nominaria	voniniai ioad patterni		tern	pat	pattern		
Parameter	Before	After	Before	After	Before	After		
	PVDG &	PVDG &	PVDG &	PVDG &	PVDG &	PVDG &		
	SCP	SCP	SCP	SCP	SCP	SCP		
Active Power	224.6 kW	12.6	51 5	35	560.4	24.2		
Losses	224.0 KW	12.0	51.5	3.5	500.4	24.2		
Reactive Power	102 kVAr	10.7	23.5	2.8	253	21.9		
Losses	102 10111	10.7	20.0	2.0	200	21.9		
DG size (Bus No.)	1500(61)			700(61)		2600(61)		
		350 (16)		200(16)		850 (16)		
Total DG Size		1850		900		2450		
Capacitor size (Bus		1040(61)		500(61)		1500(61)		
No.)		300 (16)		165 (16)		300(16)		
Total Capacitor Size		1340		665		1800		
Minimum Voltage	0.9092	0.9898	0.9566	0.9907	0.8693	0. 9227		
[pu] (Bus No)	(65)	(65)	(65)	(65)	(65)	(65)		
Active power Loss		04 20		02 20		05.68		
Reduction		94.39		93.20		95.08		
Reactive power loss		89 50		88.08	80 00			
reduction		09.00	00.00			71.01		







Fig. 11. Voltage state of 69 bus system for: a) scenario 1; b) scenario 2; c) scenario 3.

6. SIMULATION RESULTS OF ETAP

The 69 bus test system is simulated in ETAP software for analyzing real time solution. The active and reactive power losses are 225 kW and 102 kVAr, respectively. Fig. 12 shows the simulation of test system in ETAP. Table 7 exhibits the results of simulation for all three scenarios taken in account. The sizes of PVDG obtained by ICA for the test system cannot be integrated of similar rating in ETAP because market availability of PVDG of similar size, number of series parallel combination of solar array, rating of each solar panel is the major area of consideration.



Fig. 12. Simulation of 69 bus system in ETAP.

Table 7: Simulation Results of 69 bus system on ETAP							
Parameters	Before Compensation	Scenario 1	Scenario 2	Scenario 3			
Active Power Losses [kW]	225	94	150	28			
Reactive Power Losses [kVAr]	102	46	70	17			
DC size (Bus No.)	_	1496(61)	_	1496(61)			
DG Size (Dus No.)		355 (16)		355 (16)			
Total DG Size [kW]	-	1851	-	1850			
Shupt Capacitor Size [kVAr] (Bus No.)	_	_	1040(61)	1040(61)			
			300 (16)	300 (16)			
Total Capacitor Size [kVAr]	-	-	1340	1340			
Minimum Voltage [pu] (Bus No)	0.9092	0.962	0.930	0.989			
Active power Loss reduction percentage	-	58.22	33.33	87.55			
Reactive power loss reduction percentage		54.9	31.3	83.33			

Table 8 shows the parameter values for solar photo voltaic distribution generation units. A total of 1496 kW (6241 solar module each of 240 watt) is placed at bus no 61 and 355 kW at bus no 16 (1482 solar module each of 240 watt). After placing the PVDG, the losses reduced to 94 kW and voltage of each bus is also enhanced. The system after integration of PVDG is shown in Fig. 13. Under Scenario 2, shunt capacitor of 1040 kVAr at bus no 61 and 300 kVAr at bus no 16 is placed which reduces the losses by 33.33%. Under Scenario 3, both PVDG and capacitor are integrated in the test system resulting a decrement of active power

losses by 87.55%. The system depicting Scenario 1 and 3 is showcased in Figs. 13 and 14.

Table 8. PVDG parameters in ETAP for 69 bus system.						
Parameters	Values					
	PVDG Placement at Bus no 61	PVDG Placement at Bus no 16				
Manufacturer	Suniva	Suniva				
Model	ART245-60-3-1	ART245-60-3-1				
Туре	Mono-crystalline	Mono-crystalline				
Size	240 Watt	240 Watt				
Max Vdc	600	600				
Number in series	79	39				
Number of parallel	79	38				
Total number of panels	6241	1482				
Volt.dc	2421.35	1195.35				
kW.dc	1496	355				
Amp.dc	617.78	297.16				

The comparison of results obtained through ICA and ETAP is showcased in Table 9. It clearly exhibits that loss reduction is slightly more in case of ICA (Scenario 1) in comparison with ETAP, but the credibility of the results obtained through ETAP is quite higher because simulation platform considers various parameters such as type of material, solar irradiance, and time of sunrise and sundown. Efficiency of solar module is also taken into consideration. Furthermore, the model of solar panel used also plays a vital role in results obtained. In this work, Model no: ART245-60-3-1 is used. The programming platform is not considering such parameters; hence, the results obtained through ETAP and ICA differs. The minimum voltage profile is almost similar to obtained one through ICA and ETAP in Scenario 1. In case of Scenario 2, there is marginal difference in loss reduction between ICA and ETAP.



Subsequently, in Scenario 3, the loss reduction noted in ETAP is 87.55% whereas for ICA it is 94.39%. The voltage profile obtained at bus no 65 in ICA and ETAP is similar.

Fig. 13. Integration of PVDG in 69 bus test system using ETAP.



Fig. 14. Integration of PVDG and capacitor in 69 bus test system using ETAP.

	·		0		-			
	Before	Scenario S		Scer	Scenario		Scenario	
Parameters	Compensation	1	1		2		3	
	(ICA & ETAP)	ICA	ETAP	ICA	ETAP	ICA	ETAP	
Active Power Losses [kW]	225	76.6	94	148.72	150	12.6	28	
Reactive Power Losses [kVAr]	102	38.4	46	69.36	70	10.7	17	
DG size (Bus No.)		1500(61)	1496(61)	ΝIΛ	NIA	1500(61)	1496(61)	
	-	350 (16)	355 (16)	1174	NA	350 (16)	355 (16)	
Total DG Size [kW]	-	1850	1851	NA	NA	1850	1851	
Shunt Capacitor Size in				1040(61)	1040(61)	1040(61)	1040(61)	
kVAr (Bus n No.)	-		-	300 (16)	300 (16)	300 (16)	300 (16)	
Total Capacitor Size [kVAr]	-	NA	-	1340	1340	1340	1340	
Minimum Voltage [pu] (Bus	0.0007	0.9680	0.962	0.9220	0.930	0.9898	0.989	
No)	0.9092	(65)	(65)	(65)	(65)	(65)	(65)	
Active power Loss reduction	_	65 89	58 22	33 78	33 33	94 39	87 55	
percentage		00.07	50.22	00.70	00.00	74.07	07.00	
Reactive power loss		62.35	54.9	32	31.3	89.50	83.33	
reduction percentage		02.00	0 1.7	02	01.0	07.00	00.00	

Table 9. Comparison of results obtained through ICA and ETAP

7. CONCLUSIONS

The paper presented a metaheuristic social political ICA-based technique for solving nonlinear optimization problem of positioning and sizing of PVDG and shunt capacitors in distribution network for scaling down losses and enhancement in voltage. ICA had proven its efficacy in obtaining optimum solution in minimum number of iteration, significant reduction of losses in smaller DG size, and voltage enhancement of load buses. The methodology was analyzed using three distinct scenarios for obtaining best results. Each scenario was analyzed for discrete load pattern i.e. nominal, decremented and incremented. Furthermore, the test system was simulated in ETAP software. The results of ICA optimization is compared with ETAP results. The results obtained through ETAP platform signify the authenticity of solution under real time domain.

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