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A Real-Time Electronically Tunable All-MOS Universal Biquadratic Voltage-Mode Filter

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***Abstract*—** In this paper, an electronically tunable universal biquadratic voltage-mode filter that is based only on MOS transistors is proposed. Configuration of the proposed filter is simple and there is no need to use component matching. Since the proposed filter contains only MOS transistors, it is very suitable for implementation in system-on-chip (SoC) applications. The cutoff frequency of the lowpass (LP) and highpass (HP) filters as well as the center frequency and the bandwidth of the bandpass (BP) and bandstop (BS) filters can be controlled either in a continuous range or in a discrete manner by means of a digital control word. Besides, the filter type can be changed during the real time by an appropriate code. Operation of all the filtering functions are verified by simulation using the Berkeley predictive-technology models (BPTM) of the 130 nm complementary metal-oxide semiconductor (CMOS) technology with power-supply voltage, V_{DD}, of 1.2 V. The proposed filter is analyzed quantitatively, and the effects of the total-harmonic distortion (THD), noise, process, voltage and temperature (PVT) variations are also investigated. The average power consumption of the LP, HP, BP, BS, and allpass (AP) filters are found to be 30, 118, 74, 118, and 30 (all in μW). The price paid for all these advantages is more sensitivity to process variations for the lowpass filter.

***Keywords*—** Bandwidth; Distortion; Resonant frequency; Sensitivity; Tuning; Universal filter; Voltage mode; CMOS technology.

1. INTRODUCTION

Filters are very important building blocks in several applications including telecommunications, electronic circuits, control systems, analog-signal processing [1], measurements, instrumentations [2], phase-locked loops, touch-tone telephones, high-fidelity loudspeakers [3, 4], to name such a few. Filters that can exhibit several filtering functions using the same circuit topology are aptly called universal or multifunction filters. In order to enhance the filter selectivity, the filter order must be increased. As well known, first-order and second-order filters are the main building blocks in realizing higher-order filters by cascading. Filters with a higher order (three or more) can be realized by cascading first-order and second-order filter cells [5, 6]. Also, cascading is one of the most popular methods for realizing active filters with op-amps. If a passive filter is adopted in realizing first- and second-order stages, each stage can be followed by a noninverting buffer to avoid the loading effect between every two cascaded stages.

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1.1. Basic Filter Types

Although the information in this subsection is well known, it is stated here as it constitutes the foundation of this work. The second-order lowpass filter (LPF) can be obtained by cascading two stages of the first-order lowpass filter as shown in Fig. 1(a). The same concept can be applied also on the highpass filter (HPF) as shown in Fig. 1(b). The bandpass filter (BPF), which is shown in Fig. 1(c), can be obtained by cascading first-order lowpass and first-order highpass filters conditional that the cutoff frequency of the latter is smaller than that of the former. The bandpass response can also be realized by putting the highpass filter and the lowpass filter in the first and second stages, respectively. The bandstop filter (BSF) can be obtained by parallel connecting the first-order lowpass and the first-order highpass filters with the cutoff frequency of the former smaller than that of the latter. The circuit shown in Fig. 1(d) is a realization of this concept; it is the conventional twin-T bandstop filter. Finally, the allpass filter (APF) can be obtained from the circuit shown in Fig. 1(e).

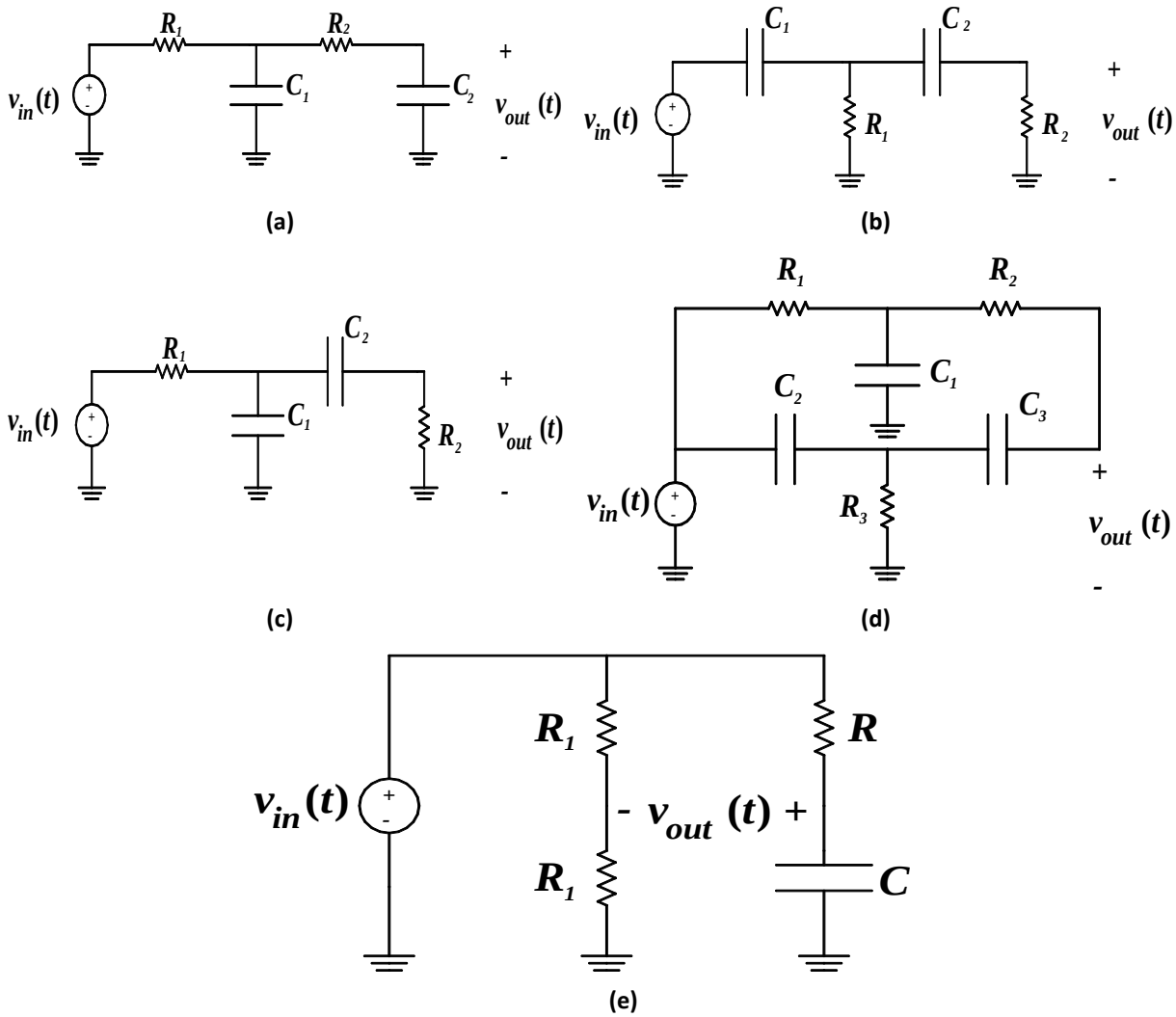

Fig. 1. The circuit schematics of the: a) lowpass filter; b) highpass filter; c) bandpass filter; d) bandstop filter; e) allpass filter.

Realization of these filters on a chip is a challenging task. This is due to the expected large areas needed to implement the resistors and the floating capacitors which are associated

with valuable silicon area and large parasitic capacitances. Also, the values of the resistors and capacitors will be inaccurate. Accordingly, realizing such passive elements in system-on-chip (SoC) is not appropriate. So, realizing the passive elements in those filters by only MOS devices can help reduce the required silicon area while keeping the performance within acceptable limits as will be explained in this work.

In this paper, an all-MOS universal voltage-mode biquadratic filter that realizes all the five filtering functions is proposed. According to the proposed filter, the different filtering functions can be determined by an input-bit pattern that can be generated by an encoder or a microcontroller. In addition, there are input terminals that are concerned with the tuning of the parameters of the filter including the cutoff frequency (ω_c), the center frequency (ω_0), and the quality factor (Q). They are aptly called tuning inputs. According to the proposed filter, both fine and coarse tuning are included as will be illustrated shortly. It is the first universal filter that is built using only MOS transistors and can be adapted to any filter type in the real time by a digital control pattern without the need to fabricate any passive elements; a major advantage in SoC applications.

The remainder of this paper is organized as follows: a survey of the CMOS filters is presented in Section 2 along with the universal filters. Section 3 presents the proposed universal filter. The quantitative analysis for this filter is given in Section 4. The simulation results are presented in Section 5. Finally, the paper is concluded in Section 6.

2. PREVIOUS WORK

In this section, a quick survey on CMOS filters is provided. Before this survey, the filter classification is presented.

2.1. Classification of Filters

In addition to the two previously mentioned criteria for filter classification, passband range and order, there are two other criteria. They are the number of the input and the output terminals and the types of the input and the output signals. From the point of view of the number of the input and the output terminals, filters can be classified into four categories; a single-input single-output filter (SISO), a single-input multiple-output filter (SIMO), a multiple-input single-output filter (MISO), and multiple-input multiple-output (MIMO) filter. From the point of view of the types of the input and the output signals, there are also four categories; voltage-mode, current-mode [7], transresistance-mode [8], and transconductance-mode [9]. The proposed filter in this paper is voltage-mode.

Current/Voltage-mode filters require high/low output impedance in order to allow for cascadability with negligible loading effects [1]. Operation in the voltage domain makes the proposed filter having a lower power consumption and a smaller chip area compared to current-mode filters. However, since the transconductance of the operational-transconductance amplifier (OTA) can be tuned over a relatively wide range, the electronic tuning of the current-mode filters realized using OTAs is better than that of voltage-mode counterparts. Also, current-mode filters have wider bandwidth and better linearity compared to voltage-mode ones [10]. For more circuit innovations on current-mode filters, the reader can refer to [11-13]. In [14], a universal filter operating in the four modes was proposed.

2.2. Realization Schemes

There are several realization schemes for implementing filters; they include the second-order LCR resonator, the two-integrator loop topology, the single-amplifier biquadratic active filter, the transconductance (G_m)-*C* filter, using OTAs, and switched-capacitor filter [15]. One method for realizing the resistors in filter circuits is using triode-operated MOS devices [16] such as those used in MOSFET-*C* filters.

Mixed-mode active filters can be realized using one of various building blocks such as differential difference transconductance amplifiers (DDTA) [17-20], voltage-differencing transconductance amplifiers (VDTAs) [21], voltage differencing buffered amplifier (VDBA) [22], current conveyors (CCs) and their derivatives [23-42], OTAs [43-45], current-feedback operational amplifiers (CFOAs) [46, 47], and four-terminal floating nullors (FTFNs) [48].

2.3. Universal Filters

In [49-51], universal filters using OTAs were proposed. The electronic tuning in this topology can be achieved by varying the gain of the OTA via the bias current. Thus, this type of filters can be realized in both bipolar and CMOS technologies and does not require resistors. So, it is suitable for integrated-circuit implementations. In [52], a CMOS universal filter was proposed to be realized using three current-conveyor transconductance amplifiers (CCTA), two grounded capacitors, and four grounded resistors. The programmability of this filter was realized by controlling the values of the bias currents. The single CCTA requires 29 transistors. Filters realized using current conveyors have better performances compared to those based on operational amplifiers from the points of view of bandwidth, linearity, and dynamic range [53]. In [1], a universal current-mode filter was proposed using three inverting second-generation current conveyors, three grounded resistors, and two grounded capacitors. In [54], a universal filter operating in the four modes (voltage, current, transadmittance, and transimpedance) was proposed. According to this filter, both the center frequency and the quality factor are electronically tuned. For more universal filters employing current conveyors, the reader can refer to [55, 56]. The last type, however, does not have an electronic tuning. Other universal filters can be found in [57-64].

The circuits proposed in [65, 66], can realize LP, HP, and BP filter responses but with large area and high output impedance. The filter proposed in [67] realizes all the filter types except the allpass response. It has the previously mentioned limitations in addition to the relatively low-frequency operation. The filters of [68, 69], need component matching to realize the allpass filter response.

Finally, filters with very low cutoff frequencies for biomedical applications can be found in [70-74].

3. THE PROPOSED UNIVERSAL FILTER

In this section, the proposed universal filter is presented. The proposed filter requires resistors and capacitors (both grounded and floating). Due to its small area and ease of fabrication, the MOSFET transistor is now considered the cheapest element in integrated circuits. Fortunately, all the resistors, the grounded capacitors, and the floating capacitors can

be realized using only MOS devices; hence the term "All-MOS" in the title. Refer to Fig. 2 for the circuit schematic of the proposed universal filter. The type of the filter is determined by changing the digital word which is represented by the bits D_0, D_1, …., *and* D_{10}. For example, if the digital word is 11010000001, then the filter response is lowpass. Refer to Table 1 for the relationship between the digital word and the filter response type. Generating the digital word is the function of the encoder shown in Fig. 3. Note that some filters can be realized using multiple bit patterns as indicated in the previously mentioned table. Also, the center frequency and the bandwidth of the filters can be tuned. In fact, the filter type as well as its parameters can be changed during the circuit's operation. For example, during the arrival of a certain input signal, the filter can operate as a lowpass one and thereafter operates as a bandpass one upon changing the controlling code. This feature can be used to secure the communication between two devices during data transmission. Specifically, the two devices can move to different bandwidths during operation while using the same controlled universal filter. So, both devices can use a specific sequence of bandwidth change so that each group of data packets can be sent at different bandwidths.

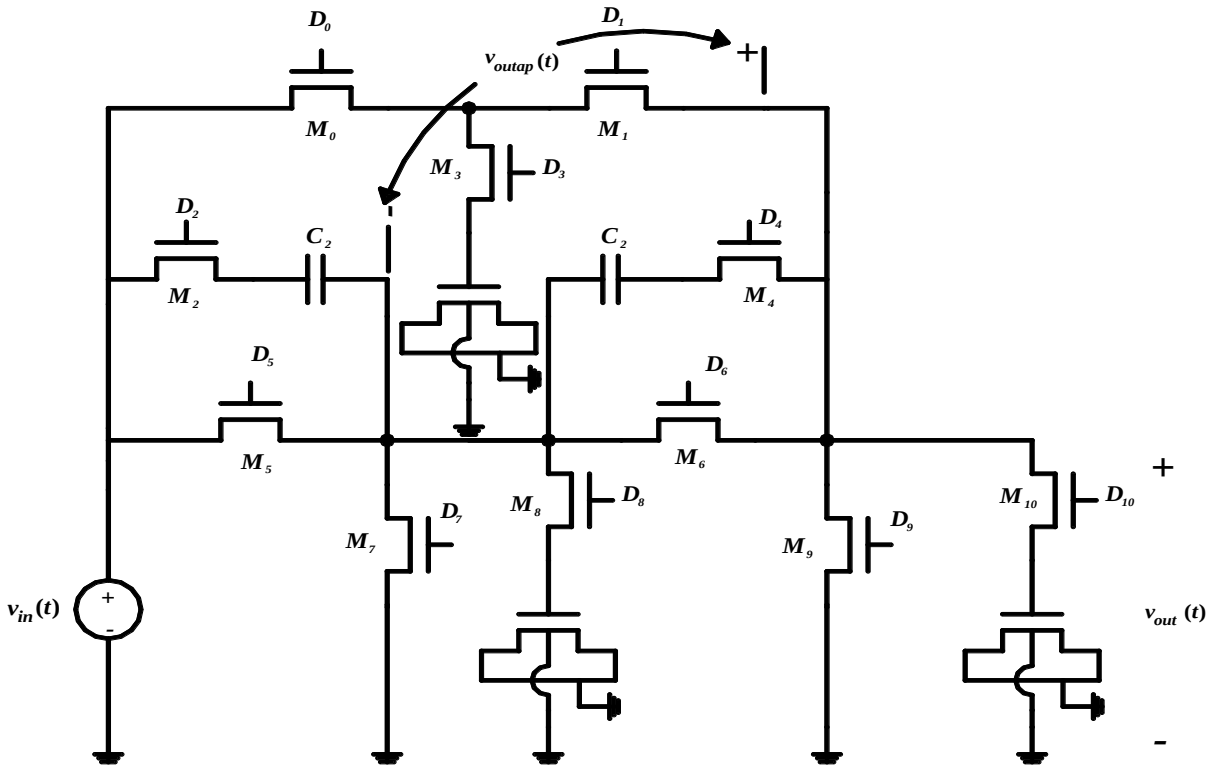

Fig. 2. Circuit schematic of the proposed universal filter.

Table 1. The relationship between the digital word and the filter type.

Filter type	Bit pattern ($D_{10}D_9D_8D_7D_6D_5D_4D_3D_2D_1D_0$)
Lowpass	10000001011 or 10101100000
Highpass	01010010100
Bandpass	01100110000 or 10011000100
Bandstop	00010011111
Allpass	10010100011

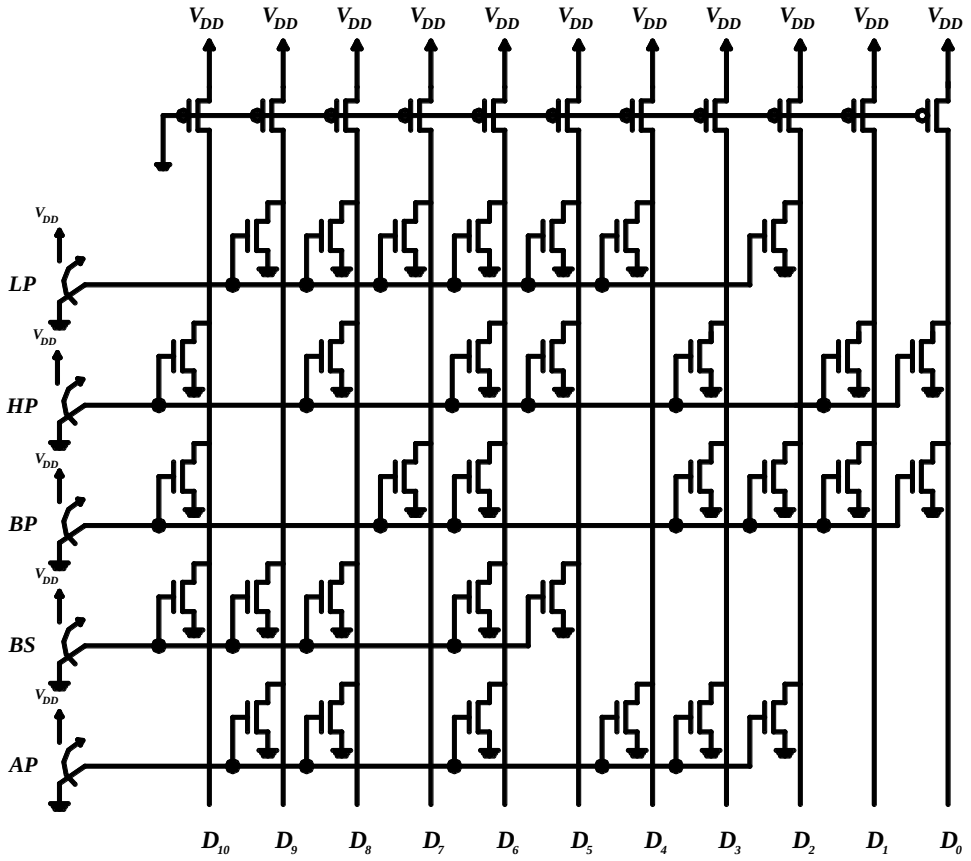

Fig. 3. Circuit schematic of the encoder whose function is to generate the digital word that determines the filter type.

There are two notes concerning the allpass filter in this circuit. The first one is that the output voltage of the allpass filter is taken between the two indicated terminals in Fig. 2 with the output voltage symbol, v_{outap}. The second note is that for ensuring constant magnitude characteristics in this case, the equivalent resistances of M_5 and M_7 must be equal; an essential requirement for this filter type as indicated by Fig. 1(e). Since the source voltage of M_5 is not at 0 V as that of M_7, the threshold voltage of M_5 is larger than that of M_7 due to the body effect. So, the aspect ratio of the former must be chosen slightly larger than that of the latter in order to compensate for this effect. However, as will be indicated in Section 5 for the simulation results, this slight effect can be neglected safely and the magnitude response of the allpass filter will be constant at the frequency range of interest even if the two aspect ratios are the same. Instead, the source and body terminals of M_5 can be connected together in order to eliminate this effect.

The values of the equivalent resistances and capacitances can be determined by properly selecting the dimensions of the realizing transistors. The grounded capacitor can be realized by shorting the drain and source terminals of the MOSFET transistor and using the gate and substrate terminals as the two terminals of the capacitor [75, 76]. The floating capacitor can also be realized using MOS transistors only as will be illustrated in Subsection 4.1. For the time being, it suffices to say that the floating capacitor is put with its conventional symbol.

Due to the operation of the proposed filter in the voltage mode, the filter must have a relatively high input impedance and a relatively low output impedance. Since the input impedance of the proposed filter is not large especially at high frequencies, the need arises to use a unity-gain voltage buffer between the input-signal source and the filter's input. This is the topic of Subsection 4.3. The usage of the buffer is also important when cascading multiple stages in order to reduce the loading effect.

3.1. Tuning

Tuning can be done at one of two levels. The first level is fine tuning which is continuous-range with a relatively narrow range; it is realized by applying an analog control voltage on the substrate terminals of the devices that act as resistors. The second tuning level is coarse tuning which is discrete and in a relatively wide range. It is realized by connecting multiple devices in parallel instead of the single devices that act as resistors and applying a digital control bit pattern on the gate terminals of these devices. Thus, this bit pattern decides the number of parallel-connected devices. Certainly, the order of all the filter types can be increased by cascading multiple lower-order stages; the number of the stages can in turn be decided on by the same method.

3.2. The Encoder Design

The encoder adopted is of the NOR-based array form. Simply stated, activating certain NMOS transistors causes the corresponding lines to discharge to logic "0." Two notes on the design of the encoder are in order. The first one is concerned with the power consumption. In order to limit the power consumption of the encoder, a precharge signal can be used to activate the PMOS devices for a certain time interval, then deactivate them. In this case, it must be noted that the parasitic capacitance at the common-drain node can discharge by the leakage currents of the NMOS devices and thus, there is a minimum frequency for the precharge signal. The second note is that the aspect ratios of the NMOS transistors of the encoders were chosen equal to three while all the PMOS precharging devices were chosen minimum-sized. This is in order to ensure a proper low value for the voltage at the discharged line; 41 mV is obtained according to the simulation.

A final note about the proposed filter is in order here. Although the proposed filter contains only MOS transistors which are certainly active devices; it is a passive one. This is simply because all these devices operate either as resistances or capacitances. Accordingly, there is no amplification and the maximum passband gain is 0 dB. This is confirmed by the fact that the estimated power consumption of the proposed filter is relatively low as shown in Subsection 5.9.

4. QUANTITATIVE ANALYSIS

In this section, some quantitative details about the proposed filter is presented.

4.1. Realization of the Floating Capacitor

In this subsection, the circuit schematic proposed by Hariton et al. [77] for realizing a floating capacitor by only MOS transistors is provided. Refer to Fig. 4 for illustration. In this figure, M_1 operates as a current source with the value of the current, I_{ref}, determined by a

reference voltage, V_{ref}, connected to its gate. M_2 and M_3 operate as a rudimentary current mirror for creating a scaled version of I_{ref} in the two MOS transistors, M_4 and M_5. Let the latter current be I_{bias}. The connection of the drain, source, and body terminals of M_4 and M_5 together allows using their gate terminals as the terminals of the floating capacitor; these two terminals are denoted by C_1 and C_2. The current source as well as the current mirror is nothing but the biasing circuitry for the floating capacitor with the common connection known as the bias terminal.

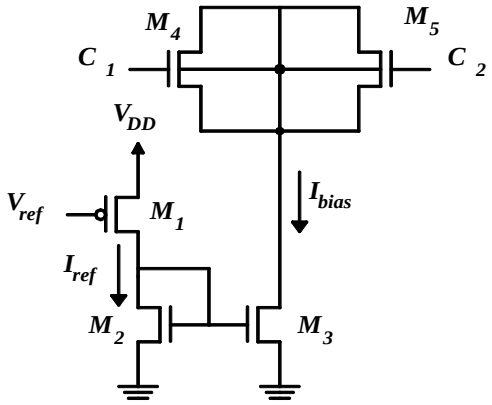

Fig. 4. Circuit schematic for realizing the floating capacitor [77].

One important note is that the current-mirroring ratio of the current mirror must be small enough to obtain a small version of I_{ref} in M_3. This is to ensure operating M_3 in the deep-triode region. In this way, M_3 operates as a resistance between the bias point and ground. As long as the gate voltages of M_4 and M_5 are larger than their threshold voltages, the floating capacitance is voltage-independent. The small value of I_{bias} can be ensured by adopting a relatively long channel length for M_3. The floating capacitance, C, is thus nothing but the series combination of the capacitances of M_4 and M_5, let them be C_{M4} and C_{M5}, respectively. In this discussion, C_{M4} and C_{M5} represent the capacitances associated with the gate terminals of M_4 and M_5, respectively. Also, the dependence of the parasitic capacitance of the MOS transistor is neglected for simplicity. So, C is given by:

$$C = \frac{C_{M4}C_{M5}}{C_{M4}+C_{M5}} \quad (1)$$

Each of C_{M4} and C_{M5} can be found from the following relationship [15]:

$$C_M = WLC_{ox} \quad (2)$$

which is the same relationship of the grounded capacitance. W is the channel width, L is the channel length, and C_{ox} is the gate-oxide capacitance per unit area, i.e. C_{M4} and C_{M5} are proportional to each of the channel widths and lengths of M_4 and M_5, respectively. So, if C_M is to be increased by a factor of n, the channel widths and lengths of M_4 and M_5 are to be increased by a factor of $\sqrt{n}$; alternatively, the channel widths or lengths of M_4 and M_5 are to be increased by a factor of n. On the other hand, the values of C_M do not depend on either V_{ref} or the sizes of M_1, M_2, and M_3. In case of adopting identical devices for M_4 and M_5, C is given by:

$$C = \frac{C_{M4}}{2} \quad (3)$$

The value of C is thus determined by the channel widths and lengths of M_4 and M_5. An alternative configuration for creating the floating capacitor can be done using a current sink along with a PMOS current mirror.

4.2. Filters' Parameters

In this subsection, the expressions of the transfer functions of the five filters are derived along with the cutoff frequencies of the lowpass and highpass filters and the center frequency, bandwidth, and quality factor of the bandpass and bandstop filters. The transfer functions of the five filter types are given by (the basic circuits of Fig. 1 are adopted here):

$$H_{lp}(s) = \frac{1}{s^2R_1R_2C_1C_2+s[R_1(C_1+C_2)+R_2C_2]+1} \quad (4)$$

$$H_{hp}(s) = \frac{s^2R_1R_2C_1C_2}{s^2R_1R_2C_1C_2+s[R_1(C_1+C_2)+R_2C_2]+1} \quad (5)$$

$$H_{bp}(s) = \frac{sR_2C_2}{s^2R_1R_2C_1C_2+s[R_1(C_1+C_2)+R_2C_2]+1} \quad (6)$$

$$H_{bs}(s) = \frac{s^3R_1R_2{}^2R_3C_2{}^2C_3+s^2(R_1+R_2)R_2R_3C_2C_3+sR_2R_3(C_2+C_3)+R_2}{(1+sR_2C_3)(1+sR_3(C_2+C_3))(R_1+R_2+sR_1R_2C_2)-s^2R_2R_3C_3{}^2(R_1+R_2+sR_1R_2C_2)} \quad (7)$$

$$H_{ap}(s) = \frac{1-sRC}{2(1+sRC)} \quad (8)$$

The load resistance was assumed to be infinite when deriving these equations. The cutoff frequency of the lowpass and highpass filters are given by (assuming that $R_1 = R_2 = R$ and $C_1 = C_2 = C$):

$$f_c = \frac{1}{4\pi\sqrt{2}RC} \quad (9)$$

The expressions of the center frequency, f_0, and the quality factor, Q, of the bandpass filter can be obtained by comparing its associated transfer function with the standard form of the transfer function. So,

$$f_0 = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \quad (10)$$

and

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1+R_1C_2+R_2C_2} \quad (11)$$

The bandwidth, BW, of the bandpass filter can be obtained from the ratio between f_0 and Q as:

$$BW = \frac{R_1C_1+R_1C_2+R_2C_2}{R_1R_2C_1C_2} \quad (12)$$

The expressions of the corresponding parameters of the bandstop filter can be derived in a similar manner. The design procedure requires substituting the values of the filter parameters such as f_c, f_0, Q, or BW in the corresponding equation in order to find the corresponding values of the constituting resistors and capacitors. Then, the extracted values of resistances and capacitances are substituted in the relevant equations regarding the transistors' parameters. The equations related to the floating and grounded capacitances were mentioned in Subsection 4.1 while those related to the resistances are derived in Subsection 4.5.

4.3. Unity-Gain Voltage Buffer

As stated in Section 3, the need arises to use a buffer with the proposed filter. The adopted buffer must have a very high input impedance, a very low output impedance, and a voltage gain that is close to unity. The source follower is a suitable candidate for these requirements [78]. Refer to Fig. 5(a) for a simple voltage buffer using the source follower biased by an ideal current source, I. R_L is the load resistance. The current source can be realized by a cascode stage as shown in Fig. 5(b) due to its high output resistance; V_{G2} and

V_{G3} are the dc biasing voltages of M_{B2} and M_{B3}. For the adopted range of frequencies in this work, the effect of the internal capacitances can be safely neglected. So, the input impedance can be considered infinite. The output impedance, R_{out}, is simply the parallel combination of the resistance seen at the source terminal of M_{B1} and the output resistance of the cascode current source which is given by [78]:

$$R_{cascode} = [1 + (g_{m2} + g_{mb2})r_{02}]r_{03} + r_{02} \quad (13)$$

where g_{m2} is the ac transconductance of M_{B2}, g_{mb2} is the ac body transconductance of M_{B2}, and r_{02} and r_{03} are the ac drain-to-source resistances of M_{B2} and M_{B3}, respectively. So, R_{out} is given by:

$$R_{out} = \frac{r_{01}}{1+(g_{m1}+g_{mb1})r_{01}} //\left[[1 + (g_{m2} + g_{mb2})r_{02}]r_{03} + r_{02}\right] \quad (14)$$

where g_{m1}, g_{mb1}, and r_{01} are the corresponding parameters of M_{B1}. For the channel lengths adopted, r_0 can be considered relatively large. Neglecting g_{mb} with respect to g_m, R_{out} can be approximated to:

$$R_{out} = \frac{1}{g_{m1}} // g_{m2}r_{02}r_{03} \quad (15)$$

g_m is given by:

$$g_m = k_n'\left(\frac{W}{L}\right)_n (V_{GS} - V_{thn}) \quad (16)$$

where k_n' is the process-transconductance parameter, $(W/L)_n$ is the aspect ratio, V_{thn} is the threshold voltage, and V_{GS} is the dc gate-to-source voltage; all of the corresponding device. g_{mb} is directly proportional to g_m [15]. So, in order to obtain a relatively low R_{out}, M_{B1} is to have a relatively large aspect ratio. The voltage gain, A_v, can be obtained from the small-signal equivalent circuit of Fig. 6 and is given by:

$$A_v = \frac{g_{m1}(r_{01}//R_L//R_{cascode})}{1+(g_{m1}+g_{mb1})(r_{01}//R_L//R_{cascode})} \quad (17)$$

which can be approximated to 1 when r_{01}, $R_{cascode}$, and R_L are relatively large and g_{mb} is neglected. It is apparent from Eq. (17) that g_{m1} must be large compared to g_{mb1} in order to overwhelm its effect in the denominator of Eq. (17) and thus A_v can be considered close to unity. This also requires a large size for M_{B1}. Finally, it must be noted that this simple buffer is not suitable for use with the floating output of the AP filter. Instead, a suitable differential-to-single ended converter can be interposed between the AP filter and the adopted buffer. This completes the design of the adopted voltage buffer.

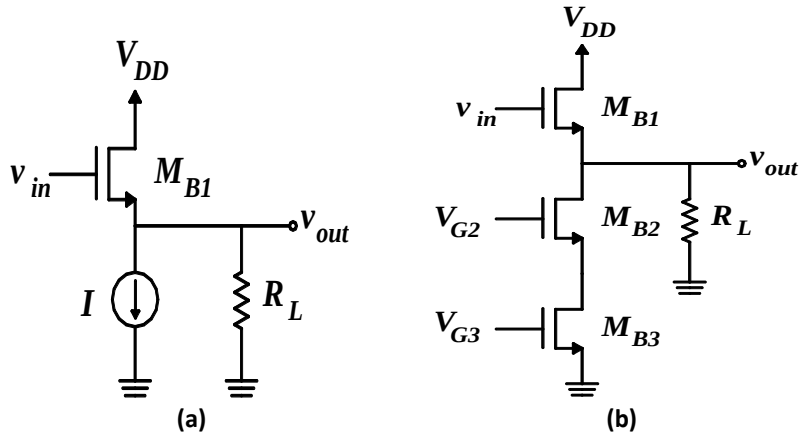

Fig. 5. a) A simple voltage buffer using the source follower; b) the realization of the current source by a cascode stage [78].

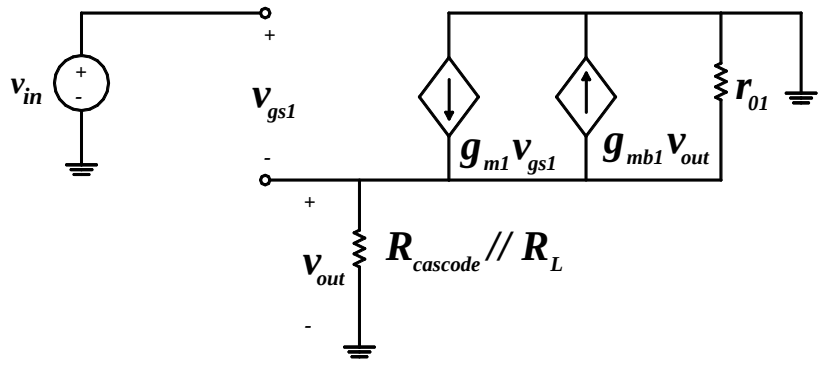

Fig. 6. Small-signal equivalent circuit of the circuit depicted in Fig. 5(b).

4.4. Maximum Frequency of Operation

Since the response of the filter versus frequency is the main criterion in assessing the filter, the maximum frequency at which the MOS transistor can operate is of a great interest. A useful figure of merit for this evaluation is the transition frequency, f_T. The transition frequency is defined as the frequency at which the short-circuit current gain of the common-source configuration is unity [15]. f_T is given by [15]:

$$f_T \approx \frac{1.5\mu_n V_{OV}}{2\pi L^2} \tag{18}$$

where μ_n is the mobility of free electrons, and V_{OV} is the gate overdrive voltage. Increasing the channel length certainly reduces f_T. However, it must be noted that the channel length determines the equivalent resistance of the MOS transistor as discussed in the previous subsection. Increasing the channel length causes the equivalent MOS resistance to increase. The increase in the equivalent resistance is associated with a decrease in the cutoff frequency. For typical values of the 0.13 μm CMOS technology, μ_n is equal to 1350 cm²/V.s and V_{OV} can be up to 0.8 V. For a channel length of 1 μm, f_T is typically 25.78 GHz. This frequency is much higher than the frequencies of interest adopted in this paper.

4.5. Tuning

In this subsection, both the fine and coarse tuning are quantified. Specifically, the relationship between the analog control voltage, v_c, and the equivalent resistance of the MOS transistor, R, is derived in accordance with the fine tuning. Also, the relationship between the digital word and R is derived in accordance with the coarse tuning.

4.5.1. Fine Tuning

The equivalent resistance of the NMOS transistor in both the triode and saturation regions can be found as the ratio of the drain-to-source voltage, v_{DS}, and the drain current, i_D. Assume that the transistor when operates in the triode region has a negligible v_{DS} with respect to the gate overdrive voltage, that it operates in the deep-triode region. In this case, the equivalent resistance, R_{triode}, is given by [15]:

$$R_{triode} = \frac{1}{k_n'\left(\frac{W}{L}\right)_n (v_{GS} - V_{thn})} \tag{19}$$

In Eq. (19), the long-channel square-law MOSFET model is implicitly adopted [79]. The relatively large adopted channel lengths for the transistors justify the usage of this model.

Controlling the equivalent resistance is done by varying the threshold voltage by virtue of the body effect. V_{thn} is related to the body voltage through the following relationship [80]:

$$V_{thn} \approx V_{thn0} - kv_{BS} \tag{20}$$

v_{BS} is the body-to-source voltage, k is the linearized body-effect parameter, and V_{thn0} is the threshold voltage at v_{BS} = 0 V. Substituting V_{thn} from Eq. (20) into Eq. (19) results in:

$$R_{triode} = \frac{1}{k_n'\left(\frac{W}{L}\right)_n (V_{DD} - V_{thn0} + kv_c)} \tag{21}$$

In Eq. (21), the source voltage is assumed to be 0 V for simplifying the analysis and v_{GS} was substituted by V_{DD}. Now, if the transistor operates in the saturation region, the equivalent resistance, R_{sat}, is given by:

$$R_{sat} = \frac{v_{DS}}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (v_{GS} - V_{thn})^2 (1 + \lambda_n v_{DS})} \tag{22}$$

Substituting V_{thn} by Eq. (20), v_{GS} by V_{DD}, and v_{DS} by its average value in the range of the saturation region extending from V_{DD} to V_{DD} – V_{thn0} results in:

$$R_{sat} = \frac{V_{DD} - \frac{1}{2}V_{thn0}}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_{DD} - V_{thn0} + kv_c)^2 \left[1 + \lambda_n \left(V_{DD} - \frac{1}{2}V_{thn0}\right)\right]} \tag{23}$$

Since the transistor operates part of the time in the triode region and another part in the saturation region, the equivalent resistance, R, can be found as a linear combination of R_{triode} and R_{sat}. This linear combination can be done as follows:

$$R = A_{triode}R_{triode} + A_{sat}R_{sat} \tag{24}$$

where A_{triode} and A_{sat} are two parameters that are related to the fraction of time the MOS device operates in the triode and saturation regions, respectively. Since during the activation of the MOS device, the device either operates in the triode region or the saturation region, we get:

$$A_{triode} + A_{sat} = 1 \tag{25}$$

That is, operation in the triode and saturation regions are two mutually exclusive events and thus the summation of their probabilities is one. Relating A_{triode} and A_{sat} to their range of voltages with respect to the whole range of v_{DS} which is V_{DD}, we get:

$$A_{triode} = \frac{V_{DD} - V_{thn0}}{V_{DD}} \tag{26}$$

and

$$A_{sat} = \frac{V_{thn0}}{V_{DD}} \tag{27}$$

Refer to Fig. 7 for the relationship between the equivalent resistance, R, and the control voltage, v_c. It must be noted that when v_c increases above a certain value (approximately $V_{DD}/2$ = 0.6 V), the effect of the latchup appears causing the parasitic npn transistor inherently present in the NMOS transistor to conduct. So, the maximum value of v_c applied to the substrate terminal is $V_{DD}/2$. The parameters of [81] are adopted in this subsection.

Another method for performing the continuous tuning is by using the circuit shown in Fig. 8 [37]. Shorting the gate and drain terminals together ensure that the two devices, M_{R1} and M_{R2}, operate in the saturation region. Assuming that these two devices are matched, the expression of the equivalent resistance which is the ratio between v_{in} and i_{in} was found to be [37]:

$$R = \frac{1}{2k_n'\left(\frac{W}{L}\right)_n (v_c - V_{thn})} \tag{28}$$

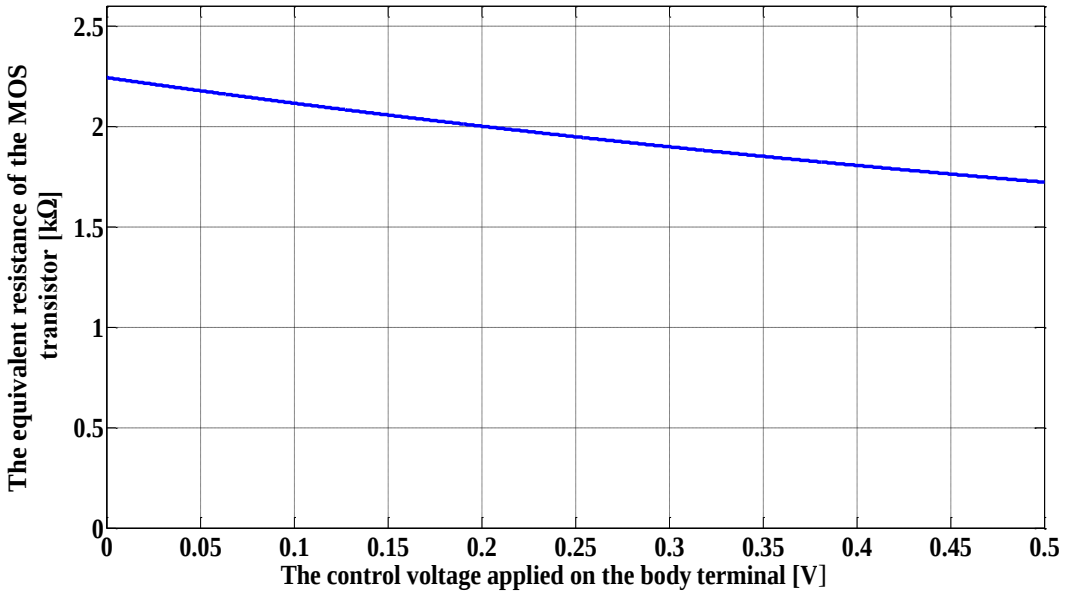

Fig. 7. The relationship between the equivalent resistance and the control voltage applied on the body terminal.

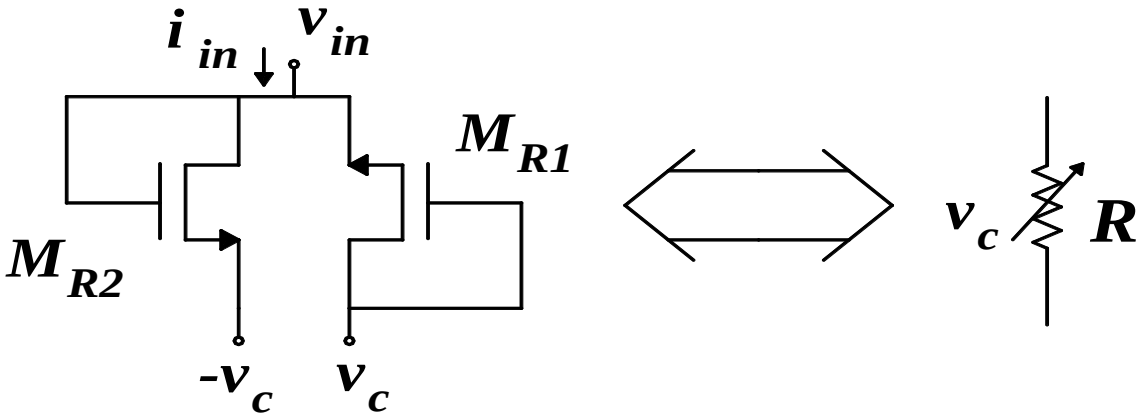

Fig. 8. An electronically tunable resistor using two NMOS transistors [37].

4.5.2. Coarse Tuning

The equivalent resistance of the conducting device can be controlled by simply connecting multiple transistors in parallel and controlling the number of the conducting devices by a digital control word. Fig. 9 illustrates the coarse tuning assuming n parallel-connected devices. Assume that the aspect ratios of these devices are binary-weighted; that is, if M_0 is assumed to have an aspect ratio equal to $(W/L)_n$, then M_1, M_2, …., and M_{n-1} will have aspect ratios equal to $2(W/L)_n$, $4(W/L)_n$, …., and $2^{n-1}(W/L)_n$, respectively. Adopting the expression of the triode region for the equivalent resistance, we get the following expressions for the equivalent resistances:

$$R_0 = k \tag{29}$$

$$R_1 = \frac{k}{2} \tag{30}$$

$$R_{n-1} = \frac{k}{2^{n-1}} \tag{31}$$

where k is a technology-dependent parameter that will be treated as constant for our purposes here and is given by:

$$k = \frac{1}{k_n'\left(\frac{W}{L}\right)_n (V_{DD} - V_{thn0})} \tag{32}$$

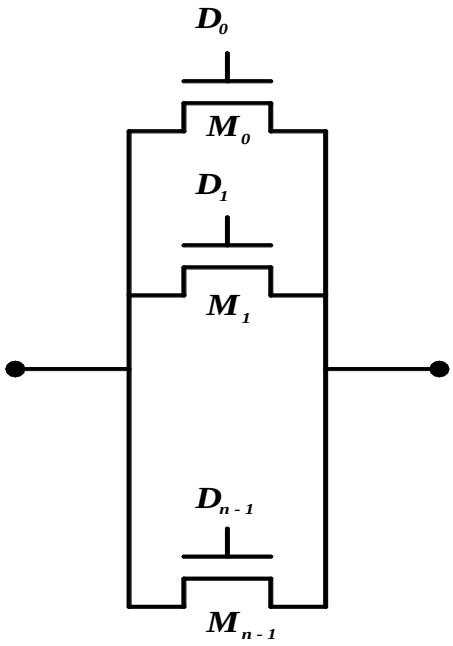

Fig. 9. The parallel combination of properly sized NMOS devices for coarse tuning.

In the previous expressions, v_{GS} was substituted by V_{DD} and the body effect was neglected. The equivalent resistance of this parallel combination is given by:

$$R = \frac{k}{D_0+2D_1+\cdots+2^{n-1}D_{n-1}} \quad (33)$$

Refer to Fig. 10 for the relationship between the equivalent resistance of the parallel-connected MOS devices and the decimal equivalent of the digital control word assuming four parallel-connected devices with four controlling bits. It must be noted that the digital input pattern of 0000 is not allowed here as it results in an infinite equivalent resistance. It is obvious that the coarse tuning has a higher sensitivity than that of the fine tuning.

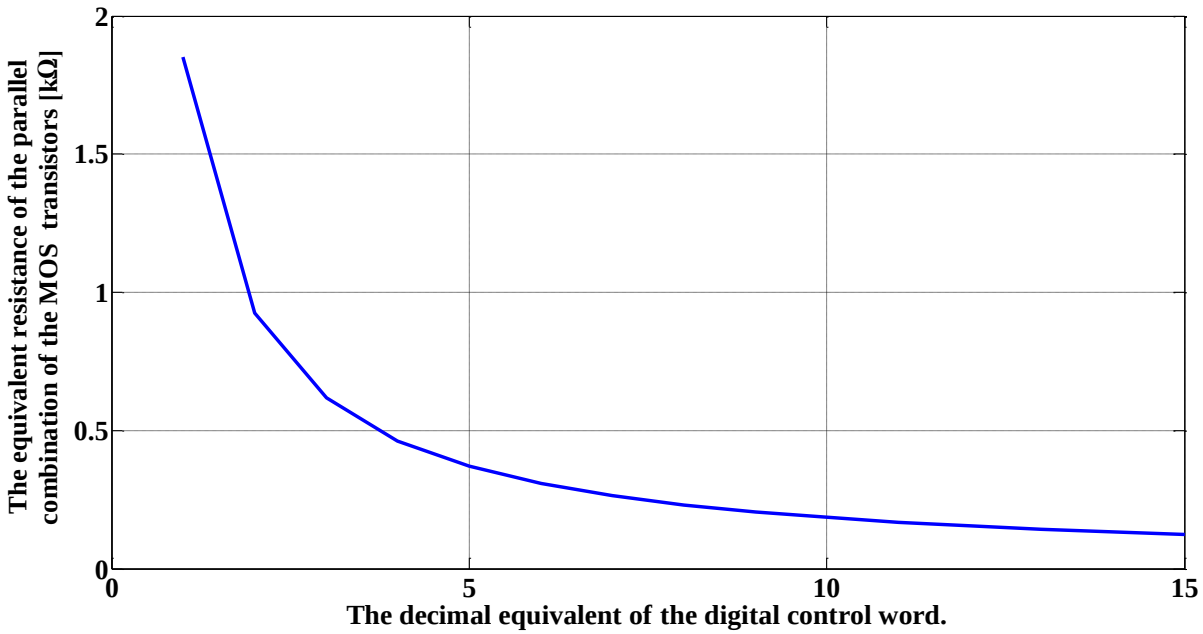

Fig. 10. The relationship between the equivalent resistance of the parallel combination of the MOSFET transistors and the decimal equivalent of the digital control word.

4.6. Sensitivity

The filter parameters depend on various components which in turn have process variations and temperature coefficients. So, the sensitivty of the filter parameters to the change of these component values are of interest. The classicial sensitivity function of a parameter, y, to a component value, x, is defined as the per-unit change in y due to a given per-unit change in x. It is denoted by S_x^y and is given by [82]:

$$S_x^y = \frac{x}{y}\frac{\partial y}{\partial x} \tag{34}$$

Usually, the component values depend on certain transistor parameters. So, the sensitivity of the filter parameters to the change of the transistor parameters is of interest. For example, f_c of the LP and HP filters depend on R and C. Each R and C in turn depends on k_n', W, L, and V_{thn} of the realizing transistor. So, the sensitivity of f_c to the change in the values of k_n', W, L, and V_{thn} is of interest. The latter can be found using the chain rule of differentiation as follows [82]: If $y = f_1(u)$ and $u = f_2(x)$, then;

$$S_x^y = S_u^y S_x^u \tag{35}$$

For the LP and HP filters, the sensitivities of f_c to R and C are given by:

$$S_R^{f_c} = S_C^{f_c} = -1 \tag{36}$$

For the BP filter, the following sensitivities can be found:

$$S_{R_1}^{f_0} = S_{R_2}^{f_0} = S_{C_1}^{f_0} = S_{C_2}^{f_0} = -1 \tag{37}$$

$$S_{R_1}^{Q} = \frac{0.5[-R_1C_1 - R_1C_2 + R_2C_2]}{R_1C_1 + R_1C_2 + R_2C_2} \tag{38}$$

$$S_{R_2}^{Q} = \frac{0.5[R_1C_1 + R_1C_2 - R_2C_2]}{R_1C_1 + R_1C_2 + R_2C_2} \tag{39}$$

$$S_{C_1}^{Q} = \frac{0.5[-R_1C_1 + R_1C_2 + R_2C_2]}{R_1C_1 + R_1C_2 + R_2C_2} \tag{40}$$

$$S_{C_2}^{Q} = \frac{0.5[-R_1C_1 + R_1C_2 - R_2C_2]}{R_1C_1 + R_1C_2 + R_2C_2} \tag{41}$$

$$S_{R_1}^{BW} = \frac{-R_2C_2}{R_1C_1 + R_1C_2 + R_2C_2} \tag{42}$$

$$S_{R_2}^{BW} = \frac{-R_1C_1 - R_1C_2}{R_1C_1 + R_1C_2 + R_2C_2} \tag{43}$$

$$S_{C_1}^{BW} = \frac{-R_1C_2 - R_2C_2}{R_1C_1 + R_1C_2 + R_2C_2} \tag{44}$$

$$S_{C_2}^{BW} = \frac{-R_1C_1}{R_1C_1 + R_1C_2 + R_2C_2} \tag{45}$$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$, then the following values are obtained:

$S_{R_1}^{Q} = \frac{-1}{6}, S_{R_2}^{Q} = \frac{1}{6}, S_{C_1}^{Q} = \frac{1}{6}, S_{C_2}^{Q} = \frac{-1}{6}, S_{R_1}^{BW} = \frac{-1}{3}, S_{R_2}^{BW} = \frac{-2}{3}, S_{C_1}^{BW} = \frac{-2}{3}, S_{C_2}^{BW} = \frac{-1}{3}$.

R and C depend on k_n', W, L, and V_{thn} as evident from Eqs. (19) and (2), respectively. In case of the LP filter, we have:

$$S_{k_n'}^{R} = -1, S_W^R = -1, S_L^R = 1$$
$$S_{V_{thn}}^{R} = \frac{V_{thn}}{V_{GS} - V_{thn}} \tag{46}$$
$$S_W^C = S_L^C = S_{C_{ox}}^C = 1$$

It is obvious from Eq. (46) that $S_{V_{thn}}^R$ decreases when increasing V_{GS}; an expected result as increasing V_{GS} overwhelms the effect of V_{thn}. In case of the floating capacitance adopted in the HP or BP filters, the sensitivities of C to each of k_n', W, L, and V_{thn} are the same as those of the LP filter but multiplied by 0.5 due to the factor, 0.5, in Eq. (3) for the floating capacitance. As a

final note, the dimensions to which the sensistivity is relatively large should be selected larger than the minimum-feature size of the adopted technology.

5. SIMULATION RESULTS

In this section, the performance of the proposed filter is verified by simulation using the 0.13 µm CMOS technology with V_{DD} equal to 1.2 V [83]. Unless otherwise specified, the following parameters are adopted: the control voltage, v_c, is taken equal to 0 V. In order to operate in the frequency range of several hundreds of MHz or a few GHZ, the channel lengths and widths of the transistors operating as resistors are equal to 1 µm and 0.13 µm, respectively, while those operating as grounded capacitors are 1 µm and 1.3 µm, respectively. A grounded capacitance of 13 fF is obtained with these dimensions. The sizes of the transistors in the floating-capacitor circuit are illustrated in Table 2. Note that for proper operation of the equivalent circuit of the floating capacitor, the aspect ratio of M_3 must be small as discussed in Subsection 4.1, so it is selected equal to 0.1. An equivalent floating capacitance of 5 fF is obtained with these dimensions. Refer to Table 3 for the proposed-filter specifications.

First, the magnitude and phase responses of the five filters are presented using the ac analysis. Then, the total-harmonic distortion is evaluated using Fourier analysis and the effect of noise is investigated using the noise analysis. The effects of the process, voltage, and temperature variations are investigated using the Monte-Carlo analysis, the parameter-sweep analysis, and the temperature-sweep analysis, respectively. The fine and coarse tuning is also verified. The power consumption is then evaluated. Finally, a comparison between the proposed filter and previous schemes is performed.

Table 2. Dimensions of the transistors in the floating-capacitor circuit.

Transistor	L [µm]	W [µm]
M_1 and M_2	0.13	0.13
M_3	1.3	0.13
M_4 and M_5	1.3	1.3

Table 3. Specifications of the proposed filter.

Process technology	0.13 µm CMOS technology
Power supply	1.2 V
Filter mode	Voltage mode
Filter types	LP, HP, BP, BS, and AP

5.1. Frequency-Domain Response

Figs. 11, 12, 13, 14, and 15 show the magnitude and phase characteristics of the lowpass, highpass, bandpass, bandstop, and allpass filters, respectively. The relevant cutoff and center frequencies of the first four filter types are shown in Table 4. The magnitude response exhibits a constant value below a frequency of 100 MHz as expected for an allpass filter. However, when the frequency increases above this limit, the effect of the internal capacitances of the MOS devices comes into action and the magnitude response decreases exhibiting a lowpass-filter response. This puts an upper frequency for its operation.

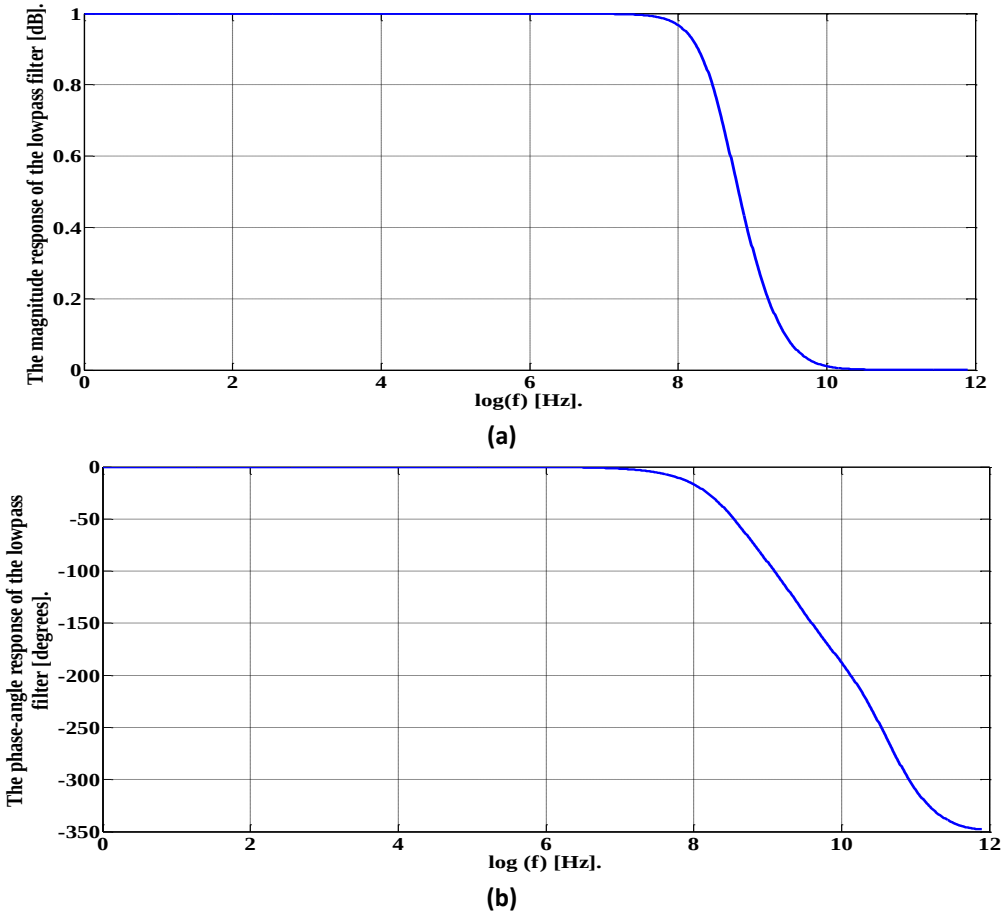

Fig. 11. The steady-state transfer function: a) magnitude; b) phase characteristics of the lowpass filter.

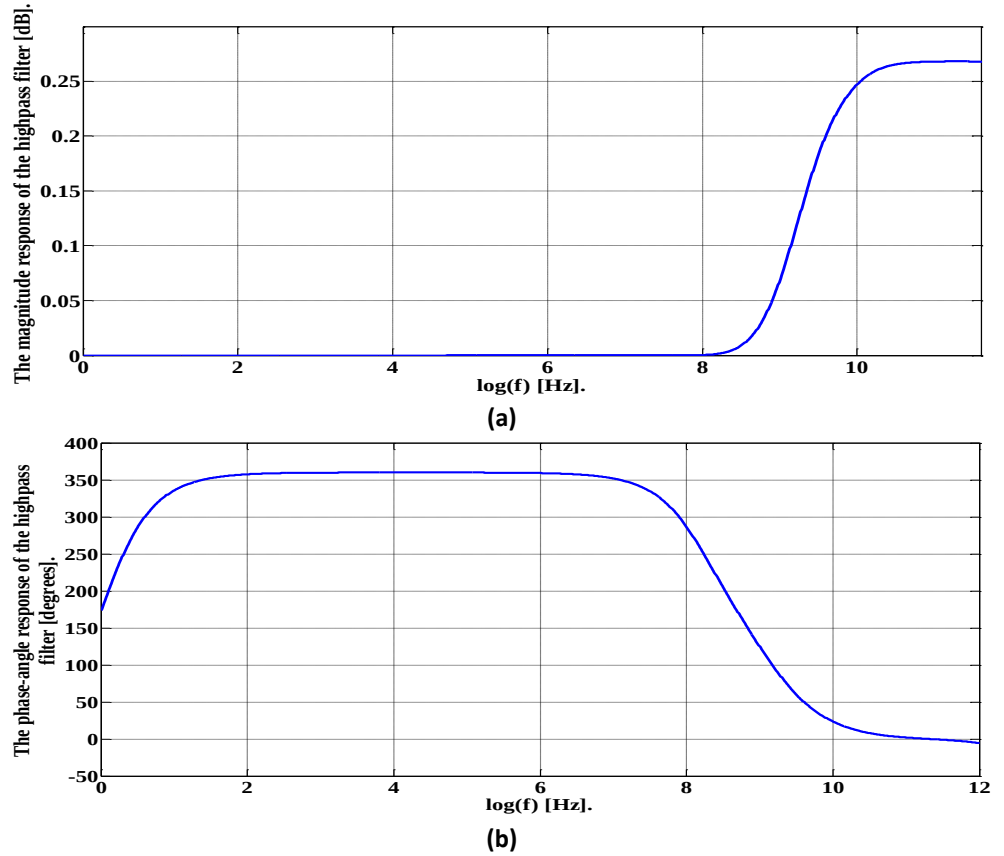

Fig. 12. The steady-state transfer function: a) magnitude; b) phase characteristics of the highpass filter.

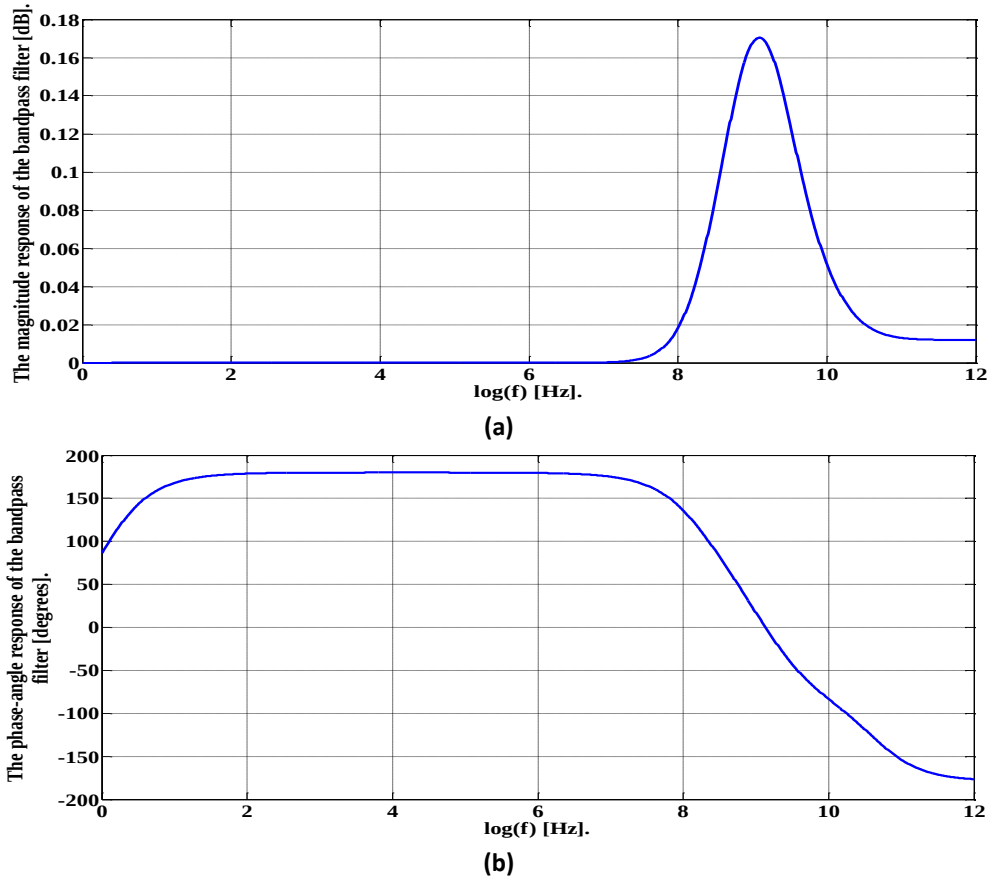

Fig. 13. The steady-state transfer function: a) magnitude; b) phase characteristics of the bandpass filter.

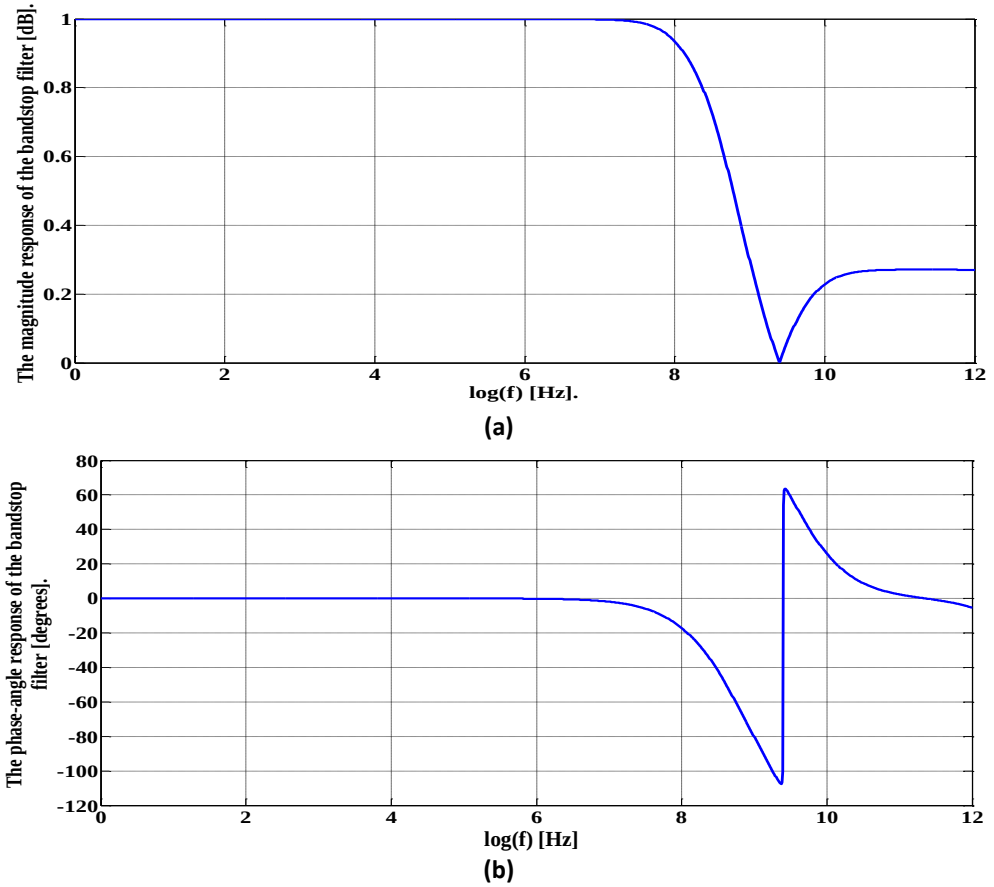

Fig. 14. The steady-state transfer function: a) magnitude; b) phase characteristics of the bandstop filter.

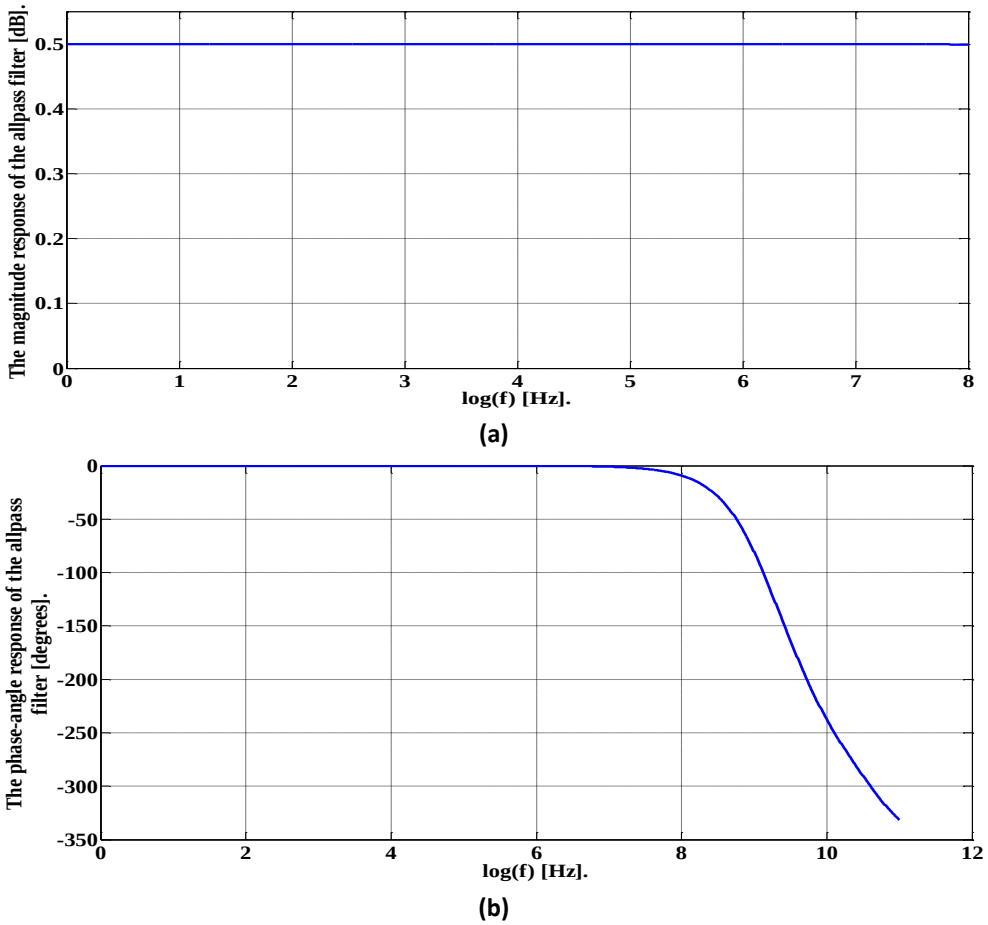

Fig. 15. The steady-state transfer function: a) magnitude; b) phase characteristics of the allpass filter.

Table 4. Critical frequencies of the four filter types.

Filter Type	Cutoff frequencies	Center frequency
Lowpass	381.5 MHz	NA*
Highpass	3.3 GHz	NA*
Bandpass	470 MHz and 3.4 GHz	1.23 GHz
Bandstop	336 MHz and 6.66 GHz	2.45 GHz

*NA = Not applicable.

5.2. Total-Harmonic Distortion

Fourier analysis is utilized here for evaluating the total-harmonic distortion (THD) for the first four filter types. The number of harmonics is taken equal to nine. Since the magnitude of the harmonic component is inversely proportional to its order, nine is very sufficient for our estimations as the harmonics above the ninth one can be safely neglected. Table 5 shows the THD values for these filters at three frequencies for each type; the first one is much lower than the cutoff frequency, the second one is at the cutoff frequency, and the third one is in the stopband. The amplitude of the input signal is assumed to be 200 mVpp. The sound performance of the proposed filters is verified by the obvious difference between the much larger THD at the stopband compared to the much smaller THD at the passband. For example, the THD of the HPF at 1 kHz is 14017% while it is equal to 0.018% for the LPF at 100 kHz. The plot of the THD versus the input-signal magnitude for the four filters are shown in Fig. 16 for a range from 10 mV to 100 mV for the input signal. Due to their close

THD values, the LP and BS filters are combined in the same plot. The same is true for the HP and BP filters. It can be easily noted that the lowpass filter has the minimum THD while the highpass filter has the maximum one for this range of the input-signal magnitude. Given the maximum permissible THD, the maximum input-signal magnitudes of the four filters can be determined.

Table 5. The THD values of the four filter types.

Filter type	Frequency	THD
Lowpass	100 kHz	0.018%
	381.5 MHz	2.4%
	500 GHz	537%
Highpass	10 GHz	4.06%
	3.3 GHz	2.87%
	1 kHz	14017%
Bandpass	100 kHz	5.68%
	470 MHz	3.13%
	1.23 GHz	4%
Bandstop	100 kHz	0.018%
	336 MHz	2.62%
	2.45 GHz	85%

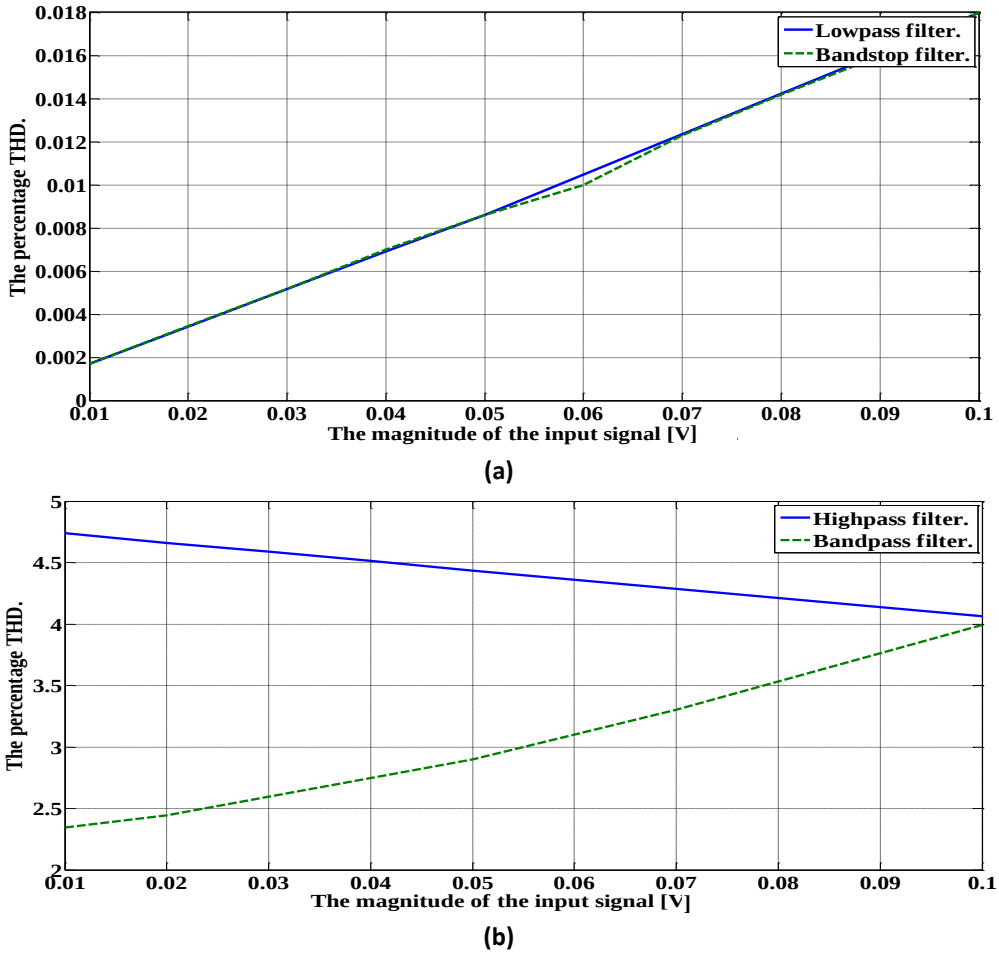

Fig. 16. Plots of the THD versus the magnitude of the input signal for: a) the LP and BS filters; b) the HP and BP filters. The following frequencies are adopted for the four filter types: 100 kHz, 10 GHz, 1.23 GHz, and 100 kHz for the LP, HP, BP, and BS filters, respectively.

5.3. Noise Effect

The noise analysis is used to evalaue the effect of noise on the performance of the proposed filters. The frequency of the input signal is taken equal to 100 kHz. The noises at the output terminals of the five filters are 1.43, 1.75, 1.74, 1.77, and 1.77 (all in mV/sqrt(Hz)), resepctively. These values are too small compared to typical values of the input-signal amplitude. These values along with the maximum permissible values discussed in Subsection 5.2 determine the dynamic range of the four filters. Note that the noise at the output terminal of the LPF is smaller than those of the remaining four types. This is barely unexpected due to the elimination of the high-frequency components inherently found in the noisy signal by the LPF.

5.4. Effect of Process Variations

The effect of the process variations on the performance of the first four filters is investigated in this subsection using the Monte-Carlo analysis. 10% Gaussian variations are assumed in each of the channel length, L, and the threshold voltage, V_{thn}. The percentage variations in the cutoff and center frequencies of the first four filters are evaluated with respect to the nominal run. The results are shown in Table 6; for the LP and HP filters, the cutoff frequencies are considered while for the BP and BS filters, the center frequencies are considered. The LP filter is the most sensitive to process variations while the BP filter is the least sensitive one.

Table 6. Variations in the cutoff and center frequencies with the process variations.

Filter type	Percentage variation
Lowpass	-10.4% to 18.6%
Highpass	-8.3% to 7.5%
Bandpass	-0.33% to 0.16%
Bandstop	-8.7% to 0.087%

5.5. Effect of V_{DD} Variations

The effect of the variations of the power-supply voltage on the performance of the first four filters is investigated in this subsection using the parameter-sweep analysis. The range of variations is ±0.1 V. The percentage variations in the cutoff and center frequencies of the first four filters are shown in Table 7.

Table 7. Variations in the cutoff and center frequencies with the power-supply variations.

Filter type	Percentage variation
Lowpass	-7.5% to 6.2%
Highpass	±10.6%
Bandpass	-8% to 11.4%
Bandstop	-4.8% to 10.2%

5.6. Effect of Temperature Variations

The effect of the temperature variations on the performance of the first four filters is investigated in this subsection using the temperature-sweep analysis. The temperature range from 15 ^{o}C to 50 ^{o}C is taken into account. The variations in the cutoff and center frequencies of the first four filters are shown in Table 8.

Table 8. Variations in the cutoff and center frequencies with the temperature variations.

Filter type	Frequency
Lowpass	295 MHz to 455.5 MHz
Highpass	2.7 GHz to 3.9 GHz
Bandpass	0.93 GHz to 1.43 GHz
Bandstop	1.86 GHz to 2.95 GHz

5.7. Tunability

In this subsection, both the fine and coarse tunability are verified.

5.7.1. Fine Tuning

As discussed in Section 4, the cutoff frequency of the LP or the HP filters can be tuned by varying the substrate voltage of the MOS transistors acting as resistors. Increasing v_c causes the equivalent resistance of the MOS transistor to decrease. So, the cutoff frequency increases with increasing the control voltage for the LP filter. This is confirmed by the plots of Fig. 17(a). By the same token, the cutoff frequency of the HP filter increases with increasing v_c as shown in Fig. 17(b).

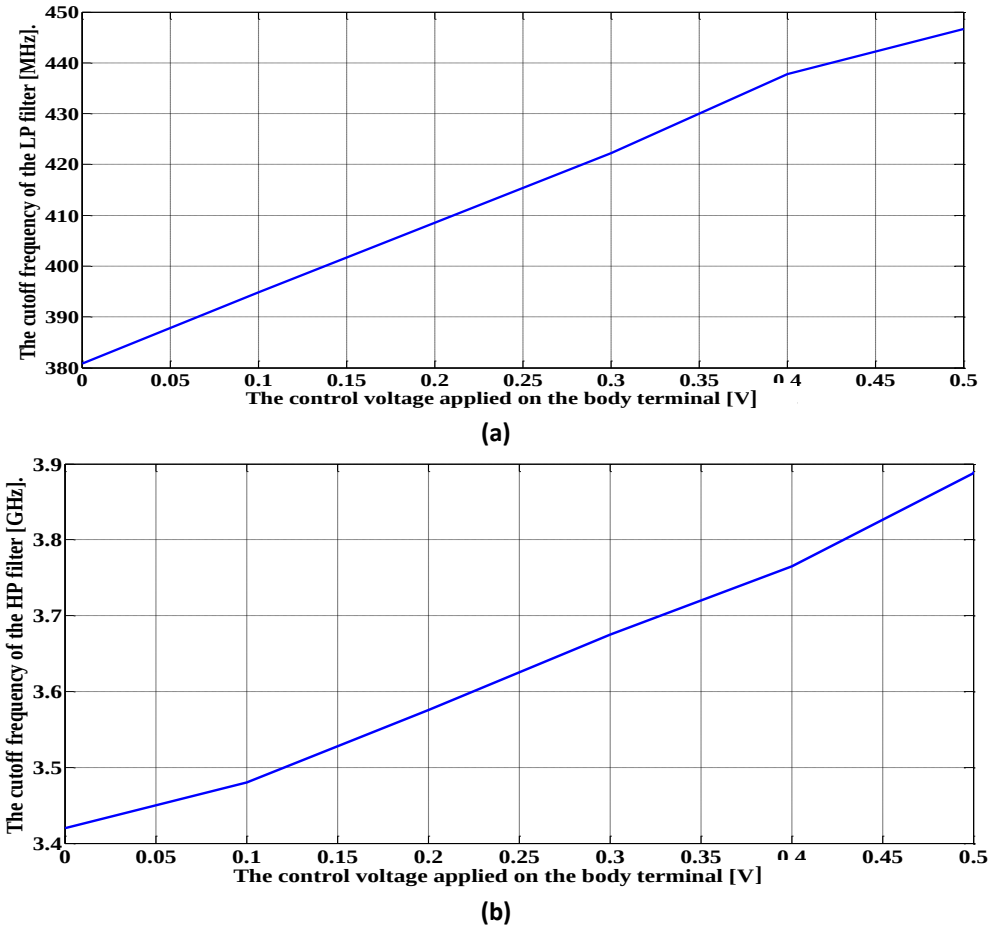

Fig. 17. Change in the cutoff frequency with the control voltage for the: a) LP filter; b) HP filter.

Since the synthesized bandpass filter consists of cascaded lowpass and highpass filter sections, its bandwidth increases when the cutoff frequency of the former is increased and/or the cutoff frequency of the latter is reduced. So, the bandwidth of the synthesized bandpass filter increases with increasing the control voltage applied on the transistors acting as resistors

in the LP filter section, let it be v_{c1}, and/or decreasing the control voltage applied on the transistors acting as resistors in the HP filter section, let it be v_{c2}. This is confirmed by the simulation results shown in Figs. 18(a) and (b) which show several plots for the magnitude characteristics of the BPF for several values of v_{c1} and v_{c2}, respectively. Concerning the bandstop filter, the range of change of its magnitude characteristics with v_{c1} or v_{c2} is very narrow. The maximum value adopted for the control voltages is $V_{DD}/2$ in order to avoid the latchup effect. If any of the control voltages is increased above this value, the latchup effect gets into action with the result that the passband gain decreases. This is confirmed by the plot shown in Fig. 19 for the maximum passband gain of the LPF versus the control voltage.

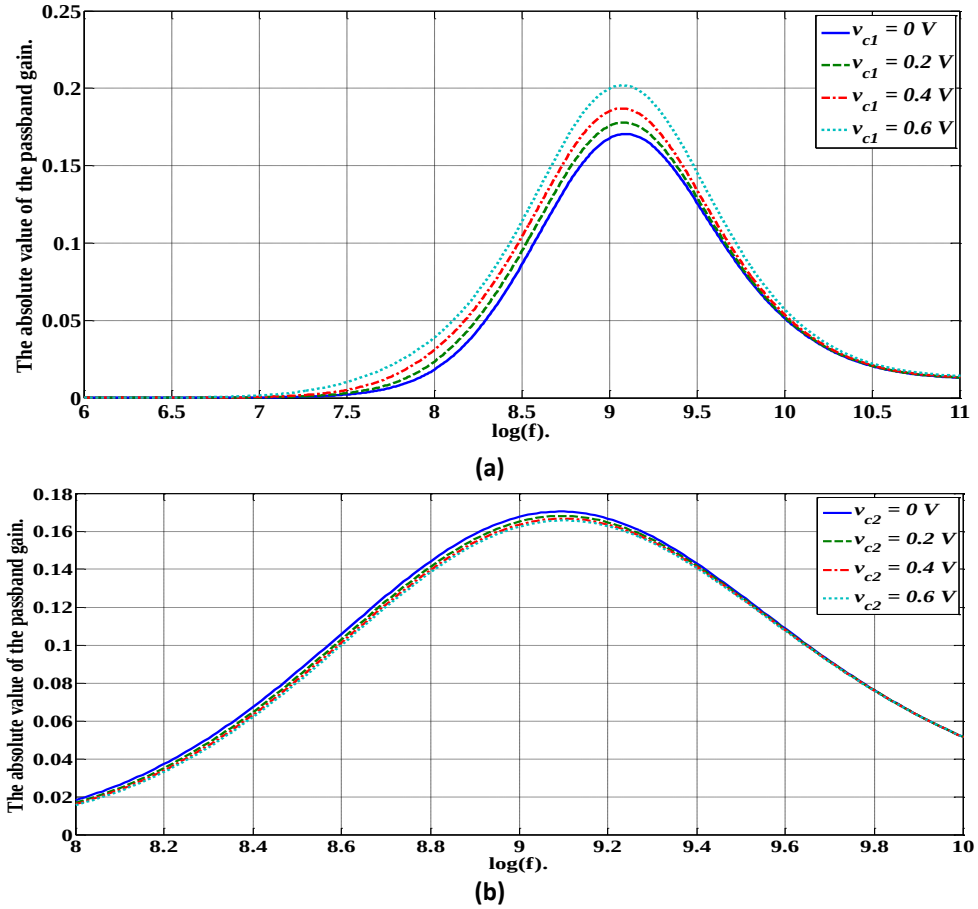

Fig. 18. Plots of the magnitude characteristics of the BPF for different values of: a) v_{c1}; b) v_{c2}.

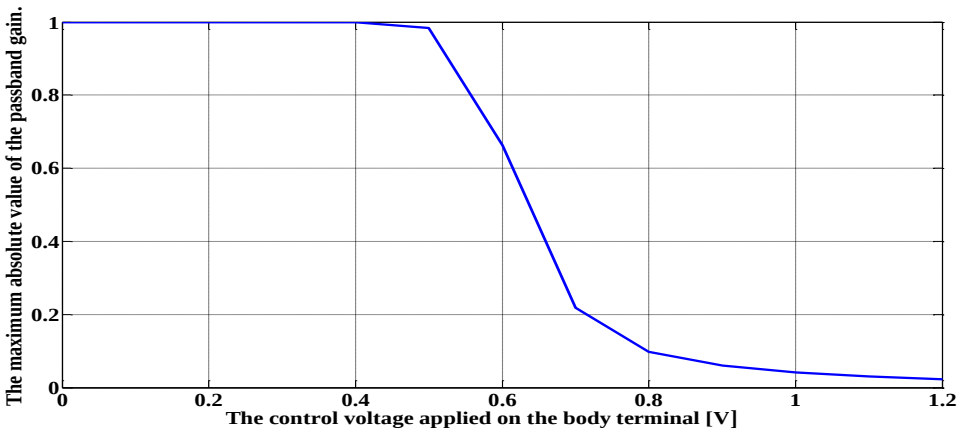

Fig. 19. Maximum absolute value of the passband gain versus the control voltage for the LPF.

5.7.2. Coarse Tuning

Simply stated, connecting several transistors in parallel decreases the effective resistance in the circuit, thus increasing the cutoff frequency. This is confirmed in Fig. 20(a) which shows the plots of the magnitude characteristics of the lowpass filter for several parallel connected devices acting as resistors. The same idea can be applied equally well on the other three filter types. The corresponding plots are shown in Figs. 20(b), (c), and (d). The parallel connected devices may have the same size or different sizes.

5.8. Power Consumption

In this subsection, the power consumption of the proposed filter is evaluated. It must be noted that the power consumption of the input signal is not estimated; rather, the power consumption of the constituting elements of the filter are of interest. Accordingly, each of the power consumption of the lowpass and the allpass filters is approximately equal to that of the encoder circuit only in the corresponding case. This is certainly due to the negligible gate current of the MOS device. The power consumption of the five filters are as depicted in Table 9 with an average value of 74 μW. Finally, note that the power consumption of the proposed filter is low compared to universal filters especially those operating in the current mode whose power consumption reaches a few milliWatts.

Table 9. Average power consumption of the five filters.

Filter type	Average power consumption [μW]		
	Encoder	Main circuit	Total
Lowpass	30	0	30
Highpass	30	88	118
Bandpass	30	44	74
Bandstop	30	88	118
Allpass	30	0	30

5.9. Comparison

In this subsection, a comparison between the proposed universal filter and previous work is made. For illustartion, refer to Table 10. The number of elements is taken as an evaluation of the area. If a baising current source is required, its area evaluation is assumed to be equal to that of one MOS transistor. The passivity or activity of the filters are judged by the potentiality of obtaining gains larger than 1 (0 dB) not by the nature of the adopted elements. The center frequency of the bandpass filter is chosen here as an evaluation of the range of frequencies of the filter.

Several notes concerning this comparison are in order. The filter of [51] has the lowest power consumption among the adopted filters. This is expected as this filter operates at the smallest power supply that is compatible with its very small frequency of 10 Hz. However, the transistor count adopted therein is relatively large. On the contrary, the scheme of [57] has a relatively large power consumption. This is due to its operation in the current mode and the adopted V_{DD} of ±1 V. Although the number of its realized filtering functions is limited, its transistor count also is limited. The work of [74] has a relatively small power consumption and transistor count; however, the realized filtering functions is limited to the

LP type only. The filter of [85] has the smallest transistor count; however, its filtering functions is limited to three types only.

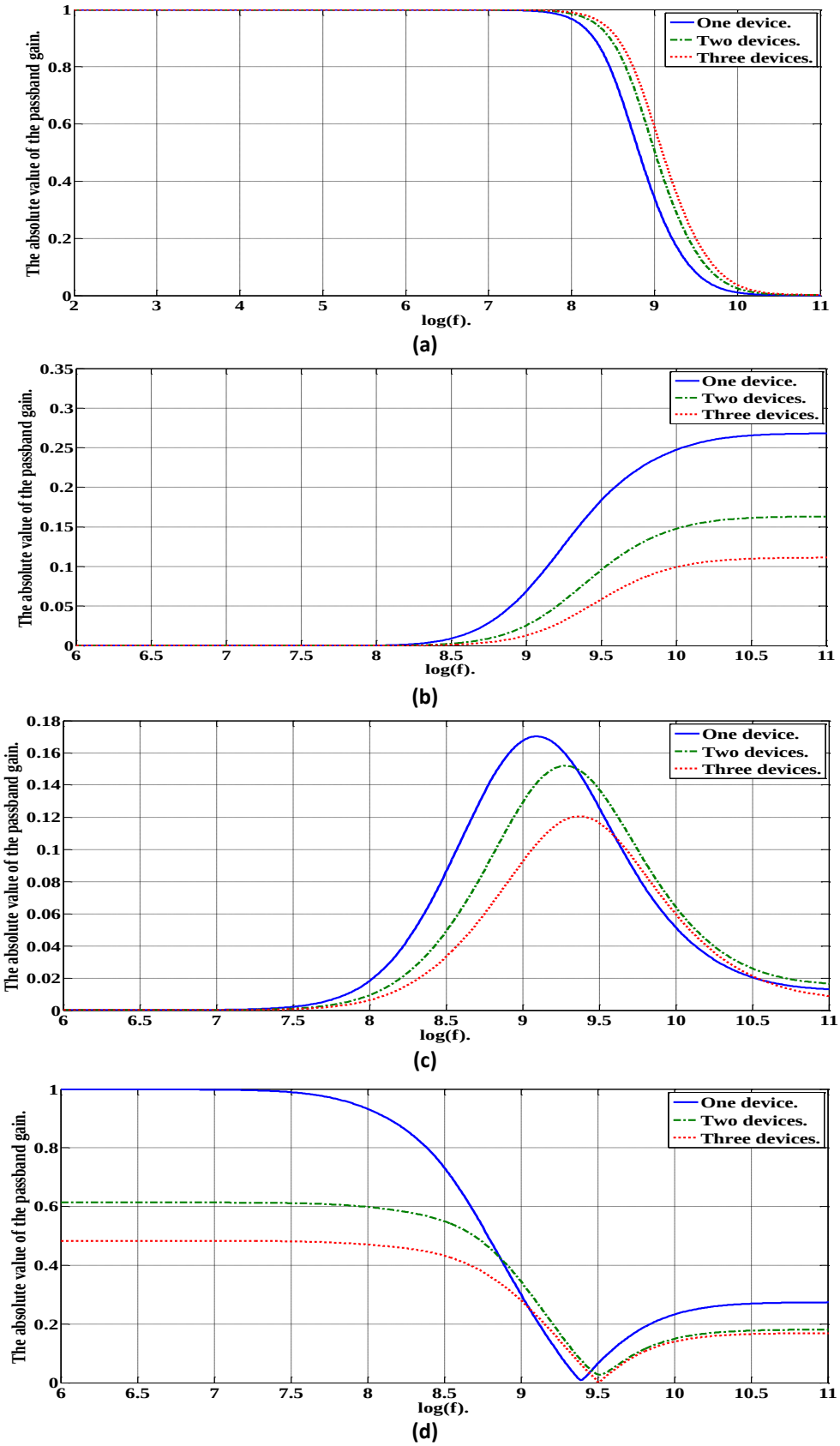

Fig. 20. Magnitude characteristics of the: a) LPF; b) HPF; c) BPF; d) BSF for several parallel connected devices with the same size.

The proposed filter lies in the middle between these types from the points of view of the transistor count and the required power consumption. The proposed filter has the highest center frequency, the lowest THD, and the more flexible tunability. It is also a universal filter with all the filtering functions realized.

Table 10. Comparison between the proposed universal filter and those reported in previous works.

	Ref. [50]	Ref. [51]	Ref. [57]	Ref. [74]	Ref. [84]	Ref. [85]	**The proposed scheme**
Technology [µm]	0.18	0.18	0.25	0.18	0.18	0.25	**0.13**
Power-supply voltage [V]	±0.9	0.5	±1	1.8	±0.9	±1.8	**1.2**
Count of elements	30 transistors and two grounded capacitors	124 transistors, one resistor, and two capacitors	30 transistors, two resistors, and two capacitors	35 transistors and one resistor	36 transistors, 7 resistors, and 10 capacitors	20 transistors and three capacitors	**70 transistors**
Average power consumption [W]	NA*	53.3 n	1.49 m	1.08 µ	0.99 m	NA*	**74 µ**
Center frequency [Hz]	1 M	10	1.6 M	NA*	50 k	10.61 M	**1.23 G**
Filter types	LP, HP, BP, BS, and AP	LP, HP, BP, BS, and AP	LP, HP, and BP	LP	LP, HP, BP, BS, and AP	LP, HP, and BP	**LP, HP, BP, BS, and AP**
Active or passive	Active	Passive	Passive	Active	Passive	Passive	**Passive**
Tunability	Yes	Yes	Yes	Yes	Yes	Yes	**Yes (Coarse and fine tunability)**
Filter mode	Voltage mode	Voltage mode	Voltage and current modes	Voltage mode	Voltage Mode	Voltage and current modes	**Voltage mode**
Suitability for SoC	No	Yes	Yes	Yes	Yes	Yes	**Yes**
THD	0.3% at 240 mV peak	< 1% @ 100 mVpp	NA*	1% @ 55 mVpp	NA*	4% @ 300 mV peak	**0.018% @ 100 mVrms**
Simulated or measured	Simulated	Simulated	Simulated	Simulated	Simulated and measured	Simulated	**Simulated**

*NA = Not available.

6. CONCLUSIONS

In this paper, an all-MOS biquadratic voltage-mode universal filter was proposed. It is the first universal filter that is built using only MOS transistors and can be adapted to any filter type in the real time by a digital control pattern. Also, it has the ability to change the filter parameters such as the cutoff frequencies or the center frequency during operation

either in a continuous manner by control voltages or in a discrete manner by a digital control word. These features of the proposed universal filter can be of great benefit for SoC applications where avoiding the need to fabricate passive elements is appreciated. It can be helpful also in communication systems that may require the ability to change the passband or the cutoff frequencies in a dynamic way in order to avoid interference or jamming or even for security reasons. The validity of the proposed filter was verified by simulation. The effects of the THD, noise, and PVT variations were investigated. The average power consumption of the LP, HP, BP, BS, and AP filters were found to be 30, 118, 74, 118, and 30 (all in μW) which are considered low compared to other universal filters especially those operating in the current domain. The price paid for all these advantages is more sensitivity to process variations for the lowpass filter.

REFERENCES

[1] H. Chen, W. Huang, M. Hsieh, K. Wu, "Universal current mode biquadratic filter with two inputs and four outputs using ICCIIs," *International Conference on Information Science, Electronics and Electrical Engineering*, Sapporo, pp. 233-236, 2014.

[2] M. Ibrahim, S. Minaei, H. Kuntman, "A 22.5 MHz current-mode KHN-biquad using differential voltage current conveyor and grounded passive elements," *International Journal of Electronics and Communication*, vol. 59, pp. 311-318, 2005.

[3] C. Alexander, M. Sadiku, *Fundamental of Electric Circuits*, New Yorks, McGraw-Hill, 2004.

[4] M. Ibrahim, S. Minaei, H. Kuntman, "A 22.5 MHz current-mode KHN-biquad using differential voltage current conveyor and grounded passive elements," *International Journal of Electronics and Communications*, vol. 59, pp. 311-318, 2005.

[5] A. Fabre, F. Dayoub, L. Duruisseau, M. Kamoun, "High input impedance insensitive second-order filters implemented from current conveyors," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 41, no. 12, pp. 918–921, 1994.

[6] J. Horng, J. Lay, C. Chang, M. Lee, "High input impedance voltage-mode multifunction filters using plus-type CCIIs," *Electronic Letters*, vol. 33, no. 6, pp. 472–473, 1997.

[7] A. Kumar, S. Kumar, D. Elkamchouchi, S. Urooj, "Fully differential current-mode configuration for the realization of first-order filters with ease of cascadability," *Electronics*, vol. 11, no. 13, pp. 2072, 2022.

[8] I. Cevik, B. Metin, N. Herencsar, O. Cicekoglu, H. Kuntman, "Transimpedance type MOS-C bandpass analog filter core circuits," *Analog Integrated Circuits and Signal Processing*, vol. 16, no. 3, pp. 543 – 551, 2021.

[9] S. Chinnapark, S. Siripongdee, W. Jaikla, S. Thanaputtiwirot, R. Sotner, S. Moto, "Resistorless transconductance-mode multifunction filter with orthogonal and electronic tune of natural frequency and quality factor," *International Electrical Engineering Congress*, Khon Kaen, Thailand, pp. 1-5, 2022.

[10] C. Toumazou., F. Lidgey, D. Haigh, *Analogue IC Design: The Current-Mode Approach*, London: Peter Peregrinus, 1990.

[11] O. Channumsin, T. Pukkalanun, W. Tangsrirat, "Universal current-mode biquad with minimum components," *Proceedings of the International Multi-Conference of Engineering and Computer Scientists*, 2011.

[12] W. Tangsrirat, T. Pukkalanun, "Structural generation of two integrator loop filters using CDTAs and grounded capacitors," *International Journal of Circuit Theory and Applications*, vol. 39, pp. 31-45, 2011.

[13] W. Jaikla, S. Lawanwisut, M. Siripruchyanun, P. Prommee, "A four inputs single-output current-mode biquad filter using a minimum number of active and passive components," *Proceedings of 35th International Conference on Telecommunications and Signal Processing*, pp. 378-381, 2012.

[14] D. Bhaskar, A. Raj, P. Kumar, "Mixed-mode universal biquad filter using OTAs," *Journal of Circuits, Systems, and Computers*, vol. 29, no. 10, pp. 2050162, 2020.

[15] A. Sedra, K. Smith, *Microelectronic Circuits*, Seventh Edition, Oxford University Press, Oxford, New York, 2015.

[16] T. Carusone, D. Johns, K. Martin, *Analog Integrated Circuit Design*, Second Edition, John Wiley and Sons, USA, 2012.

[17] P. Suksaibul, U. Torteanchai, M. Kumngern, W. Jongchanachavawat, B. Burapattanasiri, S. Lerkvaranyu, "Mixed-mode universal filter using differential difference transconductance amplifiers," *19th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, Prachuap Khiri Khan, Thailand, pp. 1-5, 2022.

[18] P. Suksaibul, U. Torteanchai, S. Manman, W. Jongchanachavawat, M. Kumngernm, S. Lerkvaranyu, "Multiple-input multiple-output universal filter using DDTAs," *International Electrical Engineering Congress (iEECON)*, Khon Kaen, Thailand, pp. 1-4, 2022.

[19] F. Khateb, M. Kumngern, T. Kulej, D. Biolek, "0.5 V differential difference transconductance amplifier and its application in voltage-mode universal filter," *IEEE Access*, vol. 10, pp. 43209–43220, 2022.

[20] M. Kumngern, P. Suksaibul, F. Khateb, T. Kulej, "Electronically tunable universal filter and quadrature oscillator using low-voltage differential difference transconductance amplifiers," *IEEE Access*, vol. 10, pp. 68965–68980, 2022.

[21] Y. Abdullah, F. Kaçar, "Electronically tunable resistorless mixed mode biquad filters," *Radioengineering*, vol. 22, pp. 1016-1025, 2013.

[22] N. Roongmuanpha, T. Pukkalanun, W. Tangsrirat, "Three-input one-output voltage-mode biquadratic filter using single VDBA," *8th International Electrical Engineering Congress*, Chiang Mai, Thailand, pp. 1-4, 2020.

[23] M. Abuelmaatti, A. Bentrcia, "A novel mixed-mode CCII-based filter," *Active Passive Electronic Components*, vol. 27, pp. 197-205, 2004.

[24] M. Siripruchyanun, W. Jaikla, "Three-input single-output electronically controllable dual-mode universal biquad filter using DO-CCCIIs," *Active Passive Electronic Components*, vol. 6, 2007.

[25] L. Zhijun, "Mixed-mode universal filter using MCCCII," *AEU-International Journal of Electronics and Communications*, vol. 63, no. 12, pp. 1072-1075, 2009.

[26] N. Pandey, S. Paul, "Mixed mode universal filter," *Journal of Circuits, Systems, and Computers*, vol. 22, no. 1, pp. 1250064, 2013.

[27] C. Chang, C. Lee, C. Hou, J. Horng, C. Tu, "High-order DDCC-based general mixed-mode universal filter," *IEE Proceedings-Circuits Devices and Systems*, vol. 153, no. 5, pp. 511-516, 2006.

[28] C. Lee, "Independently tunable mixed-mode universal biquad filter with versatile input/output functions," *AEU-International Journal of Electronics and Communications*, vol. 70, no. 8, pp. 1006-1019, 2016.

[29] C. Lee, "Mixed-mode universal biquadratic filter with no need of matching conditions," *Journal of Circuits, Systems, and Computers*, vol. 25, no. 9, pp. 1650106, 2016.

[30] S. Singh, S. Maheshwari, D. Chauhan, "Electronically tunable current/voltage mode universal biquad filter using CCCCTA," *International Journal of Recent Trends in Engineering and Technology*, vol. 3, no. 3, pp. 71-76, 2010.

[31] S. Singh, S. Maheshwari, D. Chauhan, "Novel electronically tunable mixed-mode biquad filter," *Electronics and Signal Processing, Lecture Notes in Electrical Engineering*, vol. 97, pp. 735-742, 2011.

[32] S. Maheshwari, S. Singh, D. Chauhan, "Electronically tunable low-voltage mixed-mode universal biquad filter," *IET Circuits, Devices and Systems*, vol. 5, pp. 149-158, 2011.

[33] S. Singh, D. Chauhan, "A new electronically tunable universal mixed-mode biquad filter," *Journal of Engineering Research*, vol. 4, pp. 45-64, 2016.

[34] H. Chen, "Versatile current-mode universal biquadratic filter using DO-CCIIs," *International Journal of Electronics*, vol. 100, no. 7, pp. 1010-1031, 2013.

[35] C. LEE, "Versatile universal current-mode and transresistance-mode biquadratic filter using two MOCCIIS and grounded passive components," *Journal of Circuits, Systems, and Computers*, vol. 22, no. 1, pp. 1250077, 2013.

[36] D. Singh, S. Paul, "Voltage mode third-order universal filter using a single CCII," *7th International Conference on Signal Processing and Integrated Networks*, Noida, India, pp. 160-165, 2020.

[37] H. Chen, "Versatile tunable current-mode universal biquadratic filter using MO-DVCCs and MOSFET-based electronic resistors," *The Scientific World Journal*, vol. 2014, 2014.

[38] S. Kumari, D. Nand, "DDCC-based MISO type voltage-mode first-order universal filter," *2nd International Conference on Intelligent Technologies*, Hubli, India, pp. 1-6, 2022.

[39] C. Shankar, S. Singh, R. Imam, "SIFO–VM/TIM universal biquad filter using single DVCCTA with fully CMOS realization," *Analog Integrated Circuits and Signal Processing*, vol. 109, pp. 33–46, 2021.

[40] T. Arora, "Realization of current-mode universal filter utilising minimum active elements and only grounded passive components," *7th International Conference on Signal Processing and Integrated Networks*, Noida, India, pp. 681-686, 2020.

[41] I. Rajput, R. Saini, P. Kumar, "Design and optimization of MIMO filter using current conveyor," *2nd International Conference on Advance Computing and Innovative Technologies in Engineering*, Greater Noida, India, pp. 2079-2083, 2022.

[42] Y. Pandey, T. Arora, "A current-mode active filter using VDCCs and only grounded passive elements," *2nd International Conference on Emerging Frontiers in Electrical and Electronic Technologies*, Patna, India, pp. 1-6, 2022.

[43] C. Psychalinos, C. Kasimis, F. Khateb, "Multiple-input single-output universal biquad filter using single output operational transconductance amplifiers," *AEU-International Journal of Electronics and Communications*, vol. 93, pp. 360-367, 2018.

[44] T. Nonthaputha, M. Kumngern, "CMOS single input multiple output universal biquad filter current-mode using Only OTAs," *Przegląd Elektrotechniczny*, vol. 97, no. 11, pp. 64-68, 2021.

[45] M. Mahendra, S. Kumari, M. Gupta, "Low voltage adaptive biased OTA with enhanced slew rate and its application in universal filter," *5th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques*, Mysuru, India, pp.460-465, 2022.

[46] V. Singh, A. Singh, D. Bhaskar, R. Senani, "Novel mixed-mode universal biquad configuration," *IEICE Electron Express*, vol. 2, pp. 548-553, 2005.

[47] E. Yuce, "Fully integrable mixed-mode universal biquad with specific application of the CFOA, *AEU-International Journal of Electronics and Communications*, vol. 64, pp. 304-309, 2010.

[48] N. Shah, M. Malik, "Multifunction mixed-mode filter using FTFNs," *Analog Integrated Circuits and Signal Processing*, vol. 47, pp. 339-343, 2006.

[49] A. Raj, P. Kumar and D. R. Bhaskar, "Multiple-input single-output universal biquad filters using reduced number of OTAs," *International Symposium on Advanced Electrical and Communication Technologies (ISAECT)*, Rome, Italy, pp. 1-4, 2019.

[50] B. Knobnob, P. Suksaibul, M. Kumngern, "Five-input one-output universal filter using simple CMOS OTAs," *4th International Conference on Electrical, Electronics and System Engineering*, Kuala Lumpur, Malaysia, pp. 87-90, 2018.

[51] W. Jaikla, F. Khateb, M. Kumngern, T. Kulej, R. Ranjan, P. Suwanjan, "0.5 V fully differential universal filter based on multiple input OTAs," *IEEE Access*, vol. 8, pp. 187832–187839, 2020.

[52] M. Kumngern, T. Nonthaputha, K. Klangthan, "CMOS programmable universal filter using CCTAs," *2nd International Conference on Automation, Cognitive Science, Optics, Micro Electro--Mechanical System, and Information Technology*, Jakarta, pp. 115-118, 2017.

[53] B. Wilson, "Recent developments in current conveyor and current mode circuits," *Proceedings of IEE*, vol. 137, no. 2, pp. 63–77, 1990.

[54] N. Roongmuanpha, M. Faseehuddin, N. Herencsar, W. Tangsrirat, "Tunable mixed-mode voltage differencing buffered amplifier-based universal filter with independently high-Q factor controllability," *Applied Sciences*, vol. 11, no. 20, pp. 9606, 2021.

[55] W. Chiu, J. Horng, "Voltage-mode biquadratic filters with one input and five outputs using two DDCCs," *Indian Journal of Engineering and Materials Sciences*, vol. 18, pp. 97-101, 2011.

[56] W. Jongchanachavawat, M. Kumngern, S. Lerkvaranyu, "Voltage/current-mode universal filter using single FDCCII," *16th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, Pattaya, Chonburi, Thailand, pp. 705-708, 2019.

[57] O. Channumsin, W. Tangsrirat, "Compact dual-mode SITO universal filter and quadrature oscillator with only single VDGA," *17th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, Phuket, Thailand, pp. 181-184, 2020.

[58] H. Chen, "Current-mode dual-output ICCII-based tunable universal biquadratic filter with low-input and high-output impedances," *International Journal of Circuit Theory and Applications*, vol. 42, no. 4, pp. 376–393, 2012.

[59] M. Wai, W. Jaikla, P. Suwanjan, W. Sunthonkanokpong, "Single input multiple output voltage mode universal filters with electronic controllability using commercially available ICs," *17th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, Phuket, Thailand, pp. 607-610, 2020.

[60] B. Chaturvedi, J. Mohan, A. Kumar, "Resistorless realization of first-order current mode universal filter," *Radio Science*, vol. 55, no. 1, pp. 1–10, 2020.

[61] D. Shukla, S. Tripathi, "Design of VDTA based tuneable universal filters," *IEEE Students Conference on Engineering & Systems*, Prayagraj, India, pp. 1-3, 2020.

[62] S. Kadjantuk, S. Laojum, A. Jantakun, P. Saokaew, K. Patimaprakorn, J. Budboonchu, "Mixed-mode universal filter using MCDCTA and grounded capacitors," *International Electrical Engineering Congress*, Khon Kaen, Thailand, pp. 1-4, 2022.

[63] M. Albrni, F. Mohammad, N. Herencsar, J. Sampe, S. Ali, "Novel electronically tunable biquadratic mixed-mode universal filter capable of operating in MISO and SIMO configurations," *Journal of Microelectronics, Electronic Components and Materials*, vol. 50, no. 3, pp. 189–203, 2020.

[64] M. Faseehuddin, N. Herencsar, M. Albrni, J. Sampe, "Electronically tunable mixed-mode universal filter employing a single active block and a minimum number of passive components," *Applied Sciences*, vol. 11, no. 1, pp. 55, 2021.

[65] A. Toker, S. Ozozguz, "Integrable current-mode filter realization using dual-output current conveyors for low-frequency operation," *International Journal of Electronics and Communications*, vol. 55, no. 2, pp. 145–149, 2001.

[66] O. Cicekoglu, N. Tarim, H. Kuntman, "Wide dynamic range high output impedance current-mode multifunction filters with dual-output current conveyors," *International Journal of Electronics and Communications*, vol. 56, no. 1, pp. 55–60, 2002.

[67] O. Cicekoglu, "High output impedance current-mode four-function filter with reduced number of active and passive elements using the dual output current conveyor," *Analog Integrated Circuits and Signal Processing*, vol. 28, no. 2, pp. 201–204, 2001.

[68] J. Horng, C. Hou, C. Chang, W. Chiu, C. Liu, "Current-mode universal biquadratic filter with five inputs and two outputs using two multi-output CCIIs," *Circuit, Systems, and Signal Processing*, vol. 28, no. 5, pp. 781–792, 2009.

[69] K. Abdalla, D. Bhaskar, R. Senani, "Configuration for realising a current-mode universal filter and dual-mode quadrature single resistor controlled oscillator," *IET Circuits, Devices and Systems*, vol. 6, no. 3, pp. 159–167, 2012.

[70] J. Pérez-Bailón, A. Márquez, B. Calvo, N. Medrano, "A 0.18µm CMOS widely tunable low pass filter with sub-Hz cutoff frequencies," *IEEE International Symposium on Circuits and Systems*, Florence, pp. 1-4, 2018.

[71] J. Pérez-Bailón, B. Calvo, N. Medrano, "A CMOS low pass filter for SoC lock-in-based measurement devices," *Sensors*, vol. 19, no. 23, pp. 5173, 2019.

[72] M. Dar, N. Kant, F. Khanday, C. Psychalinos, "Fractional-order filter design for ultra-low frequency applications," *IEEE International Conference on Recent Trends in Electronics, Information and Communication Technology*, Bangalore, pp. 1727-1730, 2016.

[73] J. Pérez-Bailón, A. Márquez, B. Calvo, N. Medrano, M. Sanz-Pascual, "A 1V–1.75µW Gm-C low pass filter for bio-sensing applications," *IEEE 9th Latin American Symposium on Circuits and Systems*, Puerto Vallarta, pp. 1-4, 2018.

[74] J. Pérez-Bailón, B. Calvo, N. Medrano, J. Ramírez-Angulo, "A 1.8 V Gm-C highly tunable low pass filter for sensing applications," *IEEE International Instrumentation and Measurement Technology Conference*, Dubrovnik, Croatia, pp. 1-5, 2020.

[75] N. Arora, *MOSFET Modeling for VLSI Simulation: Theory and Practice*, World Scientific, New Jersey, 2007.

[76] Y. Tsividis, C. McAndrew, *Operation and Modeling of the MOS Transistor*, Third Edition, Oxford University Press, New York, 2011.

[77] D. Hariton, "Floating MOS capacitor," United States Patent 5,926,064, 1999.

[78] B. Razavi, *Design of Analog CMOS Integrated Circuits*, Second Edition, McGraw-Hill, New York, 2017.

[79] H. Shichman, D. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuit," *IEEE Journal of Solid-State Circuits*, vol. sc-13, no. 3, pp. 285-289, 1968.

[80] N. Weste, D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Fourth Edition, Addison-Wesley, Boston, 2011.

[81] S. Sharroush, Y. Abdalla, "Parameter extraction and modeling of the MOS transistor by an equivalent resistance," *Mathematical and Computer Modelling of Dynamical Systems*, vol. 27, no. 1, pp. 50-86, 2021.

[82] R. Schaumann, M. Valkenburg, *Design of Analog Filters*, Second Edition, Oxford University Press, New York, 2001.

[83] Nanoscale Integration and Modeling (NIMO) Group, ASU, "Berkeley Predictive Technlology Model (BPTM)," *Nanoscale Integration and Modeling (NIMO) Group*, 2007. <http://ptm.asu.edu/modelcard/2006/130nm_bulk.pm>

[84] W. Jaikla, F. Khateb, T. Kulej, K. Pitaksuttayaprot, "Universal filter based on compact CMOS structure of VDDDA," *Sensors*, vol. 21, no. 5, pp. 1683, 2021.

[85] P. Mongkolwai, W. Tangsrirat, "Electronically controllable resistorless dual-mode multifunction filter," *Proceedings of the International MultiConference of Engineers and Computer Scientists*, vol. 2, Hong Kong, 2017.