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A Fully MOSFET Voltage Reference with Low Power Consumption and High Power Supply Rejection Ratio for IoT Microsystems

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***Abstract*—** In this work, a fully MOSFET voltage reference (FMVR) circuit with a current consumption of 7.6 nA and a supply voltage of 1 V is proposed. To generate the complementary to absolute temperature (CTAT) voltage, the voltage of a PN junction generated by a PMOS transistor - which is part of the bias circuit - is used. Generation of proportional to absolute temperature (PTAT) voltage is carried-out by utilizing three stages of self-cascode transistors biased in the sub-threshold region. A fraction of the CTAT voltage is added to the PTAT voltage without using an additional circuit to enable acquiring an output reference voltage of about 0.648 V with minimal temperature dependence. The proposed voltage reference is simulated in 0.18 µm of CMOS process and its area occupation is 0.0023 mm^2. The obtained post-layout simulation results demonstrate that the proposed FMVR has a temperature coefficient equivalent to 12.9 ppm/°C under the temperature variation from -25 °C to 120 °C. Moreover, the line regulation under supply voltage variation from 0.9 V to 2 V is found to be equal to 0.02 %/V, and a power supply rejection ratio of 44 dB is acquired. Comparing the main parameters of the proposed FMVR - to the state-of-the-art circuits - shows that it has higher efficiency with smaller area and lower power consumption.

***Keywords*—** Fully MOSFET voltage reference; Temperature coefficient; Proportional to absolute temperature; Complementary to absolute temperature; Line regulation; Power supply rejection ratio.

1. INTRODUCTION

Recently with the development of technology, internet of things (IoT) and the need for using wireless applications in different industries such as medical fields, the design of low power circuits and blocks has been considered significantly. Voltage reference circuit is one of the basic blocks in designing regulator, limiter and sensor circuits. Therefore, in designing voltage reference circuits, in addition to considering features such as temperature coefficient (TC) and line regulation (LR), reduction of power consumption is of particular significance. The voltage reference circuit provides an output voltage (V_{ref}) that is not sensitive to power supply (V_{DD}) variation, temperature, and the manufacturing process. Temperature-independent V_{ref} is often obtained by the balanced sum of two voltages with opposite TC, proportional to absolute temperature (PTAT) voltage and complementary to absolute temperature (CTAT) voltage [1]. The CTAT voltage is usually provided by the base-emitter (V_{BE}) of a bipolar junction transistor (BJT) or the gate-source voltage (V_{GS}) of a metal–oxide–semiconductor field-effect transistor (MOSFET) operating in the sub-threshold region, while the PTAT voltage can be generated by the difference between the two V_{BE} or V_{GS} voltages of the transistors [2].

Since power consumption is among the main challenges of IoT microsystems, voltage references based on MOSFETs with sub-threshold operating region and without using BJTs

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have recently received much attention and substantial development [3, 4]. Basically, the main reason for such an achievement by this type of circuits can be referred to their ability for operating at low supply voltage and very low power consumption [5-7]. However, since the threshold voltage (V_{TH}) in MOSFET changes with process variations, various problems may arise [8, 9]. Hence, due to the tendency for utilizing MOSFETs in voltage reference circuits, the presence of large resistors becomes inevitable, which increases the chip area and power consumption significantly [10-13].

In some voltage reference circuits, Schottky diode is used to lower the supply voltage and power consumption as much as possible. It should be noted that despite the lower voltage drop of Schottky diode compared to conventional silicon diodes, it is an inappropriate option due to both its disability for complying with CMOS technology and its high manufacturing cost [14].

In [15, 16], the all-MOSFET voltage reference is presented. It uses the V_{TH} difference of transistors with various oxide thicknesses to acquire the CTAT and PTAT voltages. However, it should be noted that using this technique increases the cost of bandgap voltage reference (BGR) fabrication, and gives undesirable power consumption. Therefore, diverse structures - without using resistors and with low voltage and power - have been proposed. They are characterized by that their MOSFETs operate in the sub-threshold region and can have slight current [17-21].

In this paper, a MOSFET - in which its source, drain and gate terminals are connected - is used as a PN junction to provide V_{CTAT}. To achieve the desirable reference voltage, two identical MOSFETs are used to decrease the V_{CTAT} voltage level. The PTAT section is also provided by three stages of cascode circuit. As principal benefits of the offered circuit, small area occupation, low power dissipation and high power supply rejection ratio (PSRR) can be mentioned. The organization of the paper is as following: in section 2 along with the configuration of the presented fully MOSFET voltage reference (FMVR), the functionality of the PTAT and CTAT voltage generators are comprehensively investigated. Section 3 provides the post-layout simulation outcomes for the proposed FMVR. Eventually, the paper is concluded in section 4.

2. THE PROPOSED FMVR CIRCUIT

The proposed FMVR circuit is exhibited in Fig. 1. In this circuit, a PMOS transistor - with gate, source, and drain terminals connected together - operates as a diode under direct bias mode, and it is used as a CTAT voltage generator. V_D is the CTAT voltage generated by M_1 (which is equivalent to the V_{GS} of two NMOS transistors), M_2 and M_3. V_{GS} is defined using the current 'I' and the dimensional ratio of the transistors. Due to the equal drain current and dimensions in M_2 and M_3, the CTAT voltage produced on the M_2 diode junction transistor is equal to half the value of V_D. The PTAT voltage is supplied by three stages of self-cascode (M_3-M_4, M_5-M_6 and M_7-M_8). The power consumption is declined owing to the operation of PTAT and CTAT transistors in the sub-threshold region.

2.1. Bias Circuit and CTAT Voltage Generator

CTAT voltage is obtained by a PMOS transistor in which its drain, source and gate terminals are connected. In this case, according to Fig. 2, due to the connection of the body to

ground and the connection of source, drain and gate to non-zero positive voltage, the created diodes are in direct bias mode. From this connection, if a sufficient voltage difference is provided, a diode voltage drop can be obtained. In direct bias, the current-voltage characteristic of this structure can be depicted as in Fig. 3. It is clear that if the diodes are ON for a specific voltage, increasing or decreasing of length (L) of transistor has no influence on the current flowing through the diode, but the higher the width of the transistor (W), the more current passes. According to Eq. (1), for a constant voltage, the higher the W, the larger the cross-sectional area of the PN junction and, consequently, the larger I_S ($I_S = J_S.A$), where Js and A are current density and cross-sectional area of the transistor ($A \propto W$), respectively [1].

$$I_D = I_S exp\left(\frac{V_D}{V_T}\right) \quad (1)$$

where, I_D is diode current, I_S and V_D are reverse saturation current and voltage drop across the diode, respectively. V_T is the thermal voltage that equals k_BT/q, where k_B, T and q are Boltzmann constant, absolute temperature and electron charge, respectively. In the proposed reference voltage, the ratio of (W/L) for the transistor that operates as a diode is considered 0.5 µm / 0.5 µm. Since transistor M_1 has the same function as a diode, the V_D relation can be expressed as:

$$V_D = V_T ln\frac{I_D}{I_S} \quad (2)$$

By deriving in terms of temperature, it is possible to measure the TC of V_D as:

$$\frac{\partial V_D}{\partial T} = \frac{k}{q} ln\frac{I_D}{I_S} - \frac{V_T}{I_S} \cdot \frac{\partial I_S}{\partial T} \quad (3)$$

The saturation current I_S is proportional to $\mu kT\ n_i^2$, where μ denotes the mobility of minority carriers and n_i is the intrinsic carrier concentration of Silicon. The temperature dependence of these quantities is represented as $\mu \propto \mu_0 T^m$ ($m \approx -3/2$), and $n_i^2 \propto T^3 \exp[-E_g/(kT)]$ [1]. Thus, I_S in terms of temperature is defined as:

$$I_S = bT^{4+m} exp\left(\frac{-E_g}{kT}\right) \quad (4)$$

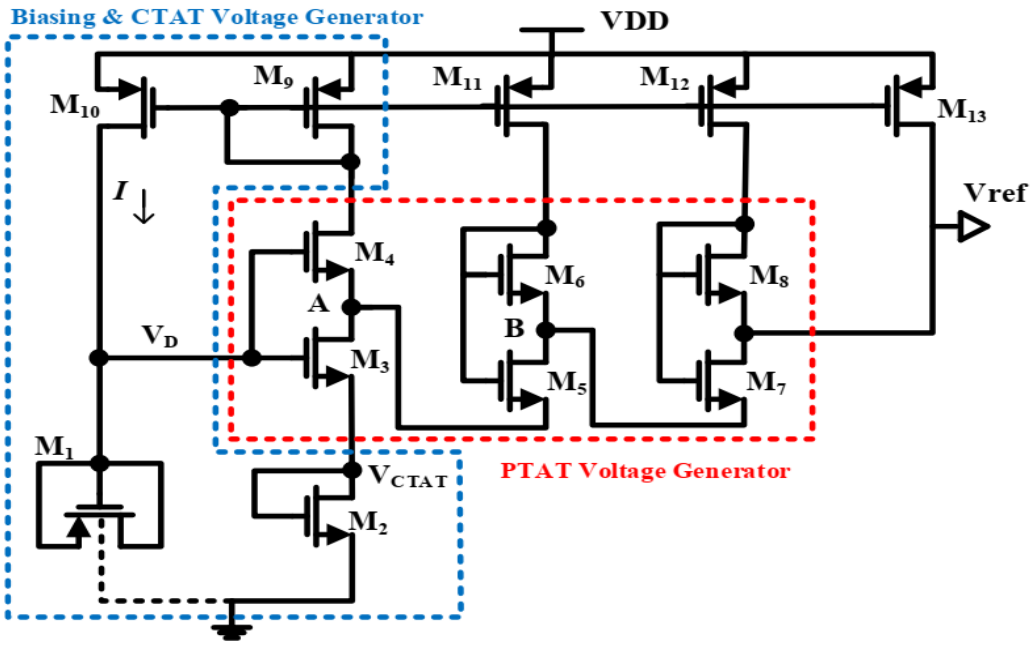

Fig. 1. Structure of the proposed voltage reference circuit.

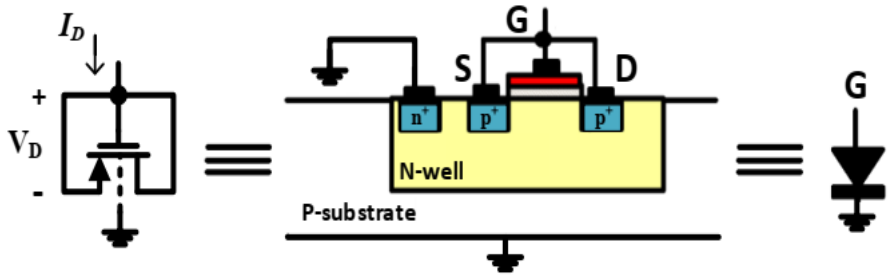

Fig. 2. The diode created using a PMOS transistor.

The I_S derivative in terms of temperature is expressed as:

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m}exp\left(\frac{-E_g}{kT}\right) + \frac{E_g}{kT^2}bT^{4+m}exp\left(\frac{-E_g}{kT}\right) \quad (5)$$

where b is the coefficient of proportionality and Eg is the bandgap energy. Using Eqs. (4) and (5) and placing them in Eq. (3), the TC relationship of V_D is obtained as expressed by Eq. (6). This equation declare that the voltage drop across transistor M_1 (PMOS) is inversely related to temperature and indicates that V_D is CTAT.

$$\frac{\partial V_D}{\partial T} = \frac{V_D - (4+m)V_T - {}^{E_g}/_q}{T} < 0 \quad (6)$$

Fig. 4 shows the V_D voltage performance in terms of temperature. According to Eq. (2), for a constant current, the higher the W of the transistor, the lower the V_D, which is due to the increase in I_S. It can be concluded – as exhibited in Fig. 4 - that to design and achieve the different voltage levels V_D, W of transistor M_1 can be changed. Since M_2 and M_3 are chosen exactly the same and $V_D = V_{GS3} + V_{GS2}$, then the CTAT voltage can be expressed as:

$$V_{CTAT} = V_{GS2} = \frac{V_D}{2} \quad (7)$$

Given the point that transistors M_2 and M_3 operate in the sub-threshold region, the current of M_2 can be calculated based on the current relationship in the sub-threshold region. Also, according to Fig. 1, the current passing through M_2 can be related to the dimensional ratio of transistors M_9, M_{11}, M_{12} and M_{13}.

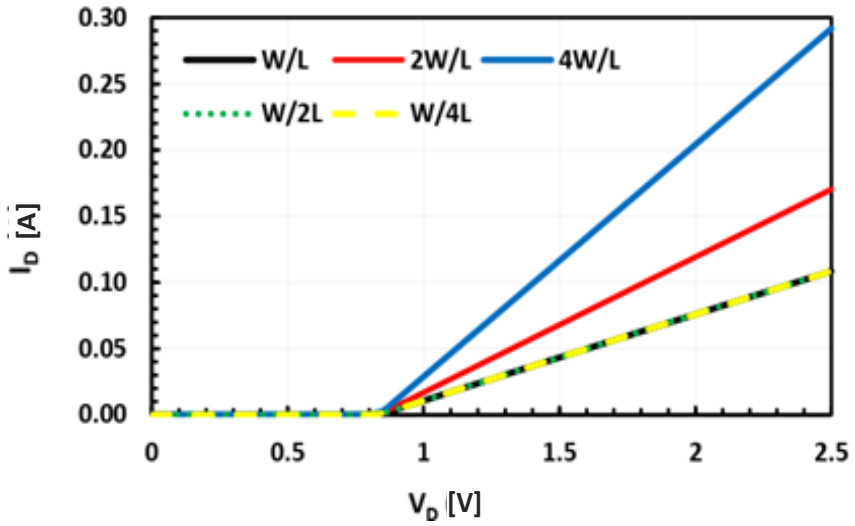

Fig. 3. Current-voltage characteristic of the diode created using a PMOS transistor.

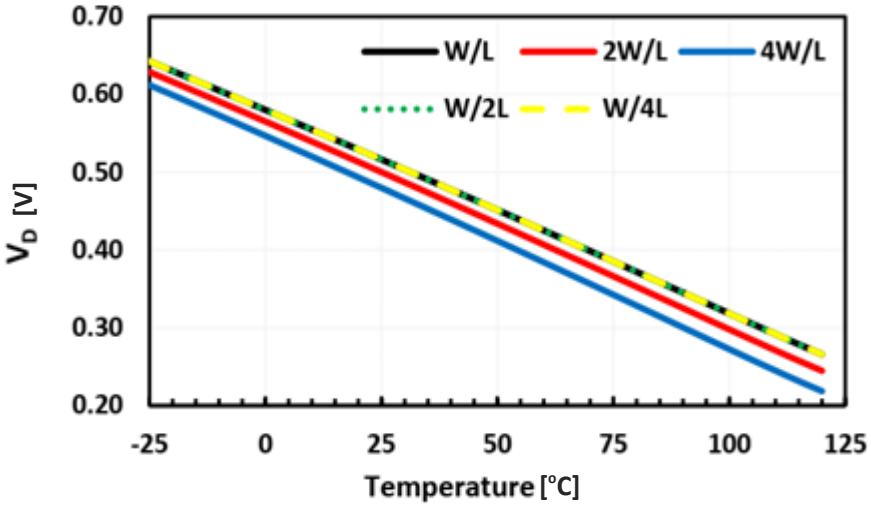

Fig. 4. V_D characteristics in terms of temperature.

2.2. PTAT Voltage Generator

In this voltage reference, the production of the PTAT voltage is achieved using a cascade of self-cascode MOSFET structure. Since all MOSFET transistors - including the transistors used in the PTAT section - operate in the sub-threshold region, if $|V_{DS}|$ of a MOSFET is greater than $4V_T$, the sub-threshold I_D current is almost independent of V_{DS} and is expressed as [2]:

$$I_D = K\mu C_{OX} V_T^2 (\eta - 1) exp\left[\frac{(|V_{GS}| - |V_{TH}|)}{(\eta V_T)}\right] \quad (8)$$

where K (K=W/L) is the aspect ratio of the MOSFET, μ is carrier mobility, C_{OX} is the oxide capacitance and η is sub-threshold slope factor.

In the PTAT voltage generator cascade structure, the PTAT voltage proportional to the thermal potential, is obtained from the sum of the difference between the gate-source voltages of the cascode transistors or the drain-source voltage of the transistors below them. By adjusting the current and dimensional ratios of the transistors (K), the first stage PTAT voltage can be defined using Eq. (8) as:

$$V_{PTAT(first\ stage)} = V_{DS,M3} = \eta V_T \ln\left(\frac{I_{M3}}{I_{M4}} \cdot \frac{K_{M4}}{K_{M3}}\right) \quad (9)$$

The proposed voltage reference uses three self-cascode MOSFET structures (transistors M_3 to M_8) that produce the PTAT voltage as:

$$V_{PTAT,total} = V_{DS,M3} + V_{DS,M5} + V_{DS,M7} \quad (10)$$

Therefore, the output of the voltage reference can be measured based on the sum of the CTAT voltage calculated in Eq. (7) and the PTAT voltage obtained from Eq. (10). Eq. (11) indicates the output of the voltage reference. The implication of TC is shown in Eq. (12):

$$V_{ref} = V_{CTAT} + V_{PTAT,total} = \frac{V_D}{2} + \left(V_{DS,M3} + V_{DS,M5} + V_{DS,M7}\right) \quad (11)$$

$$TC = \frac{\partial V_{ref}}{\partial T} = \frac{\partial V_D}{2\partial T} + \frac{\partial}{\partial T}\left(V_{DS,M3} + V_{DS,M5} + V_{DS,M7}\right)$$
$$= \frac{V_D - (4+m)V_T - {E_g}/{q}}{2T} + \eta \frac{V_T}{T} \ln\left(\frac{I_{M3}}{I_{M4}}\frac{I_{M5}}{I_{M6}}\frac{I_{M7}}{I_{M8}} \cdot \frac{K_{M4}}{K_{M3}}\frac{K_{M6}}{K_{M5}}\frac{K_{M8}}{K_{M7}}\right) \quad (12)$$

By proper selection of the current and dimensions of the transistors in the PTAT section, low and near to zero TC can be obtained. As a result, by using the PTAT cascade of self-cascode MOSFET structures in the second part of Eq. (11), the negative TC of the CTAT

voltage can be neutralized and a temperature-independent reference voltage can be generated. The dimensions of the proposed BGR transistors are given in Table 1.

Table 1. The size of the components used in the proposed FMVR.

Transistor	multiplier×W [µm]×finger/L[µm]	Transistor	multiplier×W [µm]×finger/L[µm]
M_1	1×0.5×1/0.5	M_8	2×12×5/3.5
M_2	1×4×1/2	M_9	1×2×1.5
M_3	1×4×1/2	M_{10}	1×13×1/3
M_4	2×9×5/3	M_{11}	1×5×1/5
M_5	1×2×1/2	M_{12}	1×3×1/1
M_6	2×6×5/1.5	M_{13}	1×20×1/4.5
M_7	1×2×1/2		

3. POST-LAYOUT SIMULATION RESULTS

In this paper, the simulations are carried out using Cadence in 0.18 µm CMOS technology. Fig. 5 demonstrates the voltage of the proposed FMVR nodes versus temperature in the range of -25 °C to 120 °C with a supply voltage of 1 V. As can be seen, the CTAT voltage generated on transistor M_2 (V_{CTAT}) is approximately half the voltage generated (V_D) by transistor M_1 and is in the range of 0.25 V (at 27 °C). In this case, by adding three stages of PTAT self-cascode voltage generator to CTAT voltage, a temperature-independent voltage is generated.

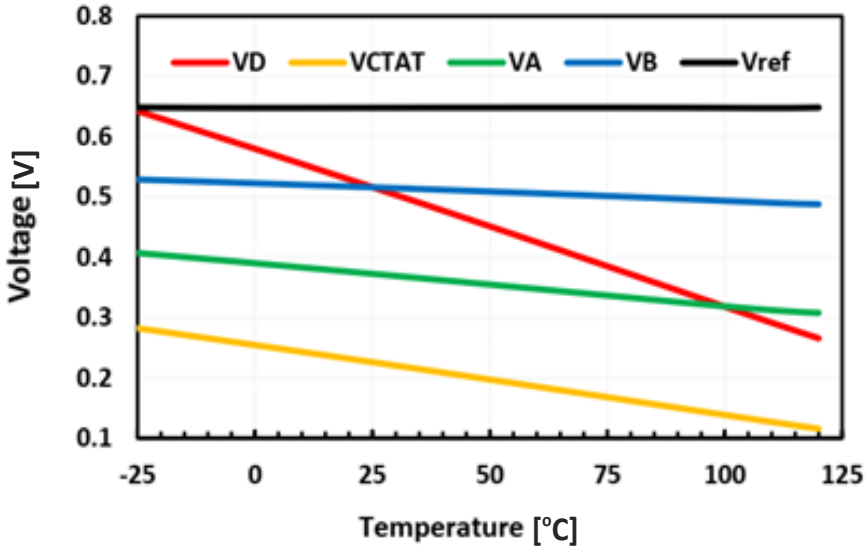

Fig. 5. Voltage characteristic of the main nodes of the proposed voltage reference in terms of temperature.

Fig. 6 shows the voltage reference output in terms of temperature - varied from -25 °C to 120 °C - with a supply voltage of 1 V for simulation in schematic and post layout mode. The reference voltage obtained in intended temperature interval varies around 0.00075 V. Considering that the FMVR output is about 0.648 V, the obtained TC - based on Eq. (13) [14] - in the schematic and post-layout simulations is 11.9 ppm/°C and 12.9 ppm/°C, respectively.

$$TC = \frac{V_{ref_{max}} - V_{ref_{min}}}{(T_{max} - T_{min}) V_{ref(27°C)}} \cdot 10^6 \left[\frac{ppm}{°C}\right] \quad (13)$$

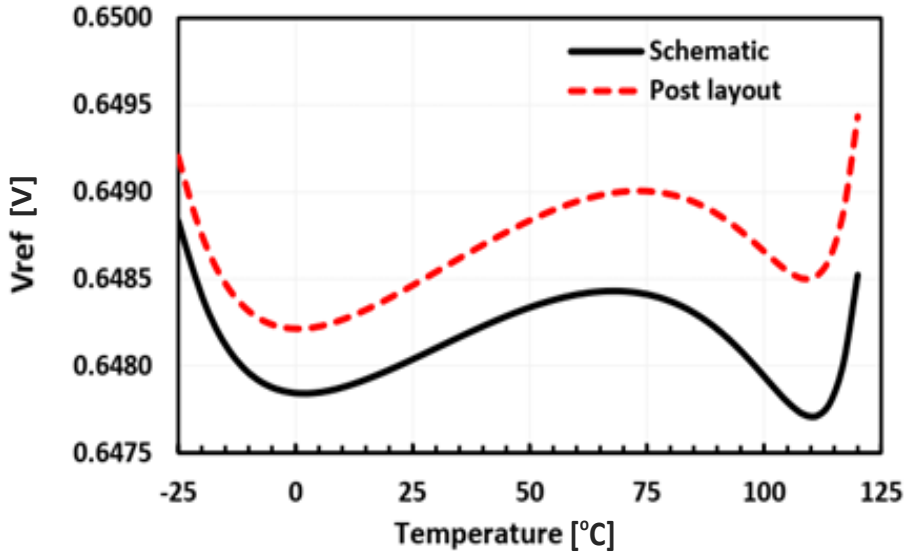

Fig. 6. Reference voltage variations versus temperature.

The output voltage characteristic in schematic and post layout simulations versus power supply variation from 0 V to 2 V is shown in Fig. 7. In this case, the results of the post layout are almost identical to the schematic outcomes. The LR according to Eq. (14) [16], for V_{DD} in the range of 0.9 V to 2 V has been calculated to be 0.02 %/V. Due to the independence of bias current I from the power supply, low LR is obtained.

$$LR = \frac{\Delta V_o}{\Delta V_i . V_o} . 100\%/V \quad (14)$$

Current consumption of the FMVR in terms of temperature is depicted in Fig. 8. It shows that the current consumption of voltage reference is almost independent of temperature. Since the proposed voltage reference is supplied with 1 V, its power consumption - as a result - is also independent of temperature and operates by changing the temperature in a certain range.

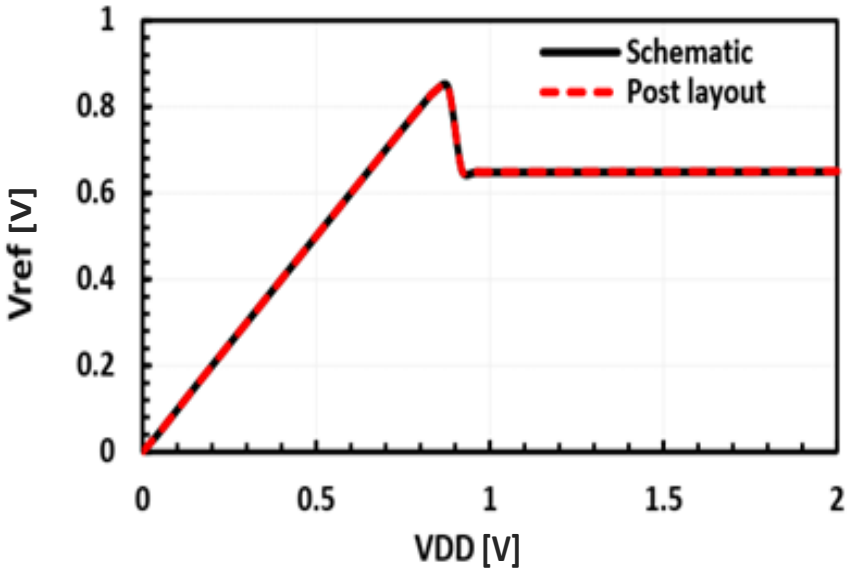

Fig. 7. Reference voltage characteristic in terms of power supply voltage.

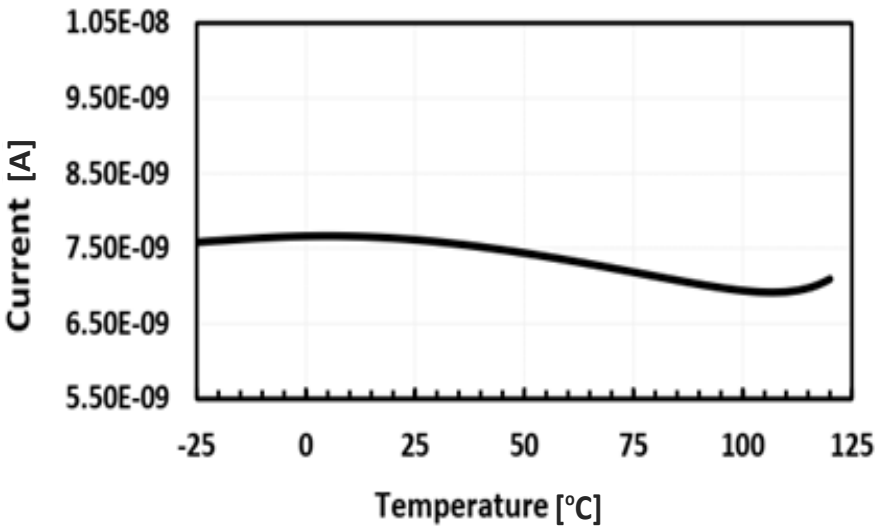

Fig. 8. FMVR current consumption characteristic in terms of temperature.

The impact of the fabrication process on circuit performance by Monte Carlo analysis - taking into account the process variations and mismatches for 1000 runs - are shown in Fig. 9. The mean (μ) and standard deviation (σ) of the reference voltage (V_{ref}) are 0.6482 V and 0.0068 V, respectively, while the value of the coefficient of variation (σ/μ) attained about 0.010.

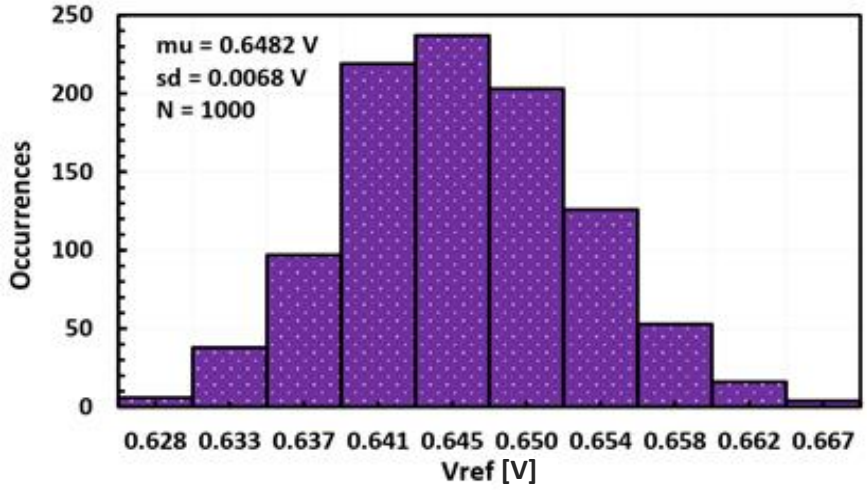

Fig. 9. Monte Carlo analysis for V_{ref} under 1000 runs.

Fig. 10 shows the output voltage variations in five considered corners analysis, namely typical NMOS- typical PMOS (tt), fast NMOS- fast PMOS (ff), slow NMOS- slow PMOS (ss), fast NMOS- slow PMOS (fs) and slow NMOS- fast PMOS (sf) for the temperature range of -25 °C to 120 °C. The results of the corner simulation for V_{ref} in five different modes for the supply voltage 1 V show that the V_{ref} varies from 0.625 V to 0.670 V at 27 °C. Moreover, Fig. 11 shows the measured output voltage in terms of temperature variation from -25 °C to 120 °C with power supplies 1 V, 1.2 V, 1.5 V, 1.8 V and 2 V. Hence, regarding diverse power supplies, the TC is acceptable and equal to 12.9 ppm/°C, 24.6 ppm/°C, 29.6 ppm/°C, 34 ppm/°C and 37.8 ppm/°C, respectively.

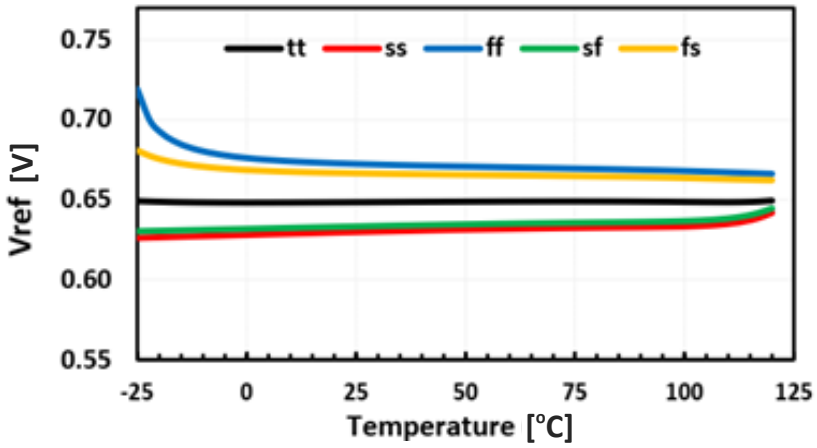

Fig. 10. Output voltage variations in corner analysis for a temperature range of -25 °C to 120 °C.

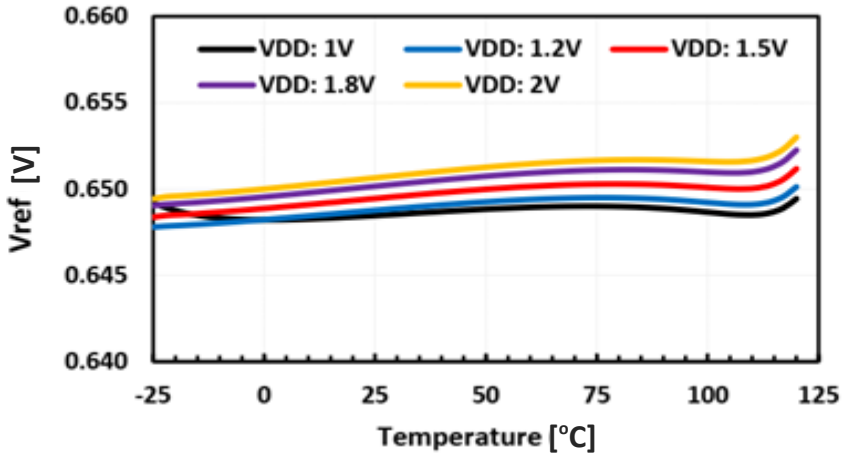

Fig. 11. Reference voltage variations with temperature under different supply voltages.

Fig. 12 illustrates the simulated PSRR of the proposed voltage reference at room temperature. The PSRR is a measurement of a circuit's power supply rejection expressed as a log ratio of output noise to input noise. The PSRR is defined as:

$$PSRR = 10\log\left(\frac{\Delta V_{Supply}^2 A_v^2}{\Delta V_{ref}^2}\right) \quad [dB] \tag{15}$$

where A_V is the voltage gain. On this subject, the PSRR attained with the supply voltage 1 V is -56 dB and -44 dB at 10 Hz and 100 Hz, respectively.

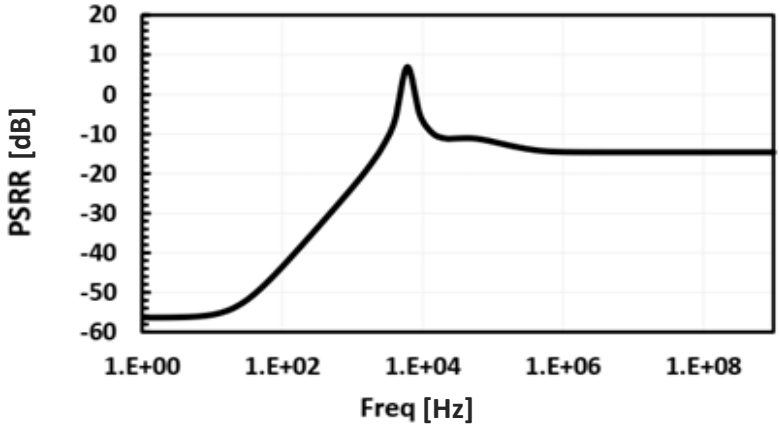

Fig. 12. Simulated PSRR of the proposed voltage reference.

The proposed voltage reference layout with a total area of 0.0023 mm² can be seen in Fig. 13. Table 2 provides the main specifications of the proposed voltage reference cell compared to the state-of-the-art low-power and without resistors voltage reference circuits. In order to compare the performance of the proposed circuits with the state-of-the-art designs, a Figure of Merit (FoM) that considers the main performance parameters of a voltage reference, such as temperature range, TC, power, and layout area, is used. It can be expressed as [22]:

$$FoM = \frac{(T_{MAX}-T_{MIN})^2}{TC \times Power \times Area} \times \frac{1}{10^{21}} \quad [°C^3/\mathrm{W} * \mathrm{mm}^2] \tag{16}$$

The results of Table 2 prove the higher efficiency with smaller area and lower power consumption of the proposed circuit compared to other designs.

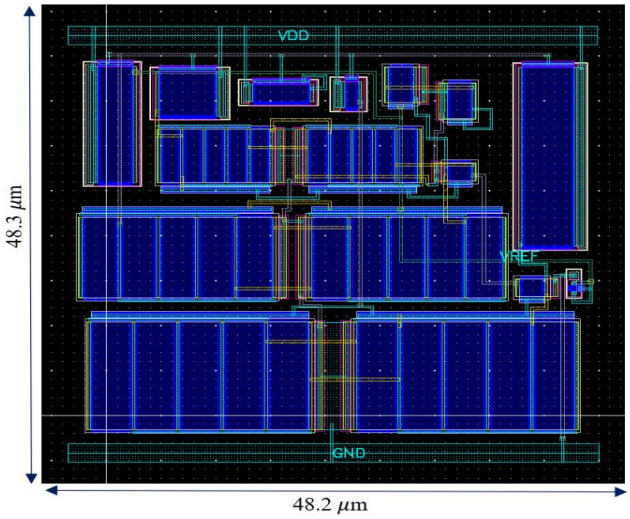

Fig. 13. Layout of proposed voltage reference.

Table 2. Main parameters of the proposed FMVR compared to the state-of-the-art circuits.

Parameter	This Work	Ref. [5]	Ref. [14]	Ref. [15]	Ref. [17]	Ref. [18]	Ref. [21]
Technology	0.18 µm CMOS	65 nm CMOS	0.13 µm BiCMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Temperature range [°C]	-25~120	-40~125	-40~85	-50~100	-40~120	-40~125	-40~85
Supply voltage [V]	0.9~2	1.2	1.1~2.5	1~1.8	1.2~1.8	0.75~1.8	1.5~6
Line regulation [%/V]	0.02	0.0076	0.23	0.5	0.737	0.014	0.003
Vref [V]	0.648	0.59	0.72	0.963	1.09	0.469	0.985
Temperature coefficient [ppm/°C]	12.9	7	56	20	147	18	60.86
PSRR [dB]	-56@ 10 Hz -44@ 100 Hz	-43@ 100 Hz	N/A	N/A	-62@ 100Hz	-67@ 100Hz	-57@ 1MHz
Power consumption [nW]	7.6	1400	748	346	100	16.3	N/A
Area [mm²]	0.0023	0.03	0.011	N/A	0.0294	0.0053	0.015
FoM [°C³/W*mm²]	0.0932	0.00092	0.000034	N/A	0.00006	0.017	N/A

4. CONCLUSIONS

In this paper, a FMVR with low voltage level, low power consumption and high PSRR appropriate for IoT microsystems was presented. In this configuration, only MOS transistors operating in the sub-threshold region were utilized to minimize the power dissipation. The CTAT voltage was generated by a PMOS transistor with all three gate, drain, and source terminals connected together, and by adding half of the CTAT voltage to the PTAT cascade voltage generator, a temperature-independent reference voltage was obtained. The proposed FMVR circuit in 0.18 µm CMOS technology generated a reference voltage of 0.648 V with a TC of 12.9 ppm/°C in the temperature range of -25 °C to 120 °C. Also, with the 1 V power supply, the attained current consumption is 7.6 nA. Finally, the obtained layout area of the proposed FMVR is around 0.0023 mm^2.

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