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The Impact of Light Illumination on Capacitance-Voltage Characteristics of Constant-Current-Stressed Metal-Oxide-Semiconductor Capacitors

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***Abstract*—** This paper experimentally investigates the impact of trap location and light illumination on the quasi-static Capacitance-Voltage (*C-V*) characteristics of metal-oxide-semiconductor (MOS) capacitors after heavy constant-current stress (CCS). It has been discovered that under illumination, the width of the dip region of the quasi-static *C-V* curve is increased as the CCS-induced damage of the SiO_2 film is worse. In addition, clear hysteresis is observed in the quasi-static *C-V* curve under illumination. This behavior is basically not observed in the dark condition. This suggests photon-induced injection of electrons into the SiO_2 film, and that they are transiently captured at traps and emitted from them. A theoretical and mathematical model is proposed to explain this dynamic process of electrons inside the SiO_2 film of MOS capacitors, subjected to CCS-induced damage. Simulations verify that the model is physically appropriate, and that the behavior of the width of the dip region of the quasi-static *C-V* curve is quantitatively explained from the experimental result. Additional discussions of the model's predictions are also provided.

***Keywords*—** MOS capacitor; Silicon oxide; C-V characteristics; Illumination; Dynamic charging; Traps; Stress-induced degradation.

1. INTRODUCTION

One reliability issue with metal-oxide-semiconductor (MOS) devices is the gate insulator degradation due to carrier injection from the gate electrode and/or the substrate [1], external radiation [2], bias-temperature stress [3, 4], and so on. Drawing on many experiments, this phenomenon was analyzed theoretically and described in detail by Nicollian and Brews [5]. Silicon oxide films have been studied often, primarily for the goals of fabricating high-performance devices and enhancing the reliability of integrated circuits. Many techniques – such as quasi-static (QS) capacitance-voltage (*C-V*) method [6], conductance method [7] and other methods reported in [8, 9] - have been proposed to examine the quality of silicon oxide films fabricated on silicon substrates.

In [10], since the influence of surface quantization of the semiconductor substrate on capacitance measurement is anticipated, the authors proposed a correction method for the flat-band voltage because errors in the flat-band voltage measurement alter the values of oxide charge and interface state density at the SiO_2/Si interface extracted from high-frequency *C-V* curves and QS *C-V* curves. In practice, when the SiO_2 film is thinner than 5 nm, the error reaches about 100 mV, which is not negligible [11, 12]. This is due to the significant difference in the carrier distribution functions near the SiO_2/Si interface, i.e., the centroid of carrier distribution - as determined by the quantum-mechanical calculation - shifts to a deeper site than that by the semi-classical calculation that decreases the effective capacitance of the

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inversion layer. In addition, it has been demonstrated that such quantum correction has to be taken in account when evaluating interface state density (D_{it}) [13, 14], where the conventional technique underestimates D_{it} values by one order in the worst case.

The above analyses were performed under the dark condition in order to minimize the external influences. Recently, an analysis of *C-V* characteristics under illumination was performed for organic devices [15, 16] as well as Schottky barrier diodes and MOS capacitors [17, 18] because the illumination activates carriers at electrodes that are then injected into the insulator film and organic materials considered. This characteristic has been utilized to examine the energy-band alignment of fabricated film stacks [15, 16] and device interface quality [17, 18].

On the other hand, the impact of illumination on the *C-V* characteristics of MOS capacitors fabricated on crystalline Si substrates has been already analyzed theoretically [19], and the phenomenon was partially verified in experiments [20-22]. The work of Pierret and Sah [19] suggested that *C-V* analysis under illumination might have value in terms of trap analysis of MOS capacitors because the transient effect can be observed in *C-V* curves when an appropriate condition is chosen. However, the theoretical basis of the practical method for trap analysis was not investigated deeply because the quality of the thermally grown SiO_2 films was not so high [23, 24], which is the motivation of this study.

This paper challenges a feasible analysis of the quasi-static *C-V* characteristics of MOS capacitors under light illumination, the gate oxide of which has experienced electrical-stress-induced damage. Such an analysis for the dynamic phenomenon in MOS capacitors has been performed only for charge-pumping current analysis [25, 26]. In this paper, the unique QS *C-V* characteristics are analyzed based on the physics-based mathematical model proposed in this paper, and the different contributions of traps around the SiO_2/Si interface and those inside the SiO_2 film to behaviors of *C-V* characteristics are addressed.

2. DEVICE STRUCTURE, FABRICATION TECHNOLOGY, AND MEASUREMENTS

We consider QS *C-V* characteristics of the illuminated MOS capacitors shown in Fig. 1. Sample devices were fabricated on n-type (001) Si substrates with resistivity of 4 Ωcm. Thin silicon oxide films with a thickness of 5.2 nm were formed by means of rapid thermal oxidation (RTO) at 1000 °C. N-type poly-Si films for the gate electrode were formed by a low-pressure chemical vapor deposition technique [27]; the nominal doping level of phosphorus atoms was $4x10^{20}/cm^3$.

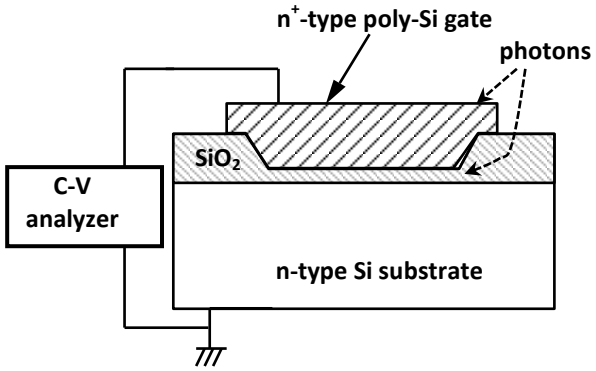

Fig. 1. Structure and measurement configuration of the investigated MOS capacitor.

The gate electrode was patterned by wet-etching to avoid process-induced damage. Poly-Si gate electrode size was 115 μm x 200 μm.

Positive gate bias was applied to all devices when evaluating device degradation by constant current stress. This stress condition allows only electron injection from the n-type substrate and does not allow hole injection from the gate poly-Si. When a negative gate voltage is applied to the device, both electron injection from the gate poly-Si and hole injection from the n-type substrate should be assumed. In order to develop a simple understanding of the degradation of SiO_2 film, positive gate bias was applied to the devices in this study as an initial electrical stress. It is known that such electron injection from the n-type Si substrate yields some traps near the SiO_2/Si interface and inside the SiO_2 film [28-31].

A semiconductor parameter analyzer (HP4155/56B) with a sweep rate of +/-10 mV/s was used to capture the QS *C-V* characteristics. Unidirectional sweep measurements were performed - where the gate voltage (V_G) was scanned from a positive voltage to a negative one – in addition to bidirectional sweep measurements, where the gate voltage was swept from a positive voltage to a negative one and returned to the original positive voltage level. D_{it} per unit area (D_{it} [/cm²/eV]) was also evaluated by means of the QS *C-V* technique. All measurements were carried out at room temperature in a dark condition or under the illumination condition. The illumination was realized by a halogen lamp (Philips Corp, 7023) equipped in the microscope. The peak wavelength of the lamp is about 800 nm and its power density is about 2 W/cm² on the device chip with the power supply of 12 V. It is anticipated that many photons will contribute to the excitation of electrons of poly-Si gate and substrate, and exited electrons are injected into the SiO_2 film as suggested in Fig. 1 because their energies are larger than the bandgap energy of silicon.

3. EXPERIMENTAL RESULTS

3.1. Impact of Illumination on QS *C-V* Characteristic; Fundamental Experimental Results

Three QS *C-V* curves of the device without any electrical stress are shown in Fig. 2, where C_{ox} is the gate SiO_2 film capacitance per unit area. The dotted line shows the theoretical result that is calculated under the dark condition; it corresponds to the quasi-static *C-V* curve (see Appendix A). The solid line shows the QS *C-V* curve measured under the dark condition; a slight over-depletion is seen for $V_G \leq$ -0.6 V because of negative sweep rate. The broken line shows the QS *C-V* curve measured under illumination, a steep swing in capacitance is observed as was theoretically expected [19]. Since the device has no electrical stress, the QS C-V curve shows a simple dip. The large difference in capacitance appearing in the broken line after the depletion condition reveals the significant generation of electrons beneath the SiO_2 film [19].

3.2. Impact of Stress-Induced Damage on QS *C-V* Characteristics under Dark Condition

Various QS *C-V* measurements were performed in order to elucidate the aspects of traps around the SiO_2/Si interface and those inside the SiO_2 film. If those traps exist only near the interface, C-V curves of post-stressed SiO_2 films should not be so sensitive to light illumination because they are, generally speaking, “fast states”. If they are sensitive to light

illumination, it is anticipated that those trap sites actually exist inside the SiO_2 film because observable transient processes are necessary. When they are "slow states", the observable trapping-detrapping processes need external energy like photons or a long time constant. Accordingly, in the following, this paper investigates the aspects of the QS *C-V* curves of post-stressed SiO_2 films.

Two experimental results are shown in Fig. 3; Fig. 3(a) shows the QS *C-V* curves derived from single-direction measurements, and Fig. 3(b) shows the curves obtained by two-direction measurements.

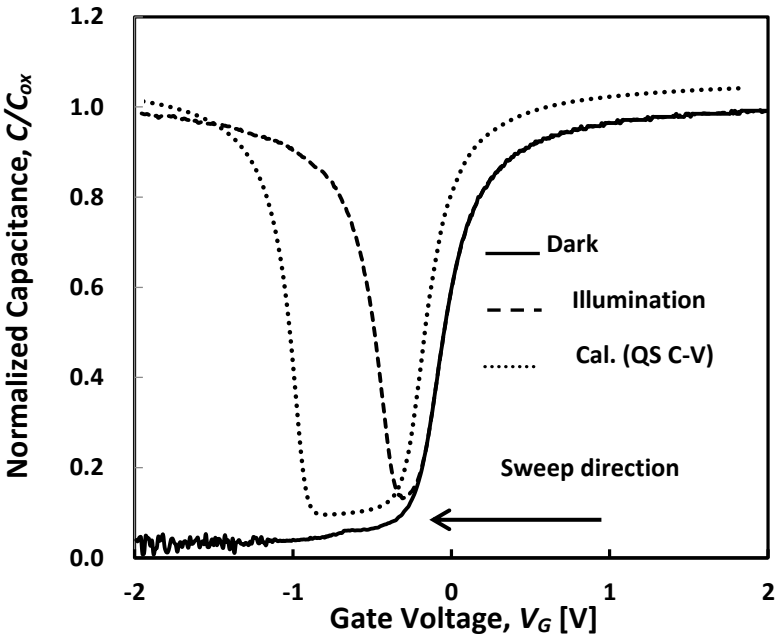

Fig. 2. QS C-V curves of the device without any electrical stress as functions of the gate voltage.

In Fig. 3(a), the solid line shows the experimental result of QS *C-V* measurement before electrical stress. Since the device after electrical stress shows a flat-band voltage (V_{FB0}) shift, the horizontal axis is changed to V_G-V_{FB0}. The broken line shows QS *C-V* curve of the device after constant-current stress (CCS) at 660 mA/cm^2; the total charge density injected (Q_{inj}) to the SiO_2 film was 16 C/cm^2. An irregular plot is observed for -1V < V_G –V_{FB0} < 0V in the device with damage. It is expected that this increase in capacitance stems from charges being trapped around the SiO_2/Si interface. The D_{it} value at the midgap is 3.9x10^{11} /cm^2/eV.

In Fig. 3(b), the solid line shows the QS *C-V* curve obtained when V_G was swept from the positive value to the negative value, and the broken line shows the QS *C-V* curve obtained when V_G was swept from the negative value to the original positive value. The QS *C-V* curves are for the device after CCS at 660 mA/cm^2, where the total charge density injected (Q_{inj}) to the SiO_2 film was 16 C/cm^2. It is found that the two curves almost overlap in the voltage region indicated by the dotted circle; it is suggested that the carrier response attributed to traps is mostly insensitive to voltage sweep direction. Since the present voltage sweep rate (+/-10mV/s) is not so fast, it should be considered that the carrier response stems primarily from the traps around the SiO_2/Si interface. As a result, the number of charged traps is basically independent of the sweep direction of V_G. A slight increase in the

capacitance value of the broken line is seen in the voltage region indicated by the "star" symbol. This phenomenon is observed on the over-depletion condition under dark illumination as is seen in Fig. 3(a). Therefore, it is considered that this stems from the generation of electrons near the SiO_2/Si interface because the sweep rate of the gate voltage is positive. Generation of electrons in the over-depletion condition increases the capacitance value of the device [9, 26].

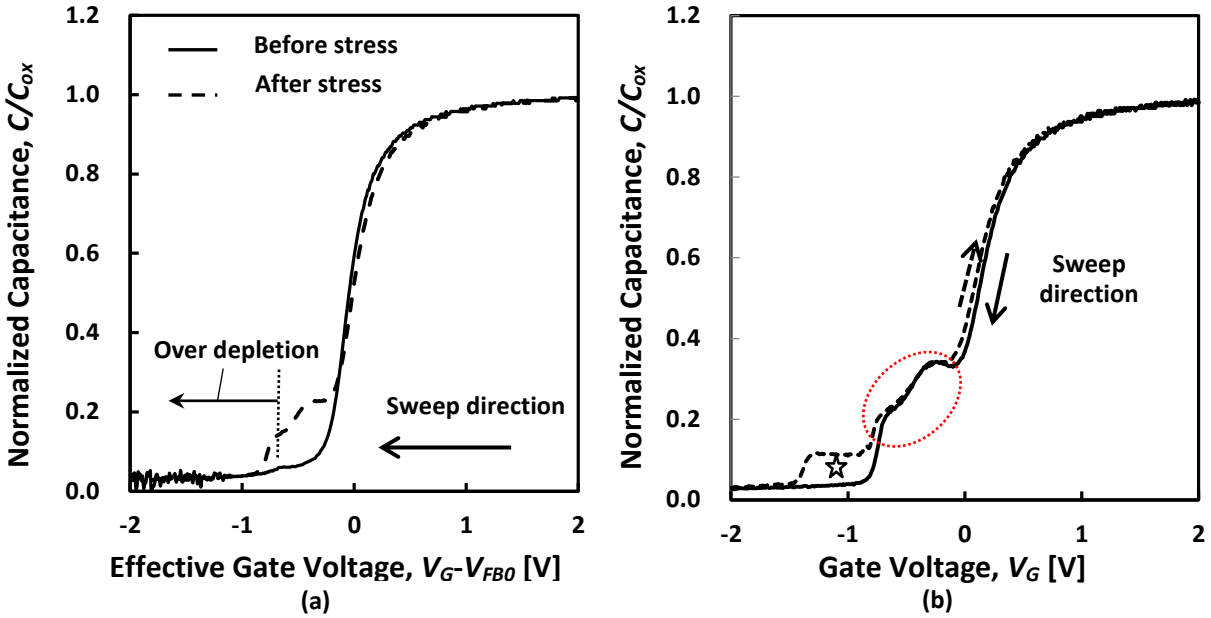

Fig. 3. QS *C-V* curves as a function of the gate voltage - under the dark condition before and after CCS - obtained by: a) unidirectional measurements; b) bidirectional measurements.

3.3. Impact of Stress-Induced Damage on QS *C-V* Characteristics under Illumination Condition

Two experimental results are shown in Fig. 4; Fig. 4(a) shows the QS *C-V* curves obtained by single-direction measurements, and Fig. 4(b) shows the curves obtained by two-direction measurements.

In Fig. 4(a), QS *C-V* measurements were performed for 4-different stress conditions, where the total charge injected into the SiO_2 film was 16 C/cm^2 and the stress current density (J_{stress}) levels were 0.66 mA/cm^2, 6.6 mA/cm^2, 66 mA/cm^2, and 660 mA/cm^2. For the purpose of comparison, the QS *C-V* characteristics of the control device before stress are also shown. Since the device after electrical stress shows a flat-band voltage (V_{FB0}) shift, the horizontal axis is changed to V_G-V_{FB0}.

"Apparent D_{it} values" around the midgap extracted from QS *C-V* curves shown in Fig. 4(a) are shown in Fig. 5 as a function of total charge density injected (Q_{inj}). Stress-current density (J_{stress}) condition is the parameter. It is seen, as expected, that "apparent D_{it} values" increase straightforwardly as the stress current density and total charge density injected are increased. The following consideration primarily focuses on a device stressed with total charge density injected (Q_{inj}) of 16 C/cm^2 and stress-current density (J_{stress}) of 660 mA/cm^2, where the "apparent D_{it} value" of the device is ~10^{12}/cm^2 as seen in Fig. 5. It should be noted that this value is much larger than the value of 3.9x10^{11}/cm^2 (see section 3.2) obtained from

Fig. 3(a). Therefore, it is suggested that the trap density existing inside the SiO_2 film is much higher than that around the SiO_2/Si interface.

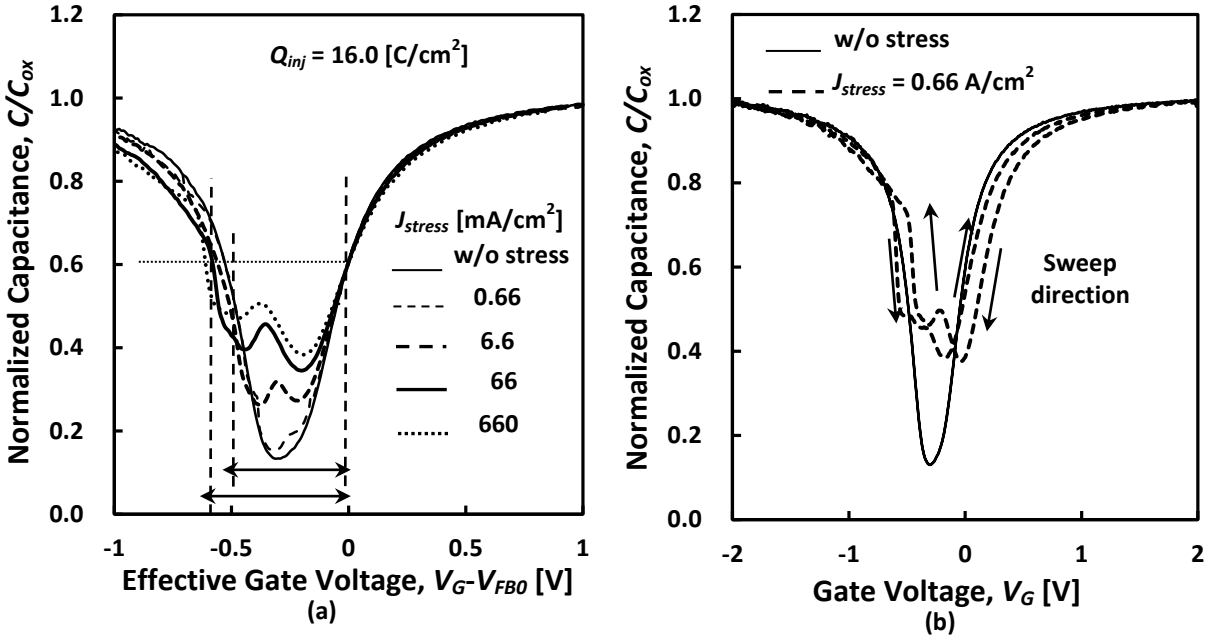

Fig. 4. QS *C-V* curves as a function of the gate voltage - under the illumination before and after CCS - obtained by: a) unidirectional measurements; b) bidirectional measurements.

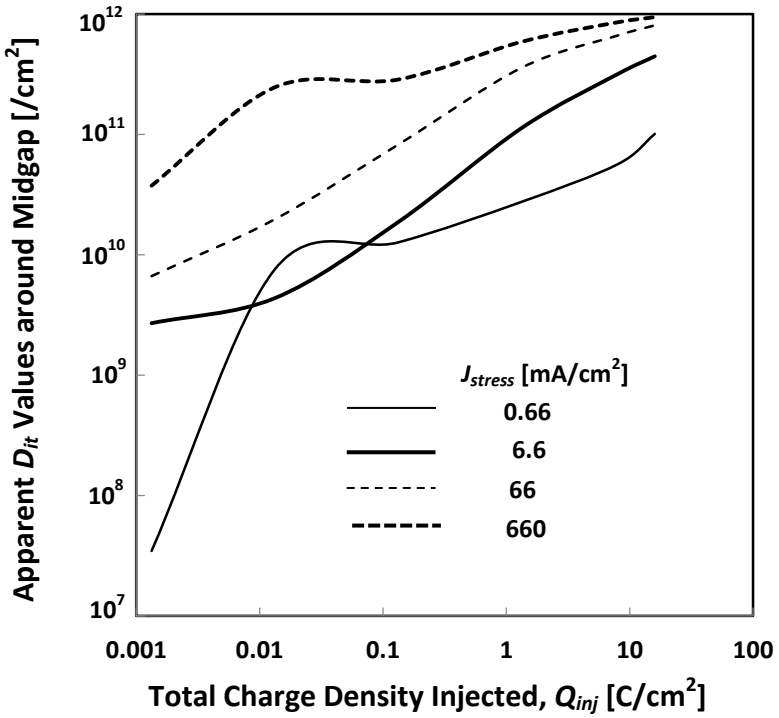

Fig. 5. "Apparent D_{it} values" - extracted from QS *C-V* curves under illumination - as a function of total charge density injected.

It is also clear that the width of the dip in the QS *C-V* curve is increased as the stress current density is increased. In Fig. 4(a), the widths of the dip regions for the devices before and after the stress of J_{stress} = 660 mA/cm² and Q_{inj} = 16 C/cm² are compared by the arrows

under the condition of C/C_{ox} = 0.6. The difference in dip width is about 0.1 V. It is confirmed that the phenomena observed in Fig. 4 are always observed when the electrical stress condition is significant. The phenomenon observed in Fig. 4(a) is discussed theoretically later.

In Fig. 4(b), QS *C-V* characteristics of the devices before and after CCS are compared. The J_{stress} and the Q_{inj} are as those in Fig. 4(a). The QS *C-V* characteristics of the control device before stress are also shown to provide a comparison with that of the device after stress. The QS *C-V* characteristics of the device after stress exhibit hysteresis; that is, the QS *C-V* curve for the V_G sweep from negative voltage to positive one shows a shift toward the negative voltage side. This reveals that negative-charged traps in the stress-induced damage region are returning to neutral states, unlike the V_G sweep from the positive voltage toward the negative voltage. Since this behavior is not observed under the dark condition as shown in Fig. 3(b), it is expected that the optical illumination triggers dynamic charging and discharging processes. The fact that the flat-band voltage - measured in the dark condition - almost matches the value calculated without any charge inside the SiO_2 film, means that most traps inside the SiO_2 film are initially neutral.

Since we cannot expect that this phenomenon stems from traps around the SiO_2/Si interface as was mentioned previously in the discussion of the QS *C-V* curves shown in Fig. 3(b), it can be assumed that it is an optical response of traps existing in a deep region of the film. This point is addressed in a later section. The following section proposes a plausible primary mechanism that is examined based on a theoretical formulation.

4. MODELING AND DISCUSSION

4.1. Feasible Model of Dynamic Charging and Discharging of SiO_2 Film

Though it is considered that the characteristics of the QS *C-V* curves shown in Fig. 3(b) stem primarily from "fast states", the characteristics shown in Fig. 4(b) stem primarily from "slow states". Thus, we use the model to discuss how the slow states alter the characteristics of the QS *C-V* curves. Since the experimental results suggest dynamic negative charging in SiO_2 films, a time-dependent local negative charge ($Q_{ic}(t) < 0$) must be assumed for the films. Since many past papers suggest that the primary traps characterize the stress-induced leakage current in thin SiO_2 films [28-30], this paper starts with this point. The model proposed here to explain the energy band diagram is illustrated in Fig. 6, where it is assumed that the local negative charge distribution is like a sheet at $z = \alpha\, t_{ox}$ (measured from the gate poly-Si/SiO_2 interface) [30, 32]; t_{ox} is SiO_2 film thickness and $0 < \alpha < 1$.

As shown in Fig. 6, some electrons exited by photons are captured by traps inside the SiO_2 film when they are injected into the film by the local electric field, where it is expected that some electrons reach trap sites through the tunneling process. Therefore, it is considered that such process is relatively "slow". $\phi_{s1}(t)$ is the time-dependent surface potential at the SiO_2/Si substrate interface, $\phi_{s2}(t)$ is the time-dependent surface potential at the gate poly-Si/SiO_2 interface, and V_{ox} is the effective oxide voltage drop across the film induced by the gate voltage (V_G).

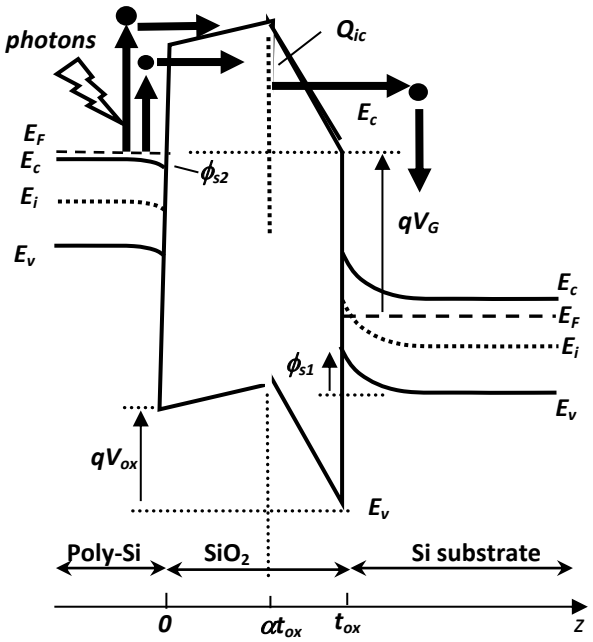

Fig. 6. The proposed theoretical model of dynamic charging and discharging of SiO2 film.

When the relation of $Q_{ic}(t) = 0$ is introduced, we have the following time-dependent equation based on Gauss's theorem [33]:

$$-C_{ox}\left[V_G - V_{FB0} - \phi_{s1}(t) - \phi_{s2}(t)\right] = Q_s\left(\phi_{s1}(t)\right), \tag{1}$$

where V_{FB0} is the flat-band voltage composed of the static Fermi level of the gate material and the static Fermi level of the Si substrate, and $Q_s(\phi_{s1}(t))$ is the total charge density per unit area in the Si substrate. Since the time retardation effect is not explicitly considered in Eq. (1), its influence is discussed later (see Appendix C). It must be noted that time "t" is measured from the moment at which a certain gate voltage is achieved in the measurement; that is, Eq. (1) reveals the transient process. Therefore, Eq. (1) is satisfied at any voltage condition. The static semi-classical theoretical form for the total charge density per unit area in the Si substrate, $Q_s(\phi_{s1})$, is given in [34]. When a negative value of $Q_{ic}(t)$ is assumed at $z = \alpha t_{ox}$, the effective charge contributing the flat-band voltage is given by $\alpha Q_{ic}(t)$ (see Appendix B). So, Eq. (1) is rewritten as [33]:

$$-C_{ox}\left[V_G - V_{FB0} - \phi_{s1,c}(t) - \phi_{s2,c}(t)\right] - \alpha Q_{ic}(t) = Q_s\left(\phi_{s1,c}(t)\right), \tag{2}$$

where $\phi_{s1,c}(t)$ and $\phi_{s2,c}(t)$ are the modified surface potential at the SiO_2/Si substrate interface and the modified surface potential at the poly-Si/SiO_2 interface, respectively. Eq. (2) also reveals the transient process as does Eq. (1). It is considered here that $\phi_{s2,c}(t)$ itself and its variation can be both discarded because the doping level of the poly-Si is very high (~4×10^{20} /cm^3). When the following relation is introduced [35],

$$\phi_{s1,c}(t) = \phi_{s1}(t) + \Delta\phi_{s1}(t), \tag{3}$$

the theoretical form of $\Delta\phi_{s1}(t)$ can be approximately derived from Eqs. (1) and (2) as [36]:

$$\Delta\phi_{s1}(t) \cong \frac{\alpha Q_{ic}(t)}{C_{ox}} + \frac{\partial Q_s\left(\phi_{s1}(t)\right)}{\partial\phi_{s1}(t)}\frac{\Delta\phi_{s1}(t)}{C_{ox}}, \tag{4}$$

where the influence of $\phi_{s2,c}(t)$ is discarded.

Finally, we have:

$$\Delta\phi_{s1}(t) \cong \frac{\alpha Q_{ic}(t)}{C_{ox} + C_S\left(\phi_{s1}(t)\right)}, \tag{5}$$

$$C_S\left(\phi_{s1}(t)\right) = -\frac{\partial Q_s\left(\phi_{s1}(t)\right)}{\partial \phi_{s1}(t)}\ , \tag{6}$$

where $C_S(\phi_{s1})$ stands for the capacitance component of the semiconductor surface [34]. When the illumination condition holds constant, the phenomenon seems to be a steady state. More details are found in Appendix C. Eq. (5) predicts the following:

- The width of dip shape of QS *C-V* curve expands with the negative value of $\alpha Q_{ic}(t)$.
- The capacitance dip shape is modulated by the surface potential (ϕ_{s1}).
- $|\Delta\phi_{s1}(t)|$ takes the maximal value in the surface depletion condition.

Simulation results given by Eq. (5) are shown in Fig. 7, where the device parameters are the same as those of the devices used here. In calculating $\Delta\phi_{s1}(t)$, the $C_S(\phi_{s1})$ values are derived from the corresponding experimental results given in Fig. 2 (see Appendix D). The two curves correspond to the two different values of $\alpha Q_{ic}(t)$ that are assumed based on the V_{FB0} shifts for Q_{inj} = 8C/cm² and 16 C/cm². The lowest values of $\Delta\phi_{s1}(t)$, that are predicted theoretically, roughly match the experimental values of the increase in width of dip region extracted from Fig. 4(a), although parameter α is not determined at this stage. We can assume that $Q_{ic}(t)/q$ > 3.2x10¹¹/cm² for Q_{inj} = 8C/cm² because α < 1.

As depicted in Fig. 4(a), for J_{stress} = 0.66 mA/cm², the width of dip region of the QS *C-V* curve is almost the same as that before stressing. This suggests that many "slow traps" are created inside the SiO_2 film for J_{stress} > 0.66 mA/cm². Though "apparent D_{it} value "range from 10⁹/cm²/eV to 10¹²/cm²/eV for J_{stress} > 0.66 mA/cm², the corresponding QS *C-V* curves successfully catch the "slow traps" created by the electrical stress because those QS *C-V* curves reveal hysteresis based on the time delay of the trapping-detrapping processes.

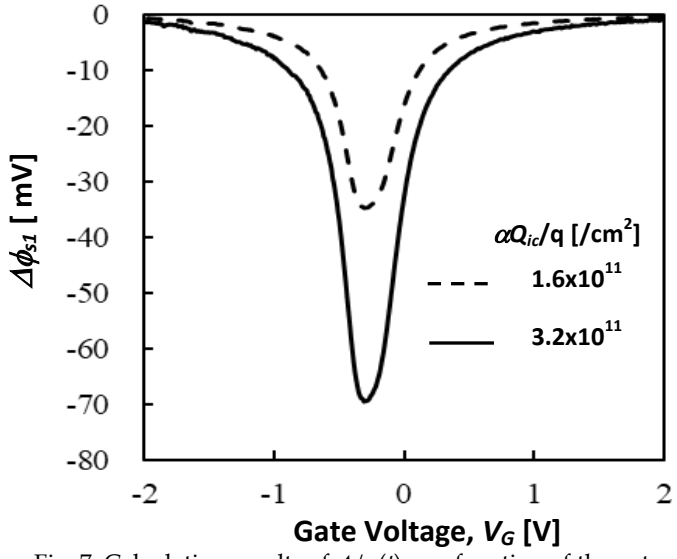

Fig. 7. Calculation results of $\Delta\phi_{s1}(t)$ as a function of the gate voltage.

In addition, the hysteresis observed in Fig. 4(b) is logically understood as follows: when the device is in standby with positive V_G value for some time, most traps in the

damaged region take a negative charge due to the assistance of photon energy; that is, some electrons of surface accumulation layer of the substrate are excited by photons and injected into the SiO_2 film, for example, by the tunneling process. Consequently, the flat-band voltage shifts toward the positive direction, and a finite negative value of $\Delta\phi_{s1}(t)$ is observed as shown in Fig. 4(a). When the device is in standby with negative V_G value, most traps in the damaged region are neutral due to the external electric field in spite of the energetic excitation provided by the electrons from the external photons. Some traps may be charged positive by the injection of holes that are injected with the aid of photon energy when gate voltage (V_G) is negative.

4.2. Additional Consideration on Dynamic Charging and Discharging of SiO_2 Film

A past experiment on stress-induced leakage current (SILC) assumed that the traps were localized inside the SiO_2 film [28-30]. Since QS *C-V* characteristics of the MOS capacitor revealing the SILC were not examined under illumination, no conclusion could be drawn as whether the device exhibited the dynamic charging and discharging characteristics observed here.

It is well known that irradiation by high-energy photons creates many traps inside SiO_2 [32, 37-44] and other dielectric films as well as at the dielectric film/Si substrate interface [45-50]. Experiments have demonstrated that the traps have positive charge. In that case, Eq. (5) suggests that the width of dip region of the QS *C-V* curve should shrink. Though the distribution of traps has been investigated, few experimental results have been reported so far [32]. This point should be examined in the future. Though the value of α is not shown here, it is also a future study to investigate whether the charge pumping technique is applicable to this issue.

The point discussed here is also important in the analysis of resistive switching mechanisms of SiO_2 films [51-56] because it is not finalized whether the conductive filament is the single primary mechanism rather than the bulk degradation considered for thin thermal SiO_2 films [57-60]. Recently, the potential for an optical trigger in the resistive switching behavior of silicon oxide films was demonstrated [61], where the authors thought that photon-induced increase in carrier density lowered the switching voltage. They demonstrated that the optical response of the leakage current is very slow, which suggests that the transient process of traps existing inside the silicon oxide film is slow. It is expected that analyses of the transient effect appearing in such QS *C-V* curves will be useful for understanding these phenomena.

5. CONCLUSIONS

This paper experimentally investigated the impact of trap location and light illumination on the QS *C-V* characteristics of MOS capacitors after heavy CCS. It was demonstrated that the *C-V* curve is modulated in the dark condition by the damage due to CCS; however, the curve exhibits virtually no hysteresis. On the other hand, under illumination, it was discovered that the width of dip region of the QS *C-V* curve is increased as the CCS-induced damage of the SiO_2 film worsens. In addition, clear hysteresis was observed in the QS *C-V* curve. It is considered that the phenomenon observed in this

experiment is triggered by the dynamic charging and discharging processes induced by photon-induced energetic excitation.

A theoretical model was proposed based on the above assumption and examined quantitatively in the light of experimental results. It has been verified that the model is acceptable. The meaning of the predictions made by the model was also addressed.

Acknowledgement: The author expresses his thanks to Mr. S. Kan (undergraduate student) for his technical assistance in measuring the *C-V* characteristics.

Appendix A: Calculation of QS C-V Curve

Quasi-static C-V curve in a metal-gate MOS capacitor is theoretically given in [34], where the total space charge (Q_s) in the semiconductor substrate is expressed as:

$$Q_S = \pm \frac{\sqrt{2} k_B T}{q L_D} F\left(\phi_{s1}, \mathrm{N}_A\right). \tag{A.1}$$

where L_D is the Debye length of the substrate and the expression of function $F(\phi_{s1}, N_A)$ is given in [34]. In this experiment, surface potential ϕ_{s2} must be taken in account because the capacitor has a poly-Si gate electrode. When Boltzmann's approximation at room temperature is applied to Poisson's equation, the space charge (Q_{SP}) near the poly-Si/SiO_2 interface can be expressed as:

$$Q_{SP} = \mp \frac{\sqrt{2} k_B T}{q L_{DG}} F\left(\phi_{s2}, \mathrm{N}_G\right), \tag{A.2}$$

where L_{DG} is the Debye length of the poly-Si and N_G is the doping level of the poly-Si. Relation among V_G and two surface potentials (ϕ_{s1} and ϕ_{s2}) is expressed as [33, 34]:

$$V_G = V_{FB} + Q_S + Q_{SP} \ . \tag{A.3}$$

Combining Eqs. (A.1), (A.2) and (A.3) yields the solution of Q_S as a function of V_G. Consequently, we have the normalized capacitance of the MOS capacitor (C/C_{ox}) as [33]:

$$\frac{C}{C_{ox}} = \frac{C_S C_{SP}}{C_S C_{ox} + C_S C_{SP} + C_{ox} C_{SP}} \tag{A.4}$$

Though Q_{SP} is calculated based on Boltzmann's approximation in Eq. (A.2), the calculation of C/C_{ox} is not influenced in practice because of $C_{SP} >> C_S$ and $C_{SP} >> C_{ox}$ independently of the physics assumed. Then we have [34]:

$$\frac{C}{C_{ox}} = \frac{C_S}{C_S + C_{ox}} \tag{A.5}$$

Appendix B: Calculation of Effective Charge (Q_f) Contributing to the Flat-Band Voltage

As shown in Fig. 6, it is assumed that all the traps exist at $z=\alpha t_{ox}$. In this case, the effective charge density (Q_f) contributing to the flat-band voltage is given by [62]:

$$Q_f = \frac{1}{t_{ox}} \int_0^{t_{ox}} z Q_{iC} \delta\left(z - \alpha t_{ox}\right) dz = \alpha Q_{iC} \tag{B.1}$$

where $\delta(z)$ is Dirac's δ function. Therefore, the contribution of charged traps to the flat-band voltage depends on factor α (< 1).

Appendix C: Relation between the Voltage Sweep and Response of Charged Traps

For example, the discharging process of electrons captured at traps is assumed. Since the gate voltage changes in stair-like manner during the measurement, the following expression is applicable to $Q_{ic}(t)$ at any voltage condition [63].

$$Q_{iC}(t) = Q_{\max}(\phi_{s1}) \exp\left(-\frac{t}{\tau_{dc}}\right) \tag{C.1}$$

where Q_{max} is the initial charge before discharging and τ_{dc} is the time constant for the discharging process. Time "t" is measured from the moment at which a certain forwarding gate voltage is setup. When the gate voltage is swept, the variation of $Q_{ic}(t)$ is given by Eq. (C.2) as:

$$\begin{aligned} \Delta Q_{iC}(t) &\cong \frac{dQ_{iC}(t)}{dt}\Delta t = Q_{\max}(\phi_{s1}) \cdot \left(\frac{\Delta t}{\tau_{dc}}\right) \exp\left(-\frac{t}{\tau_{dc}}\right) \\ &= Q_{iC}(t) \cdot \left(\frac{\Delta t}{\tau_{dc}}\right) \end{aligned} \tag{C.2}$$

Though $\Delta Q_{iC}(t)$ depends on τ_{dc}, Δt is constant at each voltage condition during the measurement and $\Delta Q_{iC}(t)$ correctly reflects the value of $Q_{iC}(t)$ at each voltage condition. Therefore, $\Delta\phi_{s1}(t)$ can be estimated by Eq. (5) at any voltage condition.

In "fast states" like those existing around the SiO_2/Si interface, generally speaking, the time constant is very short, so $\Delta Q_{iC}(t)$ can be observed only when Δt is very small. In the present experiment, however, Δt is large. Therefore, "slow states" are automatically extracted from all responses.

Appendix D: Calculation of $C_S(\phi_{S1}(V_G,t))$

Measured capacitance, C_m, is expressed as [33]:

$$C_m(V_G,t) = \frac{C_{ox}C_S(V_G,t)}{C_{ox} + C_S(V_G,t)}, \tag{D.1}$$

where $C_S(V_G,t)$ is effectively the same as that given by Eq. (6) because the surface potential is a function of V_G. $C_S(V_G,t)$ can be expressed as:

$$C_S(V_G,t) = \frac{C_{ox}C_m(V_G,t)}{C_{ox} - C_m(V_G,t)}. \tag{D.2}$$

Since $C_m(V_G,t)$ values are given in experiments, $\Delta\phi_{s1}(V_G,t)$ can be calculated using Eq. (5).

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