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Control of Improved Non-Isolated High Gain DC-DC Converter

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***Abstract*—** This paper proposes an improved non-isolated high gain DC-DC converter based on quadratic boost topology. The proposed converter contains multiplier cells to boost the output voltage level of the converter. The switched capacitor gain cell acts as multiplier and provides necessary gain improvement. A mathematical model of the high gain converter is derived based on the physical significance of the capacitors during on and off states of the switches. The controller parameters are obtained using the genetic algorithm optimization method. The proposed topology provides high gain without using extreme duty ratios. To regulate the output voltage, a closed loop PID control scheme is also proposed for the high gain converter. The proposed circuit, i.e., the high gain DC-DC converter in closed loop with PID controller is tested in MATLAB/Simulink environment. The obtained results show that the proposed circuit provides stable high voltage output even during the presence of input and load variations.

***Keywords*—** DC- DC converter; Voltage multiplier; PID controller; Genetic algorithm.

1. INTRODUCTION

Recent changes in the environmental conditions such as global warming and increased demand for electricity have led to the rapid progress in research to produce electricity from renewable resources. In that, solar energy has emerged to meet the electricity demand and to give a feasible solution to the above mentioned problem. Solar cells have gained significant attention as the foremost renewable energy technology. The photovoltaic (PV) output is not constant because it mainly depends on irradiance and temperature. The output voltage of solar PV cells is usually small and, hence, stepping up the output voltage has to be done to use the power more efficiently. A DC-DC boost converter can boost the output from a solar cell. Many industrial applications also require broad range of DC voltages to meet their demand. DC-DC boost converters are often employed in such situations to provide broad range of DC voltages. In conventional boost converters, the voltage gain increases by increasing the duty ratio. These extreme duty ratios impose inefficiently small off-times or low switching frequencies, and lead to enormous switching losses. To reduce the switching stress that many high gain DC-DC circuits emerges, transformer loss multilevel DC-DC converter circuit is majorly used to produce high gain [1]. Cascading two or more boost converters is also used to improve the voltage gain with reduced duty ratio [2]. But, the number of switches used in this circuit is quite high and it leads to switching loss in the circuit. Azizkandi et al. discussed the high voltage gain obtained by the use of voltage doubler circuit with coupled inductor [3]. Voltage surges and electromagnetic interference are present while using the coupled inductor, so it degrades the circuit efficiency. To overcome these drawbacks, many circuits are proposed in which quadratic boost topology, voltage multiplier circuits are prominent [4-8]. The conventional converter performance degrades due to low switching frequency, high ripple current, switching loss and conversion gain. An exciting

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topology which provides high voltage with single switch is the quadratic boost converter. The voltage gain provided by the circuit is in the quadratic function of the duty ratio [9-11]. Moreover, addition of switched capacitor circuit with quadratic boost converter circuit gives better voltage conversion ratio without using a transformer and without extreme duty ratio.

The proposed converter adds the advantage of both quadratic boost and multilevel boost DC-DC converter [12, 13] such as continuous input current, high gain conversion ratio, transformer loss and allows high switching frequency. It can be built in a modular way and more levels can be added without changing the main circuit. It also provides several self-balanced voltage levels and only one driven switch. Also, it resolves the imbalance problem which occurs in the diode clamped multilevel converter and provides the option for increasing the number of output voltage levels by adding a diode-capacitor pair [14-16].

Based on the above consideration, modeling the proposed high gain converter is performed using state space approach. To achieve better steady state and dynamic output responses, the converter needs to be operated in closed loop with a controller. Genetic algorithm optimization approach is used to obtain the parameters of the PID controller.

The rest of the paper is organized as follows: in section 2, the proposed high gain circuit is given and its operation is discussed in continuous conducted mode (CCM). In section 3, modeling and analysis of the proposed converter is given. The mathematical modeling is carried out using the state space approach. The design of PID controller is discussed in section 4. The performance of the proposed converter with controller is validated through simulation and the results are given in section 5. Finally, the conclusions are made in section 6.

2. HIGH GAIN DC-DC CONVERTER

The conventional quadratic non-isolated high gain converter contains one active switch (MOSFET), two capacitors and three diodes as shown in Fig. 1 which shows the formation of the proposed high gain converter from quadratic boost and multilevel boost DC-DC converters. The proposed circuit is obtained from [11-13, 15]. Authors in [11] explain the operation and control of quadratic boost converter while authors in [12, 13, 15] discuss the multilevel boost DC-DC converter. The current and voltages of the proposed converter are shown on Fig. 2 in which E represents the input voltage and V_0 represents the output voltage. The proposed high gain converter circuit consists of a single active switch (SW), couple of inductors, 2N-1 diode and 2N-1 capacitor where N indicates the number of levels in the output (see Fig. 2). The circuit operates in two modes: CCM and discontinuous conduction mode and it is based on the duty ratio. Here, the proposed converter operates in CCM mode. The inductor currents (i_{L1} and i_{L2}) in the circuit do not fall to zero, and the ripple content is also minimum.

The operation of the proposed circuit is predominantly classifies into two operating states: (i) switch-ON state and (ii) switch-OFF state.

When the converter operates in switch-ON state – as exhibited in Fig. 3 - the diode D_2 conducts, and the diode D_1 operates in reverse bias condition. During this time the inductor L_1 charges from input voltage source E and inductor L_2 from capacitor C_1. The diode D_4 goes forward biased, because the voltage across C_2 is greater than the voltage across capacitor C_4. Hence, C_2 clamps C_4's voltage through D_4. Here C_4 is connected to ground through the

switch SW. In order to simplify the circuit, short circuit path (SW path) can be divided as two, so that the original circuit cannot be disturbed by the new one.

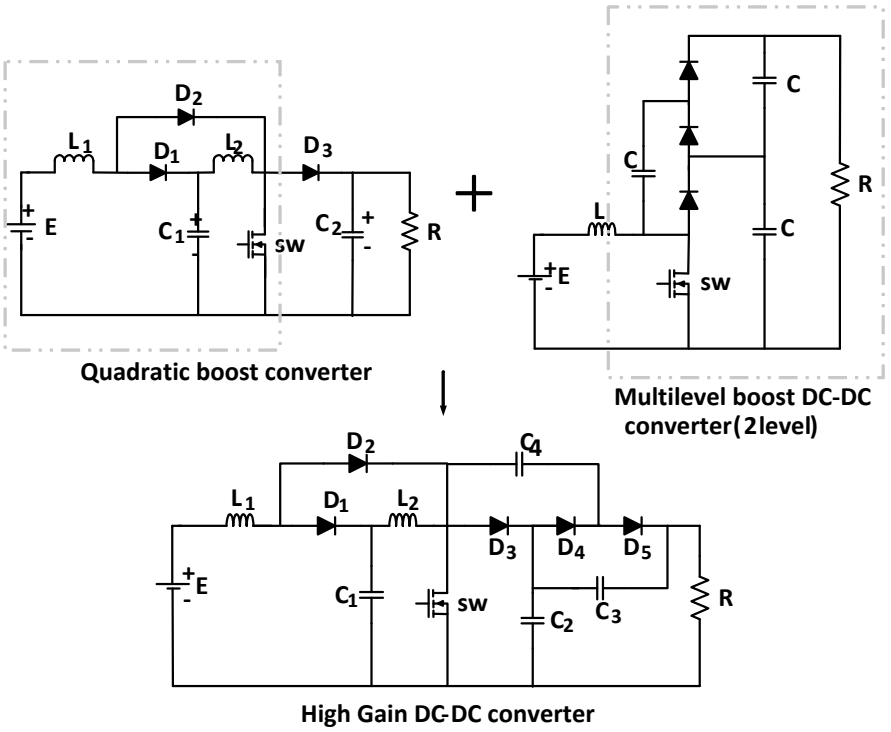

Fig. 1. Formation of proposed high gain converter.

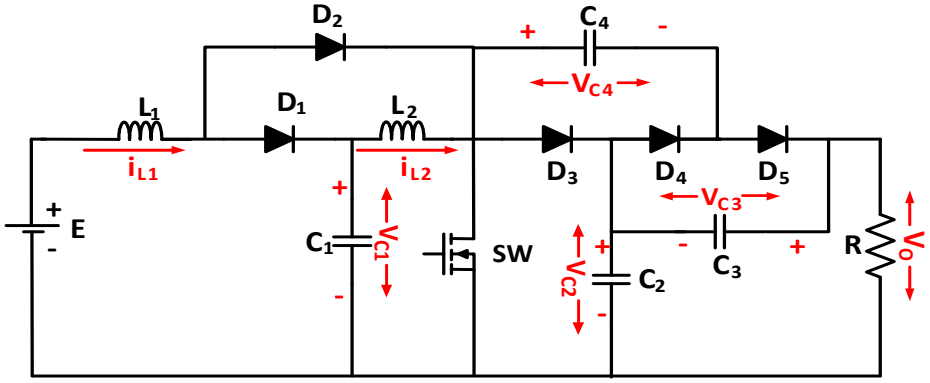

Fig. 2. Currents and voltages of the proposed high gain converter.

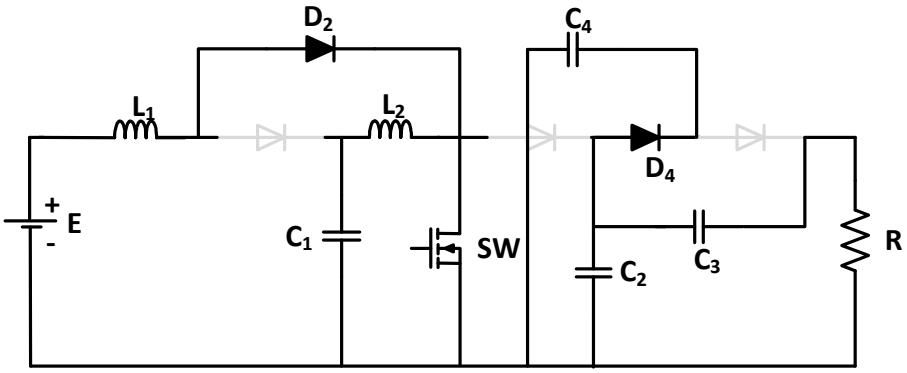

Fig. 3. Converter's operation in the switch-ON state.

Similarly - in the switch-OFF state depicted in Fig. 4 - diodes D_1 and D_3 operate in the conducting mode and other diodes D_2, D_4 and D_5 work in non-conducting mode. Therefore, the energy stored in inductors L_1 and L_2 becomes discharged. The capacitor C_1 starts charging by the conduction of D_1 and the capacitor C_2 is charged by the conduction of the diode D_3. Finally, the voltage across the capacitor C_4, input voltage E and the inductor's voltage clamp the voltage across C_2 and C_3 by the conduction of diode D_5.

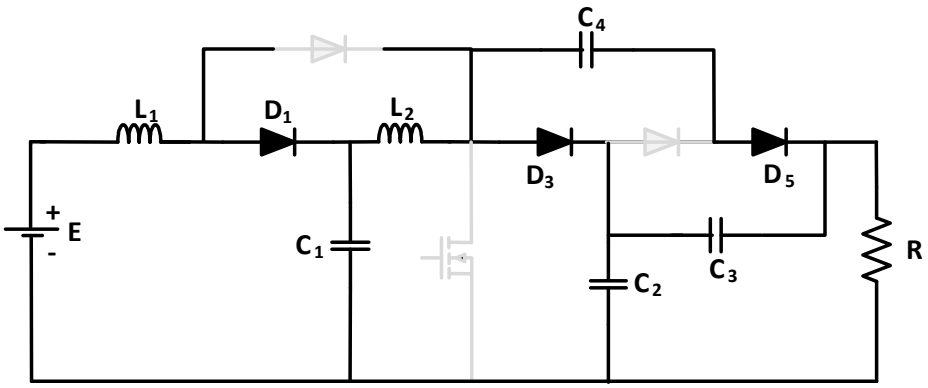

Fig. 4. Converter's operation in the switch-OFF state.

The voltage gain of the proposed converter is the same as that of the quadratic boost converter with multiplication factor or number of voltage level N and is presented as:

$$\frac{V_0}{E} = \frac{N}{(1-D^2)} \quad (1)$$

Where D represents the duty ratio and V_o is the voltage across the output resistor R. for comparison, voltage gain relation for other high gain converters are given in Table 1.

Table 1. Voltage gain relation for various types of high gain converters.

Parameter	Type of converter		
	Quadratic boost converter [11]	Multi-level boost DC–DC converter [12, 13, 15]	The proposed high gain converter
Voltage gain	$\frac{V_0}{E} = \frac{1}{(1-D^2)}$	$\frac{V_0}{E} = \frac{N}{(1-\mathrm{D})}$	$\frac{V_0}{E} = \frac{N}{(1-D^2)}$

3. MODELING OF THE PROPOSED HIGH GAIN CONVERTER

The state space model of the proposed converter can be derived for the ON and OFF states separately. These two models can be combined and an average model can be obtained. The transfer function of proposed converter can be obtained from the average state space model. The ON and OFF state diagrams are shown in Figs. 3 and 4 and can be reduced - by combining the capacitance values and simplified circuits - to the circuits shown in Figs. 5 and 6. The proposed converter output voltage is in balancing form and the same values of capacitors are used in the switched circuit.

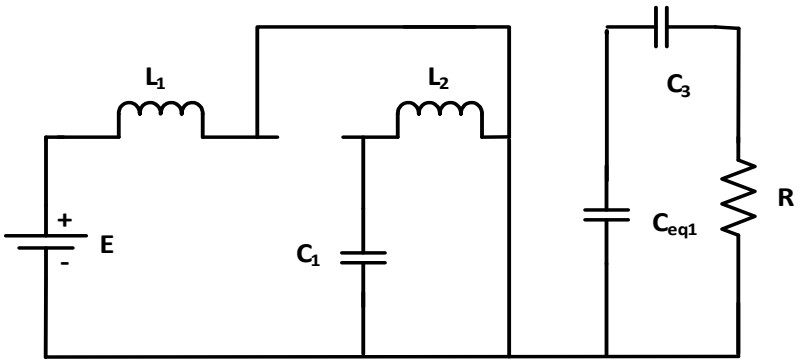

Fig. 5. Simplified ON state diagram.

Fig. 5 shows the equivalent circuit during ON state. Here, capacitor C_1 is in parallel with capacitor C_3 and the equivalent value is treated as C_{eq1}. Hence the corresponding ON state relation is given in the Eq. (2) as:

$$\begin{aligned}\frac{di_{L1}}{dt} &= \frac{E}{L_1}\\ \frac{di_{L2}}{dt} &= \frac{V_{C1}}{L_2}\\ \frac{dV_{C1}}{dt} &= -\frac{i_{L2}}{C_1}\\ \frac{dV}{dt} &= -\frac{NV}{RC_{eq1}}\end{aligned} \tag{2}$$

Where N represents the number of levels such as the number of diode and capacitor pairs that are used to increase the gain, while V represents the voltage across the capacitor C_2, C_3 and C_4. In the proposed circuit, the number of levels N is taken as 2.

Similarly, when the switch is in the OFF state, the capacitors C_4 and C_3 are in parallel but the equivalent capacitor C_{eq2} is C and is shown in Fig. 6. Here $C \approx C_1 \approx C_2 \approx C_3$ and $V_1 \approx V_2 \approx V_3 \approx \ldots\ldots \approx V_N \approx V/N$, The voltage across the load resistor R is $V=V_o$.

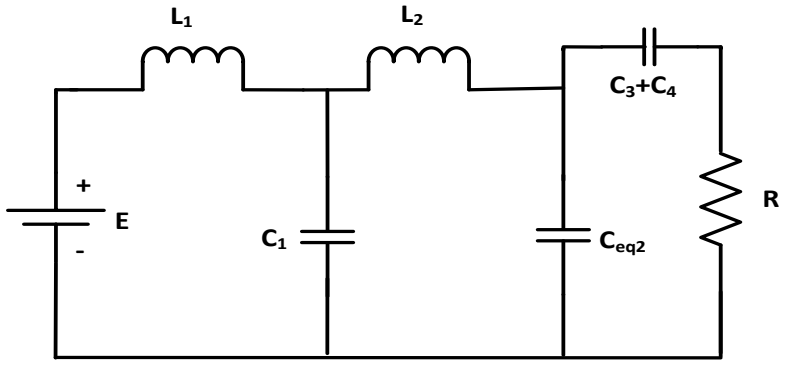

Fig. 6. Simplfied OFF state diagram.

Eq. (3) shows the OFF state relation.

$$\begin{aligned}\frac{di_{L1}}{dt} &= \frac{E}{L_1} - \frac{V_{C1}}{L_1}\\ \frac{di_{L2}}{dt} &= \frac{V_{C1}}{L_2} - \frac{V}{L_2}\\ \frac{dV_{C1}}{dt} &= \frac{i_{L1}}{C_1} - \frac{i_{L2}}{C_1}\\ \frac{dV}{dt} &= \frac{i_{L2}}{C_{eq2}} - \frac{NV}{RC_{eq2}}\end{aligned} \tag{3}$$

The state space model can be obtained by assuming that the perturbations are sufficiently small such that nonlinear terms can be neglected. The circuit components are derived from the allowable limits of capacitor voltage and inductor current.

As per the state equation $\dot{x} = Ax + Bu$, switch-ON state and switch-OFF state equations are formed using Eqs. (2) and (3) and given in Eqs. (4) and (5), respectively, where C_{eq1}=2C, C_{eq2}=C.

$$\begin{bmatrix} \dot{i_{L1}} \\ \dot{i_{L2}} \\ \dot{V_{C1}} \\ \dot{V} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{N}{2CR} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ \text{V} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [\text{E}] \tag{4}$$

$$\begin{bmatrix} \dot{i_{L1}} \\ \dot{i_{L2}} \\ \dot{V_{C1}} \\ \dot{V} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & -\frac{N}{CR} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ \text{V} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [\text{E}] \tag{5}$$

Output equation $y = Cx + Du$, where D= 0. Switch-ON and switch-OFF states for output equation remains the same and is given by:

$$V = [0\ 0\ 0\ N] \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ \text{V} \end{bmatrix} + [0][E] \tag{6}$$

Any variable in the physical system has two parts, i.e., u = U + $\hat{u}$, d = D + $\hat{d}$, x = X + $\hat{x}$, y = Y + $\hat{y}$. Eqs. (7-10) depict how the average model of the ON state and the OFF state is derived from the relations A = A_1 D + A_2 (1-D) and B = B_1 D + B_2 (1-D).

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{N}{2CR} \end{bmatrix} D + \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & -\frac{N}{CR} \end{bmatrix} (1 - D) \tag{7}$$

$$A = \begin{bmatrix} 0 & 0 & -\frac{(1-D)}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{(1-D)}{L_2} \\ \frac{(1-D)}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{(1-D)}{C} & 0 & -\frac{N}{2CR} - \frac{N(1-D)}{CR} \end{bmatrix} \tag{8}$$

$$B = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \text{D} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \text{(1-D)} \tag{9}$$

$$B = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \text{(E)} \tag{10}$$

The general small signal model is given in Eqs. (11) and (12) as:

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + [(A_1 - A_2)x + (B_1 - B_2)u]\hat{d} \quad (11)$$

$$\hat{y} = C\hat{x} + D\hat{u} + [(C_1 - C_2)x + (D_1 - D_2)u]\hat{d} \quad (12)$$

By replacing $\dot{x} = 0$, duty cycle d is replaced as $\hat{d}$ where $A\,\hat{x} + B\,\hat{u}$ is termed as small signal model. Here, $\hat{x}.\hat{d}$ is assumed to be neglected and $\dot{x} = Ax + Bu = 0$. The general small signal mode state equation and output equation are expressed in Eqs. (13) and (14), respectively.

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} \quad (13)$$

$$\hat{y} = C\hat{x} + D\hat{u} \quad (14)$$

From the above equation, small signal model state space equation for the high gain DC-DC converter is formed and shown in Eq. (15):

$$\begin{bmatrix} \dot{\widehat{\imath_{L1}}} \\ \dot{\widehat{\imath_{L2}}} \\ \dot{\widehat{V_{C1}}} \\ \dot{\hat{V}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{(1-D)}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{(1-D)}{L_2} \\ \frac{(1-D)}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{(1-D)}{C} & 0 & -\frac{N}{2CR} - \frac{N(1-D)}{CR} \end{bmatrix} \begin{bmatrix} \widehat{\imath_{L1}} \\ \widehat{\imath_{L2}} \\ \widehat{V_{C1}} \\ \hat{V} \end{bmatrix} + \begin{bmatrix} \frac{E}{(1-D)L_1} & \frac{1}{L_1} \\ \frac{E}{(1-D)^2 L_2} & 0 \\ -\frac{\left(\frac{3}{2}-D\right)NE}{(1-D)^4 RC_1} & 0 \\ -\frac{\left(\frac{3}{2}-D\right)NE}{(1-D)^3 RC} + \frac{NE}{(1-D)^2 RC} & 0 \end{bmatrix} \begin{bmatrix} \hat{d} \\ \hat{e} \end{bmatrix} \quad (15)$$

The variable with hats represents the small signal parameters. $\hat{d}$ and $\hat{e}$ represent the duty ratio (control signal) and input voltage, respectively.

3.1. Components Design

Designing the circuit components is based on the permissible changes in current and voltage in corresponding inductors and capacitors, respectively. 20% of current variation is considered to design the inductor value and 5% change in voltage is considered to design the capacitor value. Current flow through the inductor depends on the duty ratio. Eq. (16) represents the inductor L_1 which depends on input voltage, switching frequency and change in inductor current. Eq. (17) represents the inductor L_2. Similarly the capacitor values are formulated and given in Eqs. (18) and (19).

$$L_1 = \frac{ED}{\delta i_{L1} f_{sw}} \quad (16)$$

$$L_2 = \frac{ED}{\delta i_{L2}(1-D) f_{sw}} \quad (17)$$

$$\mathbf{C_1} = \frac{\mathbf{I_0 D}}{\mathbf{(1-D)\Delta V_{C1} f_{sw}}} \quad (18)$$

$$\mathbf{C = C_2 = C_3 = C_4} = \frac{\mathbf{I_0 D}}{\mathbf{\Delta V_{C2} f_{sw}}} \quad (19)$$

where δi_{L1} and δi_{L2} represent the change in inductor currents L_1 and L_2, respectively. 20% of change in the inductor current is appreciated. From the design formula, L_1 varies from 60 µH to 240 µH and L_2 varies from 240 µH to 960 µH. ΔV_{C1}, ΔV_{C2} represent the change in voltage across capacitors C_1 and C_2, respectively. In order to design the capacitor, the change in voltage is considered as ΔV_{C1}= ΔV_{C2}= 5%. The parameter C_1 varies from 8.33 µF to 33 µF and C_2 varies from 33 µF to 110 µF. f_{sw} represents the switching frequency chosen as 40 kHz.

The circuit parameters are designed for the rated values of 48 V, 24 W. The parameters are obtained from the design formula in [17] and the circuit parameters are listed in Table 2.

Table 2. Circuit parameters of the proposed converter.

Parameter	Value
Input voltage (E)	6 V
Output voltage (V_0)	48 V
Inductor (L_1)	90 μH
Inductor (L_2)	382 μH
Capacitor (C_1)	22 μF
Capacitor (C_1, C_2, C_3)	100 μF
Duty ratio (D)	0.5
Load resistor (R)	100 Ω

4. PID CONTROLLER

PID controller is an automatic process controller that produces accurate and stable output. It is widely used to regulate the temperature, pressure and other variables in the industrial process. The performance of the proposed converter is satisfactory under normal operating conditions. But, the output of the converter would not be stable when there are sudden changes in the input or load. To achieve effective dynamic and steady state responses, it is necessary to operate the converter in closed loop using PID controller. The controller gain parameters such as K_p, K_i and K_d are responsible for providing required dynamic performance for the converter. Controller gains are tuned either by Zeigler Nichols tuning method or by automatic tuning method. The duty cycle is the control parameter for the proposed system and the output voltage is the control variable. $\hat{V}$ represents the output voltage across the load resistor R. From the state space Eq. (4), the transfer function is obtained for the ratio of output voltage ($\hat{V}$) to duty ratio ($\hat{d}$) and it is given in Eq. (20) where $\hat{V}=\hat{V_o}$ and $\hat{e}=0$. Using the designed parameter (shown in Table 1) and Eq. (20) relation, the output voltage to duty ratio transfer function is derived and given in Eq. (21).

$$\frac{\hat{V}}{\hat{d}} = C[SI - A]^{-1}B \tag{20}$$

$$\frac{\hat{V}}{\hat{d}} = \frac{-7200s^3+3.14\times10^8s^2-2.9\times10^{12}s+7.9\times10^{16}}{s^4+200s^3+2.5\times10^8s^2+4.9\times10^{10}s+8.2\times10^{14}} \tag{21}$$

4.1. Optimization Using Genetic Algorithm

Genetic algorithm (GA) is a stochastic search process for finding approximate solution for a given optimization problem based on natural selection and natural genetics. The fittest individuals are selected as in [18, 19].

Zeigler Nichols tuning method is the most popular design method for finding the parameters of PID controller. The large percentage overshoot and high oscillatory responses are the major drawbacks of the PID controller designed using the Ziegler Nichols method. The PID controller can also be designed using the meta-heuristic methods such as GA and particle swarm optimization. Especially, GA is proven to optimize good PID gains with PID controller to minimize the error between the feedback value and reference value. The optimized objective functions are calculated by iterative process which consists of selection, reproduction, cross over and mutation.

4.1.1. Fitness Function

To optimize the PID gain using GA, a good fitness function is needed to be determined. Some popular fitness functions are mean of the squared error (MSE), integral of time multiplied by absolute error (ITAE), integral of absolute magnitude of the error (IAE) and integral of the squared error (ISE). The fitness of the chromosome is decided by the value of the fitness function and main aim of the fitness function is to reduce the error. The fitness function values are determined using the relation in Eq. (22).

$$Fitness\ Functoin\ Value = \frac{1}{Performance\ Index} \quad (22)$$

We are choosing the ITAE as the fitness function and is given in Eq. (23).

$$f = \int t|e(t)|dt \quad (23)$$

4.1.2. Implementation of GA

GA optimization is simulated using optimization tool in MATLAB. Here, ITAE is chosen for the fitness function. The unknown output parameter of the fitness function is defined as K_p, K_i, and K_d. Other input parameters are presented in Table 3.

Table 3. GA parameters.

Population size	80
Lower bound	[0 0 0]
Upper bound	[40 40 10]
Initial range	[-100 100]
Selection function	Stochastic uniform
Elite count	0.1
Crossover fraction	0.8
Mutation function	Constraint dependent

The flowchart of the GA process is shown in Fig. 7. The general execution procedure for GA is as follows:

a) The outputs are defined as K_p, K_i, and K_d. ITAE is chosen as the fitness function
b) Initial population of 80 is created
c) The selection of lower and upper bound: The proper choice will reduce the iteration time. Lower bound and upper bound is defined as [0 0 0] and [40 40 10], respectively
d) Each individual is rated based on the fitness function value. A small value indicates the individual is fit. A large value shows that the individual is less fit
e) The best fit individuals are selected as parent
f) The best fit parent is selected to be breed by crossover and mutation to produce new population
g) The value of elite count in this case is 0.1. This indicates that only small amount of low fitness individual is selected to be inherited to new population in new generation
h) Crossover and mutation of parents is done to create new children for new population
i) Process is repeated until the output satisfies the stopping criteria. For each generation, the iteration tries to converge to zero value of fitness function
j) The simulation is conducted several times to ensure the accuracy of the results.

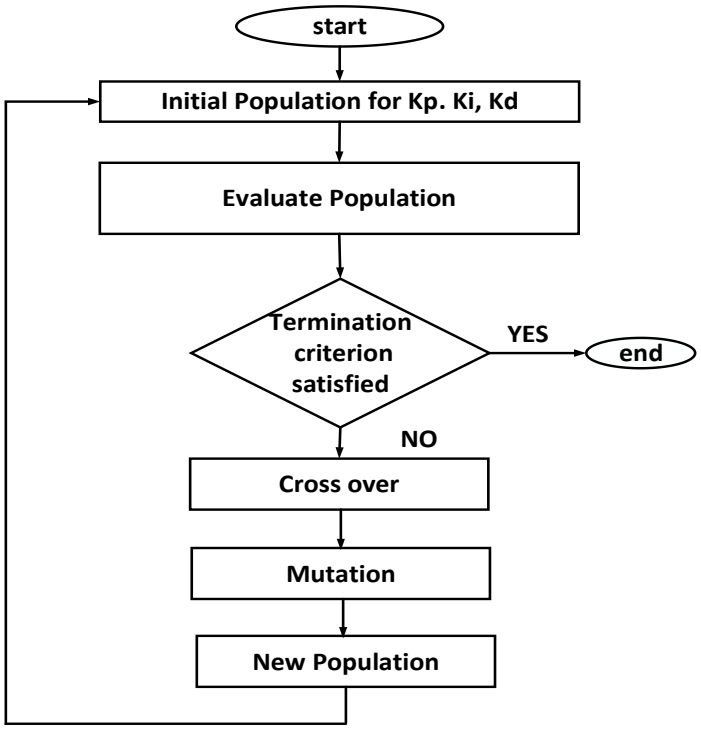

Fig. 7. Flowchart of the GA process.

This process continues till obtaining a stable and accurate solution. Using the above procedure, the controller gain parameters are obtained and given in Table 4.

Table 4. Parameters of PID controller.

Parameter	K_p	K_i	K_d
Value	0.00149	1.02	0.015

5. PERFORMANCE ANALYSIS

The proposed high gain converter with PID controller is implemented using MATLAB/Simulink. Block diagram and Simulink diagram are displayed in Figs. 8 and 9, respectively.

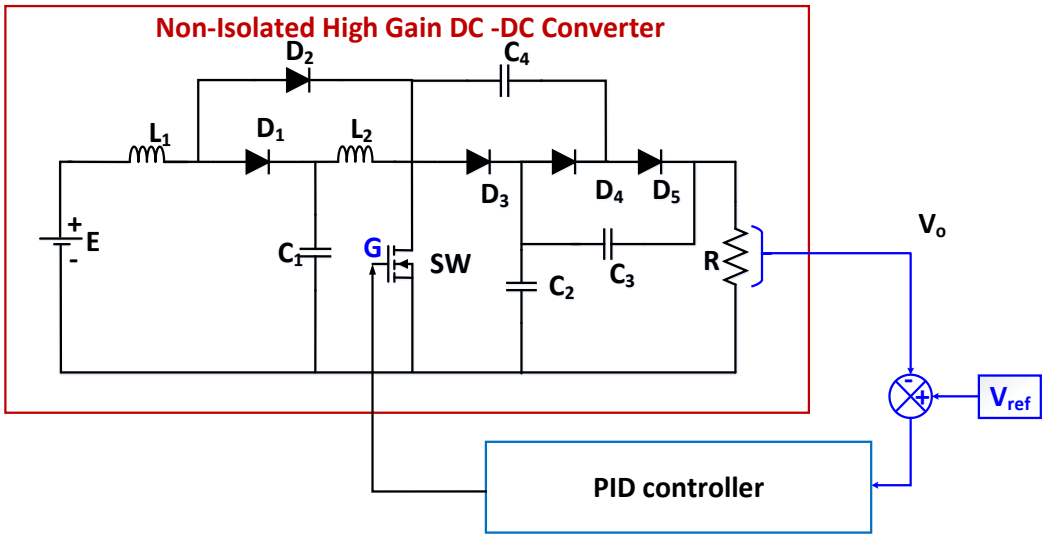

Fig. 8. Block diagram of proposed high gain DC-DC converter with PID controller.

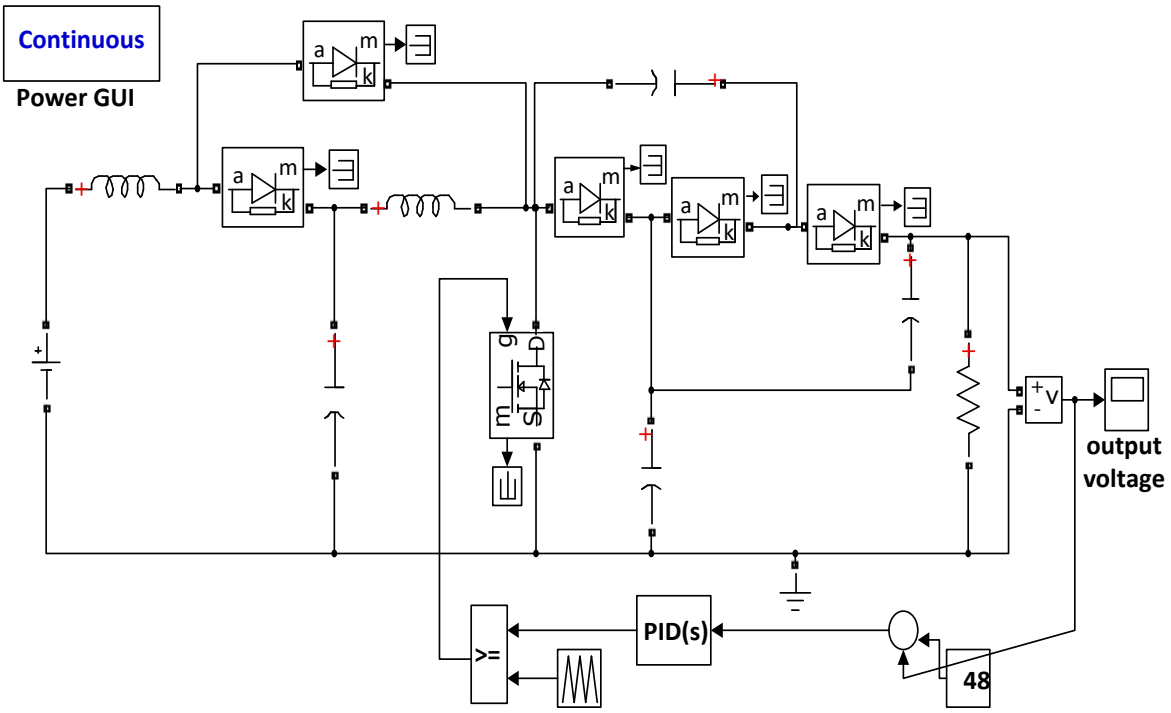

Fig. 9. Simulink diagram of the proposed high gain DC-DC converter with PID controller.

Initially, the system is tested under open loop condition by varying the input voltage from 5 V to 9 V. It is found that the output voltage of the converter varies from 30 V to 58 V (see Fig. 10). The regulation can be achieved only by using PID controller in the closed loop. It is found that the step variation of input voltage will not affect the performance of the closed loop system and the output is maintained at a constant regulated voltage of 48 V as shown in Fig. 11.

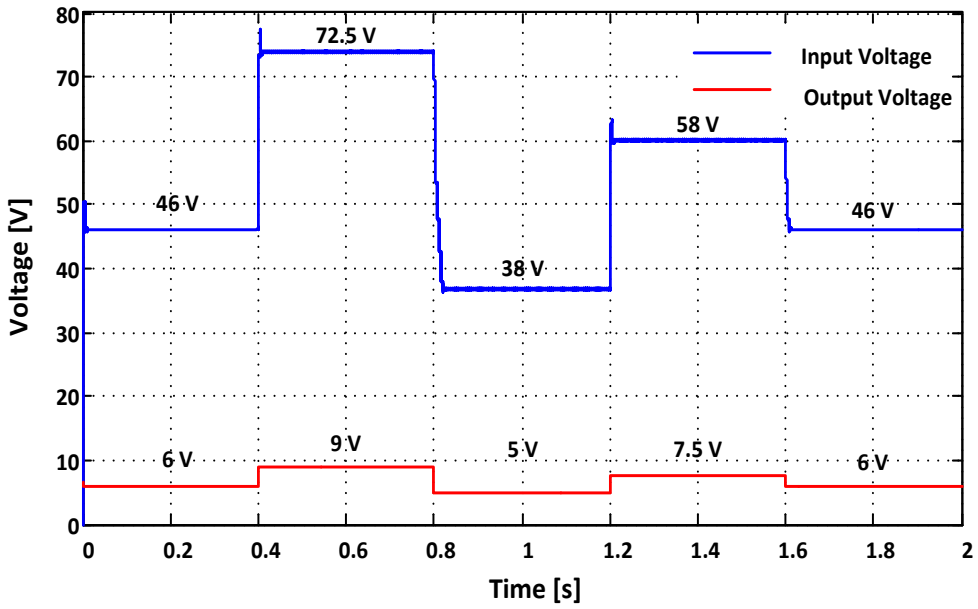

Fig. 10. Open loop response of V_0.

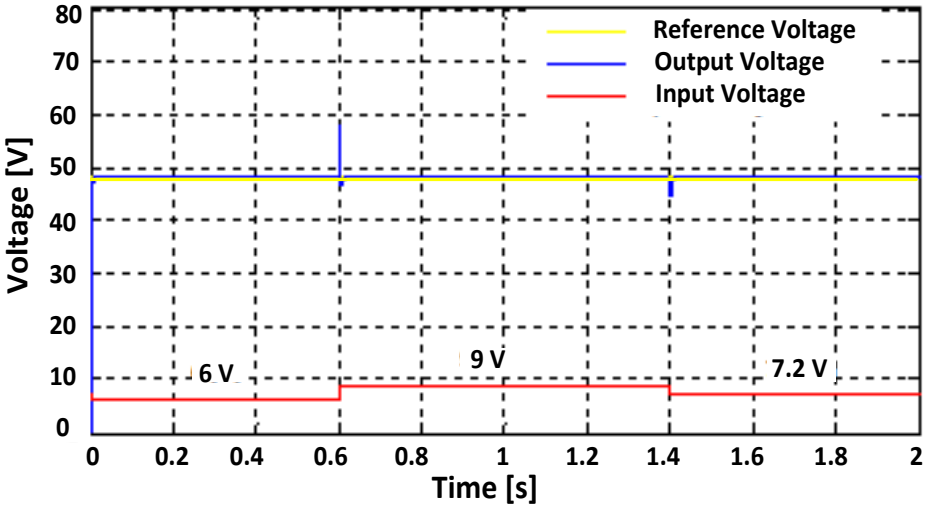

Fig. 11. Closed loop response of V_0.

The inductor current i_{L1} varies from 1.6 A to 2.6 A, inductor current i_{L2} varies from 0.8 A to 1.2 A, output current maintained as 0.3 A for the 6 V input with the load resistor 250 Ω (see Fig. 12). The voltage across switch (as shown in Fig. 13) represents the converter low duty cycle (i.e., approximately 0.6) with reduced switching stress.

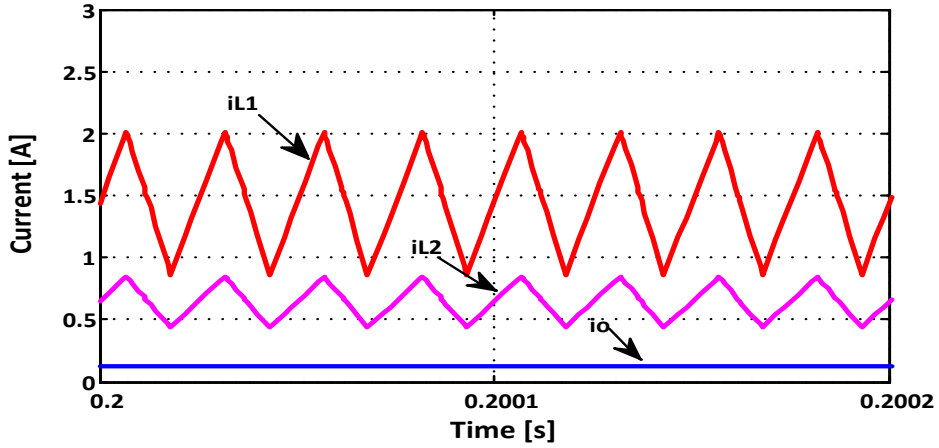

Fig. 12. Current waveforms.

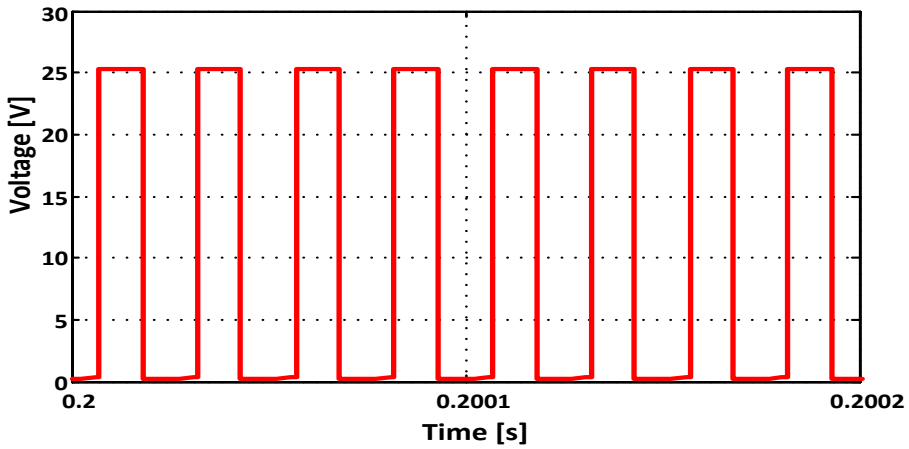

Fig. 13. Voltage stress across the switch.

The output of the proposed converter is tested under dynamic step changes on load resistor. To test the control action, the load resistor is varied from 250 Ω to 500 Ω. The output remains constant at 48 V with reduced ripple as shown in Fig. 14. The step load disturbance is given at 0.5 s, and it is observed that a small undershoot arises (i.e. Approximately 0.6 V) and it settles within 0.01 s. Even the output current varies from 0.2 A to 0.45 A (shown in Fig. 15), there is no abrupt change in the output voltage. Hence, the output voltage has been regulated and maintained at the required value in spite of variations in input voltage and load. Voltage gain to duty ratio graph plots (Fig. 16) compares various converters in terms of the voltage gain with different duty ratios. The graph exhibits that the proposed high gain converter gives more voltage gain than other converters. Because the large variation in load affects the performance of the converter, the controller with high performance for fast transient response and good regulation is necessary. For achieving good dynamic and steady state response, PID controller is extensively used. Fig. 14 shows the response of the proposed converter for different load conditions (i.e., 500 ohms to 250 ohms). Also, the different loads are applied and analysis of the performance is shown in Figs. 17 and 18. The results exhibits that the proposed converter gives better regulation on drastic load changes (variation around 0.5 V to 1 V).

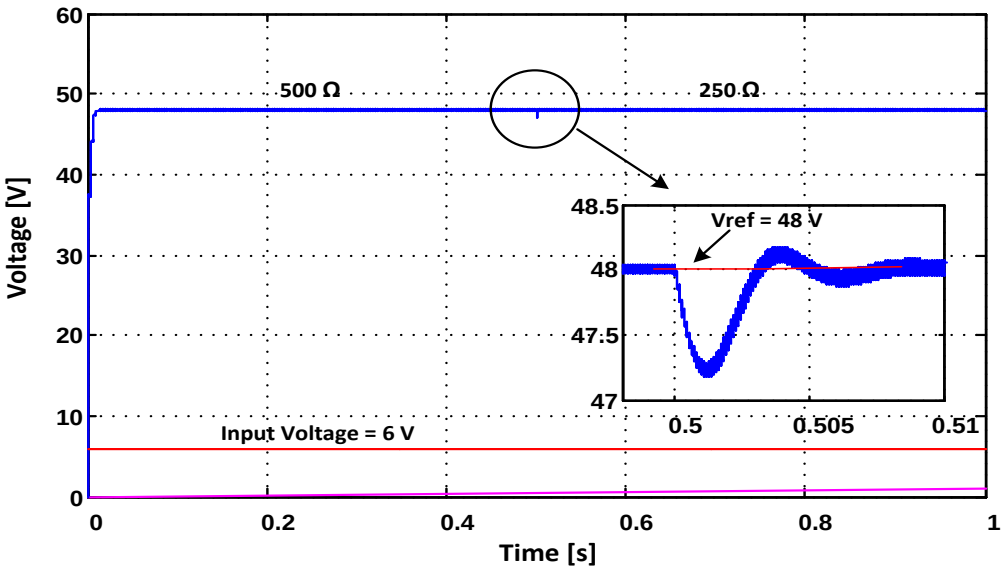

Fig. 14. Step load response of the proposed converter.

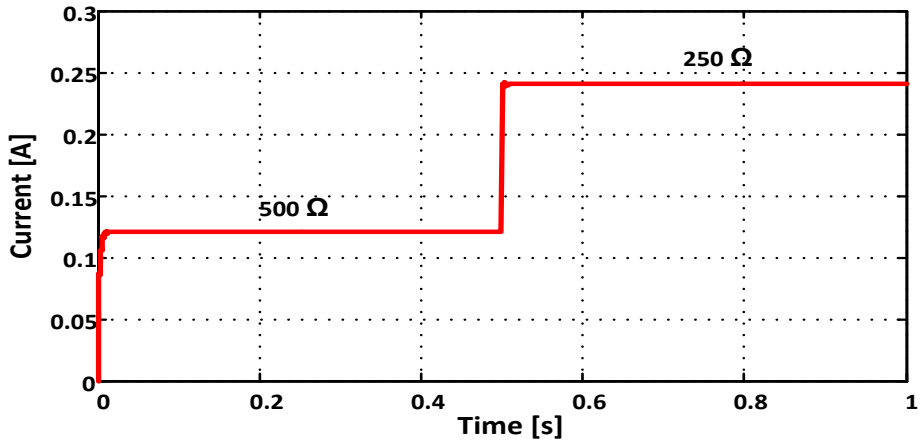

Fig. 15. Output current of the proposed converter.

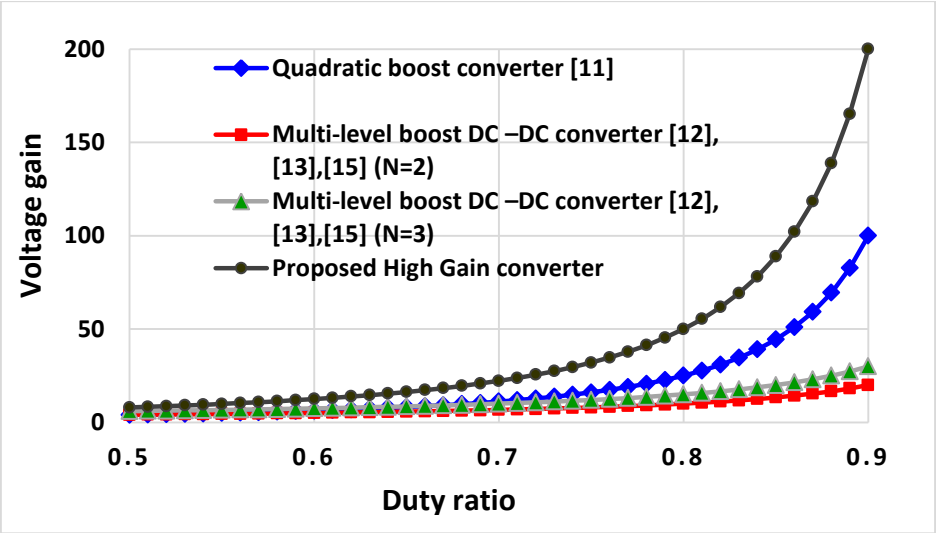

Fig. 16. Voltage gain vs duty ratio for various converters.

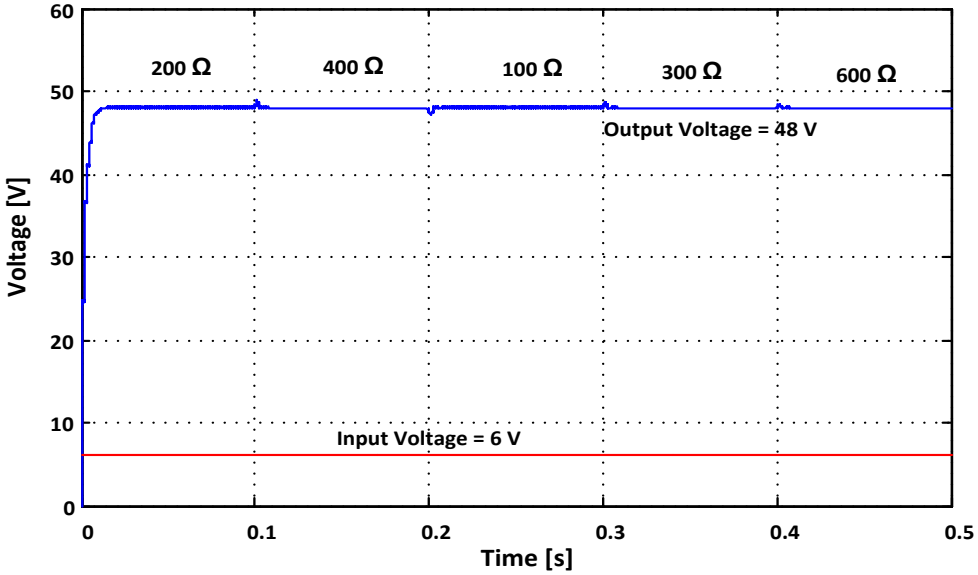

Fig. 17. Dynamic step load response of the proposed converter.

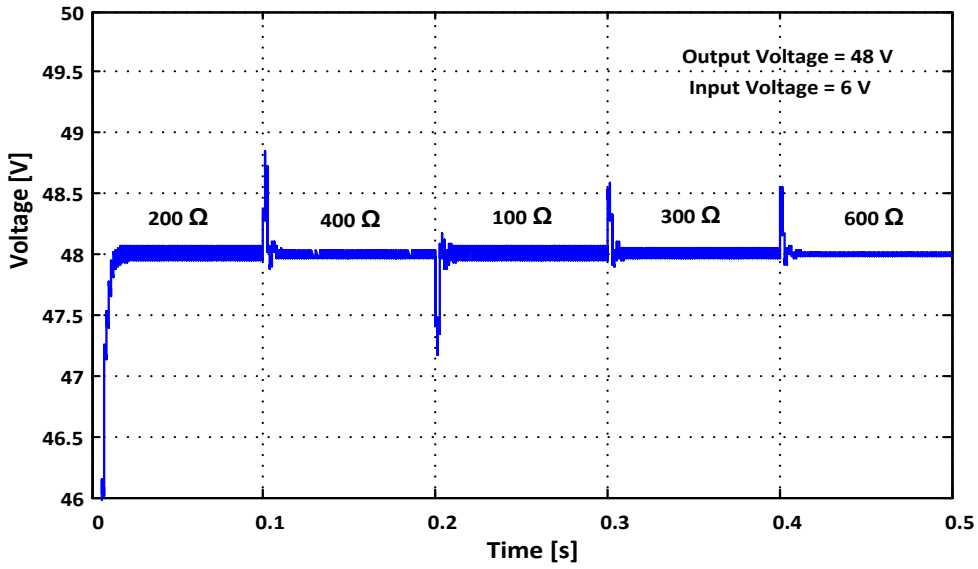

Fig. 18. Voltage ripple on dynamic load response.

The implementation of PID controller for the proposed converter has not been tried before. In this paper, the performance of proposed circuit is analyzed based on the dynamic performance, settling time of load variation and line variation is too minimum and the overshoot also present under the limit (see Table 5), hence PID controller operates in excellent manner.

Table 5. Performance of the proposed circuit.

Parameter		Settling time [s]	Overshoot [%]
Dynamic response	Load variation	0.003	5.2
	Line variation	0.02	18

6. CONCLUSIONS

An improved high gain DC-DC converter is proposed in this work. A mathematical model of the proposed converter was obtained based on the circuit behavior during ON and OFF conditions. The performance of the proposed converter was analyzed in simulation. It was found that the converter provides high gain for normal duty ratio of 0.5. A PID controller was designed using GA optimization method and the performance of the converter in closed loop with PID controller was also tested in simulation. It was found that the proposed converter with PID controller provides stable high voltage output even during the presence of input and load variations. The output voltage of the proposed high gain converter was regulated with reduced overshoot/undershoot, and it provided constant DC output voltage for supplying grid or battery charging applications.

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