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Extended Research on Small-Signal Modelling of Current-Mode Controlled Parallel-Input/Series-Output Buck-Based Converters

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Abstract— A more detailed state-space-based small-signal model is developed for peak current-mode controlled parallel-input/series-output buck-derived dc-dc converters operating in the continuous conduction mode. The model allows the control of each module individually; and it includes the sampling effect of the module current loop. The derived model is employed to assess the effect of mismatch between the output-filter inductors on the control-to-output voltage responses of a two-module converter. Results from the detailed cycle-by-cycle simulations are in good agreement with the predictions of the mathematical model up to half the switching frequency.

Keywords— Current-mode control, Modular dc-dc converters, Small-signal modelling.

I. INTRODUCTION

The modular approach in designing dc-dc converters is increasingly gaining importance in the field of power electronics. With this approach, two or more single-cell converters are connected in a variety of arrangements to fulfil system input/output requirements that cannot be efficiently met by a single converter. As one of these arrangements, the parallel-input/series- output (PISO) architecture is suitable for high-output voltage applications such as photovoltaic systems, fuel cell systems, wind energy systems, and dedicated switched-mode dc power supplies. The major advantage of the PISO structure is that the voltage and current stresses on the circuit components of the participating modules can be reduced.

Various dc-dc converter topologies like the buck-based, the boost-based, and the buck-boost-based have been used for the constituent modules of the PISO converters. Several control schemes with a variable degree of complexity have been proposed for the control of these converters [1]-[18]. One of these schemes adopts the peak current-mode control (CMC) technique which is widely used for controlling single-cell converters due to its advantages over the voltage-mode (duty-ratio) control such as better line-noise rejection, improved dynamics, and automatic overload protection. However, all the published works on peak CMC PISO converters [2], [3], [8], [10], [11] have studied the system dynamics under the assumption that the constituent modules are identical.

To preliminarily investigate the dynamics of dc-dc converters, many researchers and power supply designers depend on small-signal models. Averaging techniques such as state-space averaging [19] and circuit averaging [20] are well-established methods to construct small-signal models for the power stages of single-cell dc-dc converters; they are covered in many power electronics textbooks such as [21], [22]. State-space averaging replaces the separate state equations that govern each mode of the converter's operation with a single state-space description by taking a time-weighted average of these equations. The circuit averaging technique, however, involves manipulations of circuits instead of equations such that the

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converter circuit connections do not vary with time. This is done by first replacing the switching elements in the circuit with dependent voltage and current sources whose waveforms are defined to be identical to the original switch waveforms, averaging the waveforms over one switching cycle [21].

In addition to the power-stage model, CMC converters require a CMC-stage law to be included into the development of the small-signal model. This can be done either algebraically by augmenting the power-stage state-space matrices or a current-sensing network interfaced with the power-stage model.

With the growing interest in PISO dc-dc converters, more research into the dynamics and control of these converters is needed. Therefore, the objective of this paper is to extend previous work on the small-signal modelling of pulse-width modulated (PWM) peak CMC buck-derived PISO converters operated in the continuous-conduction mode. A state-space-based small-signal model that allows the control of each module individually is derived. Parasitic elements and the sampling effect of the module current loop are included in the derivation. A special case of interest regarding the effect of mismatch between output-filter inductors on the control-to-output voltage responses of a two-module converter is investigated. The proposed model is verified using PSIM cycle-by-cycle simulation.

The following sections of this work are organized as follows: Section (II) presents the small-signal modelling of the power and the CMC stages of a two-module PISO buck-based dc-dc converter. In Section (III), the resultant model is used to study the control-to-output voltage responses with mismatched inductors. Section (IV) discusses the module output voltage responses under closed-loop conditions. Section (V) is left for the conclusion.

II. SMALL-SIGNAL MODELLING

Fig. 1 shows a two module peak CMC PISO buck-based converter. Each module has its own current and voltage feedback circuits for increased-system reliability. The converter box in the figure represents a suitable transformer-isolated buck-derived topology whose role is to apply a variable duty-ratio waveform to the respective low-pass filter.

The control of each module of Fig. 1 can be explained using the idealized waveforms of Fig. 2: Module inductor current (i_L) is sensed by a resistor (R_i) and compared to a control voltage (V_e), generated by the voltage feedback circuit. Effective duty ratio (D) is determined when the sensed inductor current (i_L*R_i) whose rising slope is [$M_1 = (V_S - V_O)$*R_i /L] reaches a peak value equal to V_e. A compensating ramp with slope (M_c) is used to eliminate instability when D> 0.5 [23]. The converter works in the continuous-current mode; the inductance and switching cycle (T) are chosen such that i_L never gets to zero. CMC results in an inner (current) loop that regulates the inductor current. The controller in the outer (voltage) loop generates the value of V_e needed to regulate the output voltage (V_o) at a desired value.

A) Power-Stage Modelling

The power-stage small-signal model of the single-module buck converter is well established (see for example [22]). Each module of the converter under consideration is treated as a single buck circuit with the following assumptions: a) ideal switching devices; b) module isolation transformer with a unity turns ratio. With these assumptions, the power-stage small-signal model of the two-module converter is shown in Fig. 3, where ($V_s\ \hat{d}_1$) and ($V_s\ \hat{d}_2$) represent small AC changes in the effective duty ratio of module 1 and module 2 respectively, while ($D_1\ \hat{v}_s$) and ($D_2\ \hat{v}_s$) denote the effects of small AC changes in the supply voltage on modules 1 and 2 respectively. A current source is connected across the load to include the effect of

changes in load current. Two parasitic elements are considered: the capacitor equivalent series resistance (R_C) and inductor internal resistance (R_L).

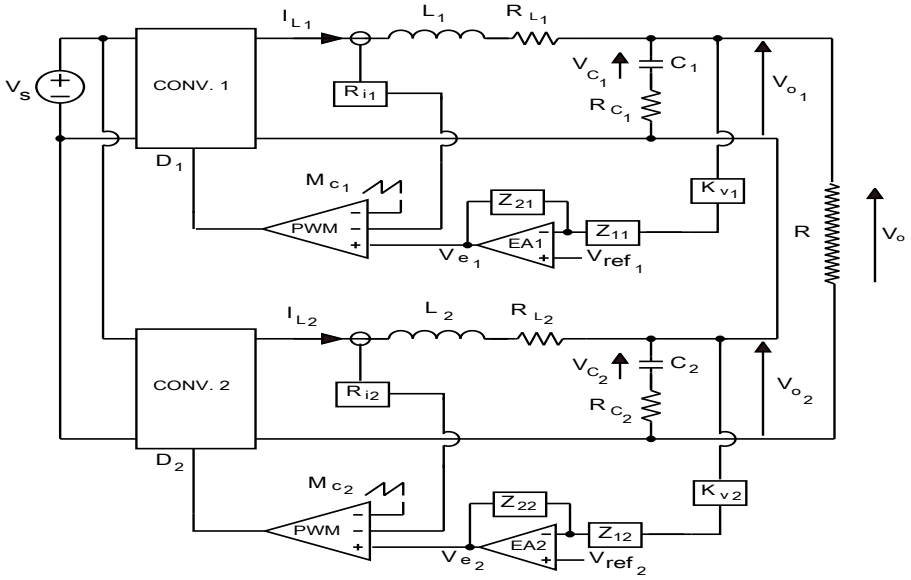


Fig.1. Schematic of the peak current-mode controlled two-module dc-dc converter

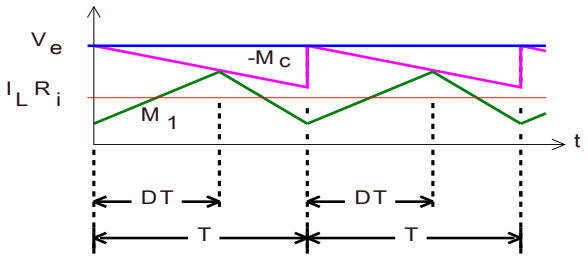


Fig. 2. Control voltage, stabilizing ramp, and sensed inductor current at steady state

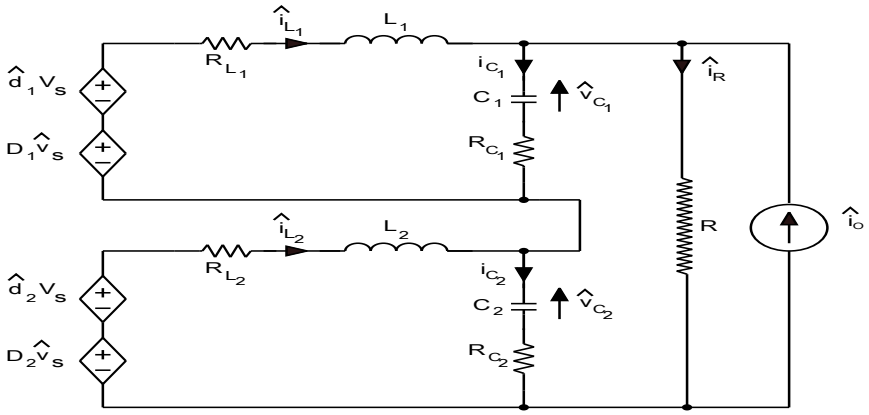


Fig. 3 Schematic of the circuit used for power stage modelling

Using circuit equations, the state-space matrix representing the power stage can be expressed as:

$$\dot{\hat{\mathbf{x}}} = \frac{d}{dt}\begin{bmatrix}\hat{\imath}_{L1}\\ \hat{v}_{c1}\\ \hat{\imath}_{L2}\\ \hat{v}_{c2}\end{bmatrix} = \begin{bmatrix}a_{11} & a_{12} & a_{13} & a_{14}\\ a_{21} & a_{22} & a_{23} & a_{24}\\ a_{31} & a_{32} & a_{33} & a_{34}\\ a_{41} & a_{42} & a_{43} & a_{44}\end{bmatrix}\begin{bmatrix}\hat{\imath}_{L1}\\ \hat{v}_{c1}\\ \hat{\imath}_{L2}\\ \hat{v}_{c2}\end{bmatrix} + \begin{bmatrix}b_{11} & 0 & b_{13} & b_{14}\\ 0 & 0 & 0 & b_{24}\\ 0 & b_{32} & b_{33} & b_{34}\\ 0 & 0 & 0 & b_{44}\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\\ \hat{v}_s\\ \hat{\imath}_o\end{bmatrix} \quad (1)$$

where

$$a_{11} = -\left(\frac{R_{L1}}{L_1} + \frac{R_{C1}(R_{C2}+R)}{L_1 R_S}\right);\ a_{12} = \frac{-(R_{C2}+R)}{L_1 R_S};\ a_{13} = \frac{(R_{C1}R_{C2})}{L_1 R_S};\ a_{14} = \frac{R_{C1}}{L_1 R_S} \quad (2a)$$

$$a_{21} = \frac{(R_{C2}+R)}{C_1 R_S};\ a_{22} = a_{24} = \frac{-1}{C_1 R_S};\ a_{23} = \frac{-R_{C2}}{C_1 R_S} \quad (2b)$$

$$a_{31} = \frac{(R_{C1}R_{C2})}{L_2 R_S};\ a_{32} = \frac{R_{C1}}{L_2 R_S};\ a_{33} = -\left(\frac{R_{L2}}{L_2} + \frac{R_{C2}(R_{C1}+R)}{L_2 R_S}\right);\ a_{34} = \frac{-(R_{C1}+R)}{L_2 R_S} \quad (2c)$$

$$a_{41} = \frac{-R_{C1}}{C_2 R_S};\ a_{42} = a_{44} = \frac{-1}{C_2 R_S};\ a_{43} = \frac{(R_{C1}+R)}{C_2 R_S} \quad (2d)$$

$$b_{11} = \frac{V_s}{L_1};\ b_{13} = \frac{D_1}{L_1};\ b_{14} = \frac{-RR_{C1}}{L_1 R_S};\ b_{24} = \frac{R}{C_1 R_S} \quad (2e)$$

$$b_{32} = \frac{V_s}{L_2};\ b_{33} = \frac{D_2}{L_2};\ b_{34} = \frac{-RR_{C2}}{L_2 R_S};\ b_{44} = \frac{R}{C_2 R_S} \quad (2f)$$

where the symbol (^) represents small-signal variations; and $R_S = R + R_{C1} + R_{C2}$. The small-signal model represented by (1) is suitable for the control of each module individually.

B) CMC-Stage Modelling

The "New Continuous Time" technique [23] for the small-signal modelling of single-cell PWM peak CMC dc-dc converters is widely accepted and will be adopted for this work. Based on this technique, the small-signal model of the converter under consideration is shown in Fig. 4. For each module, the model includes: the modulator gain F_m, the sampling gain of the current loop H_L, and the feedforward gains H_S and H_O created when the current feedback path is closed.

- ***Module pulse-width modulator gain***

The modulator gains of module 1 and module 2 can be respectively written as

$$F_{m1} = \frac{1}{(M_{11}+M_{C1})T} = \frac{1}{\left(\frac{R_{i1}(V_S-V_{O1})}{L_1}+M_{C1}\right)T} \quad (3a)$$

$$F_{m2} = \frac{1}{(M_{12}+M_{C2})T} = \frac{1}{\left(\frac{R_{i2}(V_S-V_{O2})}{L_2}+M_{C2}\right)T} \quad (3b)$$

The time delay caused by the modulation process introduces an exponential term in the PWM modulator gain; the effect of this delay on CMC stability has been investigated in [24]. It reduces the maximum duty ratio, before current loop instability occurs, from 0.5 to around 0.36. However, this only happens if no external compensation ramp is used. With such a ramp, the PWM delay effect on system stability can be neglected.

- ***Sampling gain of the module current loop***

The CMC converter can be considered as a sample-and-hold system [23]. Sampling gain is approximated by a double right-hand plane zero at half the switching frequency. For module 1 and module 2, the sampling gains are respectively

$$H_{L1} \cong R_{i1}\left(1+\frac{s}{\omega_n Q_z}+\frac{s^2}{\omega_n^2}\right) \tag{4a}$$

$$H_{L2} \cong R_{i2}\left(1+\frac{s}{\omega_n Q_z}+\frac{s^2}{\omega_n^2}\right) \tag{4b}$$

where $Q_z = -2/\pi$ and $\omega_n = \pi/T$

- ***Input voltage feedforward gain***

A Feedforward gain of the input voltage is created when the module current loop is closed. An improvement to the feedforward gain of [23] is presented in the analysis of [25]. It adds a high-frequency zero to the gain proposed in [23]. The input voltage feedforward gains of module 1 and module 2 can be respectively expressed as:

$$H_{S1} = \frac{TR_{i1}}{2L_1} - \frac{D_1^2 T^2 R_{i1}(3-2D_1)}{12L_1}s \tag{5a}$$

$$H_{S2} = \frac{TR_{i2}}{2L_2} - \frac{D_2^2 T^2 R_{i2}(3-2D_2)}{12L_2}s \tag{5b}$$

- ***Output voltage feedforward gain***

When the module current loop is closed, a feedforward gain of the output voltage is also created. The output voltage feedforward gains of module 1 and module 2 are respectively:

$$H_{o1} = \frac{(1-D_1)^2 TR_{i1}}{2L_1} \tag{6a}$$

$$H_{o2} = \frac{(1-D_2)^2 TR_{i2}}{2L_2} \tag{6b}$$

Referring to the block diagram of Fig. 4, the duty ratio laws of module 1 and module 2 are

$$\hat{d}_1 = F_{m1}(\hat{v}_{e1} - H_{L1}\hat{\imath}_{L1} + H_{s1}\hat{v}_s + H_{o1}\hat{v}_{o1}) \tag{7a}$$

$$\hat{d}_2 = F_{m2}(\hat{v}_{e2} - H_{L2}\hat{\imath}_{L2} + H_{s2}\hat{v}_s + H_{o2}\hat{v}_{o2}) \tag{7b}$$

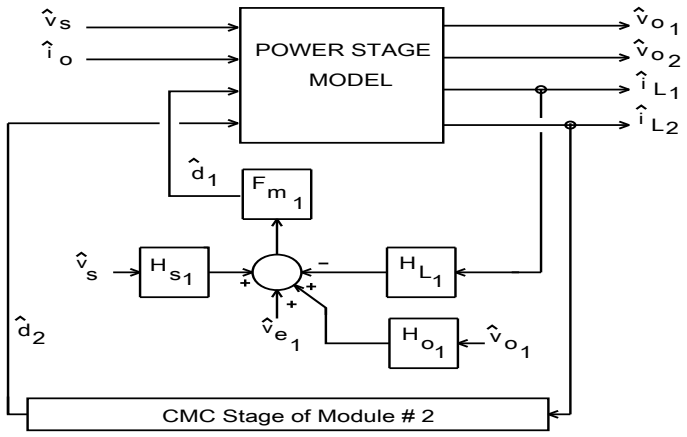


Fig. 4. Small-signal model of the power and CMC stages

Applying Laplace transforms to (1), and substituting for each module its respective duty ratio given by (7), we get

$$\begin{bmatrix} s\hat{\imath}_{L1} \\ s\hat{v}_{c1} \\ s\hat{\imath}_{L2} \\ s\hat{v}_{c2} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} & A_{14} \\ A_{21} & A_{22} & A_{23} & A_{24} \\ A_{31} & A_{32} & A_{33} & A_{34} \\ A_{41} & A_{42} & A_{43} & A_{44} \end{bmatrix} \begin{bmatrix} \hat{\imath}_{L1} \\ \hat{v}_{c1} \\ \hat{\imath}_{L2} \\ \hat{v}_{c2} \end{bmatrix} + \begin{bmatrix} B_{11} & 0 & B_{13} & B_{14} \\ 0 & 0 & 0 & B_{24} \\ 0 & B_{32} & B_{33} & B_{34} \\ 0 & 0 & 0 & B_{44} \end{bmatrix} \begin{bmatrix} \hat{v}_{e1} \\ \hat{v}_{e2} \\ \hat{v}_s \\ \hat{\imath}_o \end{bmatrix} \tag{8}$$

where

$$A_{11} = a_{11} - \frac{V_s F_{m1}}{L_1}(H_{L1} - a_{21}R_{c1}C_1H_{o1})\ ;\ A_{12} = a_{12} + \frac{V_s F_{m1}}{L_1}H_{o1}(1 + a_{22}R_{c1}C_1) \tag{9a}$$

$$A_{13} = a_{13} + a_{23}R_{c1}C_1\frac{V_s F_{m1}}{L_1}H_{o1}\ ;\ A_{14} = a_{14} + a_{24}R_{c1}C_1\frac{V_s F_{m1}}{L_1}H_{o1} \tag{9b}$$

$$A_{21} = a_{21}\ ;\ A_{22} = a_{22}\ ;\ A_{23} = a_{23}\ ;\ A_{24} = a_{24} \tag{9c}$$

$$A_{31} = a_{13} + a_{41}R_{c2}C_2\frac{V_s F_{m2}}{L_2}H_{o2}\ ;\ A_{32} = a_{32} + a_{42}R_{c2}C_2\frac{V_s F_{m2}}{L_2}H_{o2} \tag{9d}$$

$$A_{33} = a_{33} - \frac{V_s F_{m2}}{L_2}(H_{L2} - a_{43}R_{c2}C_2H_{o2})\ ;\ A_{34} = a_{34} + \frac{V_s F_{m2}}{L_2}H_{o2}(1 + a_{44}R_{c2}C_2) \tag{9e}$$

$$A_{41} = a_{41}\ ;\ A_{42} = a_{42}\ ;\ A_{43} = a_{43}\ ;\ A_{44} = a_{44} \tag{9f}$$

$$B_{11} = \frac{V_s F_{m1}}{L_1}\ ;\ B_{13} = \frac{D_1 + V_s F_{m1} H_{S1}}{L_1}\ ;\ B_{14} = b_{14}(1 - V_s F_{m1} H_{o1})\ ;\ B_{24} = b_{24} \tag{9g}$$

$$B_{32} = \frac{V_s F_{m2}}{L_2}\ ;\ B_{33} = \frac{D_2 + V_s F_{m2} H_{S2}}{L_2}\ ;\ B_{34} = b_{34}(1 - V_s F_{m2} H_{o2})\ ;\ B_{44} = b_{44} \tag{9h}$$

where F_m, H_L, H_S and H_O are given by (3), (4), (5), and (6) respectively.

Equation (8) represents the small-signal model of the two-module converter with current loops closed and voltage loops open.

III. CONTROL-TO-OUTPUT VOLTAGE RESPONSES

A) Response with Identical Inductors

The control-to-output voltage response is of interest because it is a useful tool for designing the voltage feedback loop controller. Since each module has independent current and voltage feedback loops, we will choose one of the two modules (say module 1); and study the effect of the filter inductor mismatch on its control-to-output voltage response$\left(\frac{\hat{v}_{o1}}{\hat{v}_{e1}}\right)$. It is appropriate, however, to first inspect the case when the two inductors are identical before comparing the response with that of the mismatched inductors.

Referring to the converter of Fig. 1, we have:

$$v_{o1} = v_{c1} + sv_{c1}C_1R_{c1} \tag{10}$$

Therefore, the control-to-output voltage of module 1 is:

$$\frac{\hat{v}_{o1}}{\hat{v}_{e1}} = \frac{\hat{v}_{c1}}{\hat{v}_{e1}}(1 + sC_1R_{c1}) \tag{11}$$

The system represented by (8) is solved for$\left(\frac{\hat{v}_{c1}}{\hat{v}_{e1}}\right)$; and by using (11) the transfer function $\left(\frac{\hat{v}_{o1}}{\hat{v}_{e1}}\right)$ is obtained and programmed into Matlab with the following parameters:

V_S= 180 V; V_{O1}= V_{O2}=126 V; R= 40 Ω; T= 10 μs; L_1= L_2= 300 μH

R_{L1}= R_{L2}= 20 mΩ; C_1= C_2= 1.25 μF; R_{C1}= R_{C2}= 50 mΩ; R_{i1}= R_{i2}= 0.1 Ω

Inductance and capacitance values are chosen such that the percentage peak-to-peak output voltage ripple $\Delta V_{O1}/V_{O1}$= $\Delta V_{O2}/V_{O2}$= 1% and the percentage peak-to-peak inductor current ripple $\Delta I_{L1}/I_{L1}$= $\Delta I_{L2}/I_{L2}$= 20%.

The control-to-output voltage responses are depicted in Fig. 5, with compensating ramp amplitudes V_{ramp}= 0.18 V and 0.5 V. These values of V_{ramp} are chosen to demonstrate the underdamped and damped responses as clarified below by calculations. Matlab pole-zero locations and damping ratios are given in Table 1.

With V_{ramp}= 0.18 V, Table 1 shows that after pole-zero cancellation, the behavior at low frequencies is influenced by a real left-hand plane (LHP) zero located between two real LHP poles. At high frequencies, there is a real LHP zero at $1/(C_1R_{C1})$. In addition, there is a complex pole at half the switching frequency (f_S/2) which is responsible for the peaking observed. This double pole is due to the sampling effect of the current loop. The Q of this second-order pole is controlled, as in peak CMC single-cell buck dc-dc converter, by using the compensation ramp.

With V_{ramp}= 0.5 V, critical damping of the second-order pole is achieved. Table 1 shows that by increasing V_{ramp} to 0.5 V, the double pole splits into two real ones: One of these poles moves towards the low-frequency region; and the other to frequencies beyond f_S/2. The following equation can be used to determine the size of ramp required to prevent the peaking at f_S/2:

$$Q = \frac{1}{\pi[(1-D)(1+M_c/M_1)-0.5]} \tag{12}$$

To check the damping ratio predicted by Matlab when V_{ramp}= 0.18 V, we have:

$$\frac{M_{c1}}{M_{11}} = \frac{M_{c2}}{M_{12}} = \frac{0.18/(10\times10^{-6})}{0.1(180-126)/(300\times10^{-6})} = 1 \quad (13)$$

From (12)

$$Q = \frac{1}{\pi[(1-0.7)(1+1)-0.5]} \approx 3.18 \quad (14)$$

Hence, damping ratio= 0.5/Q≈ 0.157, which is close to Matlab result of 0.153. Note that the double zero cancels out with the nearest double pole.
Now, with V_{ramp}= 0.5 V, we have

$$\frac{M_{c1}}{M_{11}} = \frac{M_{c2}}{M_{12}} = \frac{0.5/(10\times10^{-6})}{0.1(180-126)/(300\times10^{-6})} \approx 2.78 \quad (15)$$

and

$$Q = \frac{1}{\pi[(1-0.7)(1+2.78)-0.5]} \approx 0.5 \quad (16)$$

giving a damping ratio of 1, which also agrees with Matlab result.
To validate the model results, a two-module PISO buck-derived converter is implemented using PSIM as Fig. 6 shows. The chosen buck-derived topology is the well-known full-bridge inverter with transformer isolation followed by a full-bridge rectifier. Fig. 7 shows PSIM "ac sweep" results. The "ac sweep" facility allows users to obtain frequency responses with the circuit being in its original switched-mode form. Good agreement can be observed between the derived model results and PSIM simulations up to half the switching frequency.

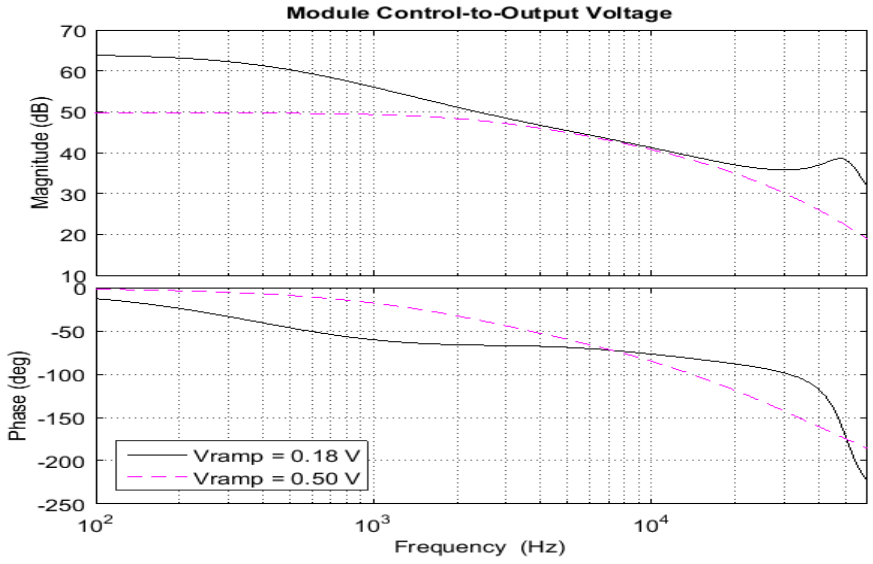


Fig. 5. Derived model results showing module control-to-output voltage responses when identical inductors are used with V_{ramp}= 0.18V and V_{ramp}= 0.5V

TABLE 1
MATLAB POLE-ZERO LOCATIONS (IDENTICAL INDUCTORS CASE)

	Under-damped Response (Ramp Amplitude= 0.18V)		Damped Response (Ramp Amplitude= 0.50V)	
		Damping ratio		Damping ratio
Zeros	-1.6e+07 -48246 + 3.1299e+05i -48246 - 3.1299e+05i -22286		-1.6e+07 -3.6722e+05 -2.3963e+05 -41434	
Poles	-2.63e+03 -4.19e+04 -4.81e+04 + 3.13e+05i -4.81e+04 - 3.13e+05i -4.84e+04 + 3.13e+05i -4.84e+04 - 3.13e+05i	1.00e+00 1.00e+00 1.52e-01 1.52e-01 1.53e-01 1.53e-01	-1.88e+04 -6.48e+04 -2.35e+05 -2.44e+05 -3.66e+05 -3.69e+05	1.00e+00 1.00e+00 1.00e+00 1.00e+00 1.00e+00 1.00e+00

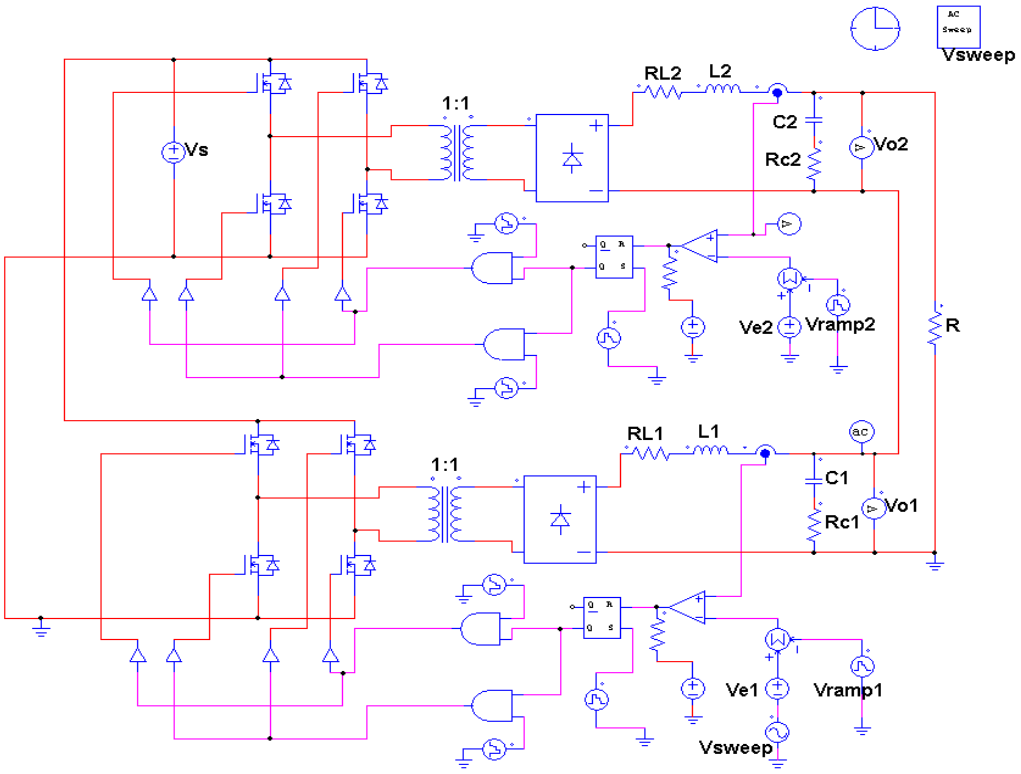


Fig. 6. PSIM schematic of the two-module buck-derived converter

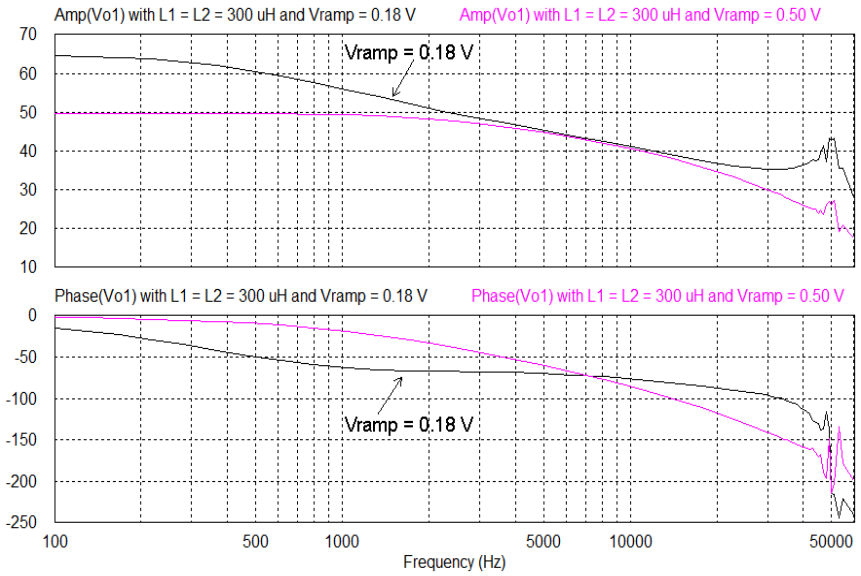


Fig. 7. PSIM results showing module control-to-output voltage responses when identical inductors are used with V_{ramp}= 0.18V and V_{ramp}= 0.5V

B) Response with Mismatched Inductors

To study the effect of inductor mismatch, one of the two inductors is given an inductance value of 360 µH (20% higher than nominal value of 300 µH). Inductance tolerances can be less than this, but the worst-case scenario is behind this choice.

Two cases regarding the location of the mismatched inductors are considered:

Case (1): Module #1 has an inductor with the highest value (L_1= 360 µH; L_2= 300 µH)

Case (2): Module #2 has an inductor with the highest value (L_1= 300 µH; L_2= 360 µH)

- ***Response with V_{ramp}= 0.18V***

Fig. 8 shows the derived-model results for cases (1) and (2) when V_{ramp}= 0.18V. The response when identical inductors are used is also plotted for comparison. Matlab pole-zero locations and damping ratios are given in Table 2. From Fig. 8, it can be observed that the 20% mismatch in inductance values causes small changes in the magnitude and phase responses at low frequencies. A more noticeable change can be seen at high frequencies for the case when L_1= 360 µH and L_2= 300 µH. The slope ratio for this case is

$$\frac{M_{c1}}{M_{11}} = \frac{0.18/T}{R_{i1}(V_s - V_{o1})/L_1} = \frac{0.18/(10\times10^{-6})}{0.1(180-126)/(360\times10^{-6})} = 1.2 \quad (17)$$

and

$$Q = \frac{1}{\pi[(1-0.7)(1+1.2)-0.5]} \approx 1.99 \quad (18)$$

giving a damping ratio≈ 0.251, which is close to the damping ratio of 0.245 predicted by Matlab.

To support the mathematical model results, responses generated by PSIM ac sweep are given in Fig. 9 which shows a good agreement with the derived-model results up to half the switching frequency.

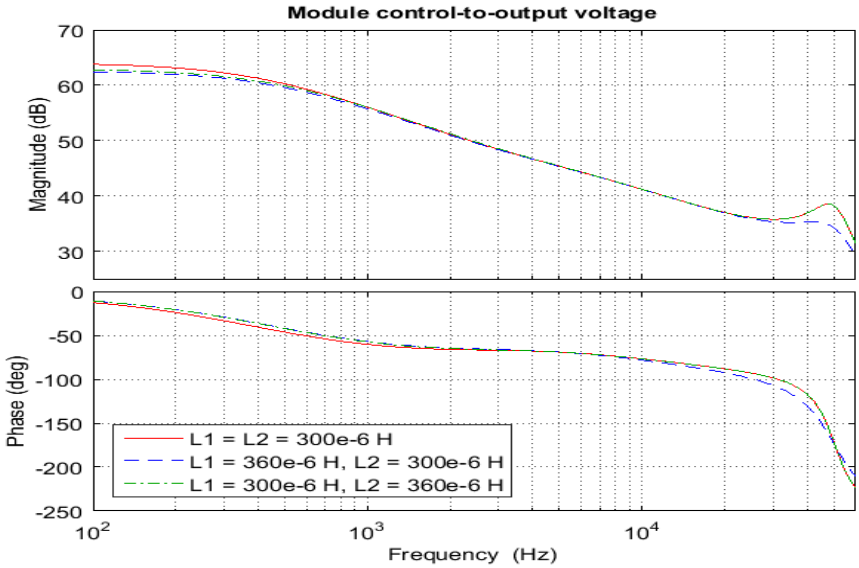


Fig. 8. Derived model results showing module control-to-output voltage responses when identical and mismatched inductors are used with V_{ramp}= 0.18V

TABLE 2
MATLAB POLE-ZERO LOCATIONS (V_{ramp}= 0.18V)

	L_1= 360 µH L_2= 300 µH	Damping ratio	L_1= 300 µH L_2= 360 µH	Damping ratio
Zeros	-1.6e+07 -48246 + 3.1299e+05i -48246 - 3.1299e+05i -22286		-1.6e+07 -77345 + 3.0619e+05i -77345 - 3.0619e+05i -23288	
Poles	-3.08e+03 -4.24e+04 -7.74e+04 + 3.06e+05i -7.74e+04 - 3.06e+05i -4.83e+04 + 3.13e+05i -4.83e+04 - 3.13e+05i	1.00e+00 1.00e+00 2.45e-01 2.45e-01 1.52e-01 1.52e-01	-3.08e+03 -4.24e+04 -7.74e+04 + 3.06e+05i -7.74e+04 - 3.06e+05i -4.83e+04 + 3.13e+05i -4.83e+04 - 3.13e+05i	1.00e+00 1.00e+00 2.45e-01 2.45e-01 1.52e-01 1.52e-01

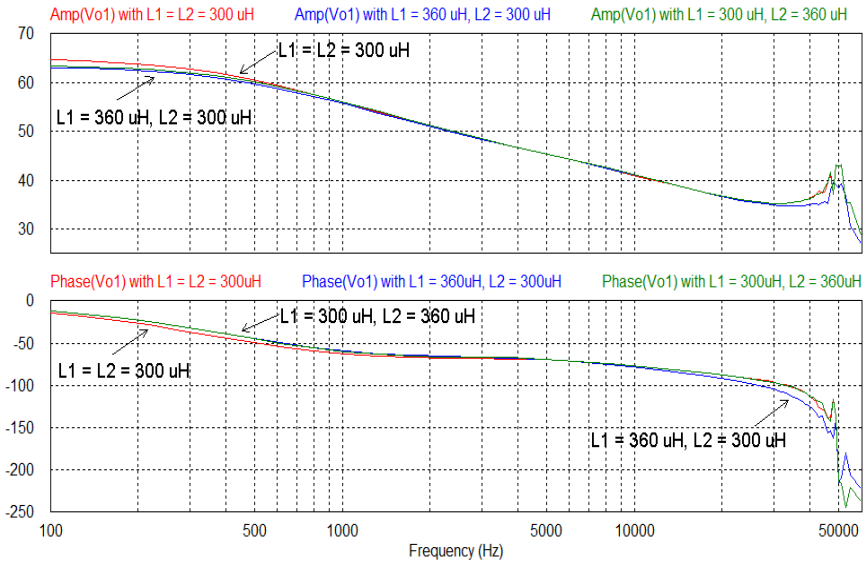


Fig. 9. PSIM results showing module control-to-output voltage responses when identical and mismatched inductors are used with V_{ramp}= 0.18V

- ***Response with V_{ramp}= 0.5V***

Fig. 10 illustrates the model results for Cases (1) and (2) when V_{ramp}= 0.5 V. Matlab pole-zero locations are given in Table 3. The response with identical modules is also plotted for comparison. The figure shows a slight decrease in the low-frequency gain when mismatched inductors are used. The figure also shows an overdamped response for the case (L_1= 360 µH and L_2= 300 µH). The slope ratio for this case is now

$$\frac{M_{c1}}{M_{11}} = \frac{0.5/T}{R_{i1}(V_s - V_{o1})/L_1} = \frac{0.5/(10\times10^{-6})}{0.1(180-126)/(360\times10^{-6})} \approx 3.33 \quad (19)$$

and

$$Q = \frac{1}{\pi[(1-0.7)(1+3.33)-0.5]} \approx 0.4 \quad (20)$$

and the damping ratio= 1.25. Table 3, however, indicates a damping ratio of 1 because the roots of the denominator are all first-order poles.

Fig. 11 depicts the responses generated by PSIM ac sweep when V_{ramp}= 0.5V. It has a good agreement with the mathematical model results up to half the switching frequency.

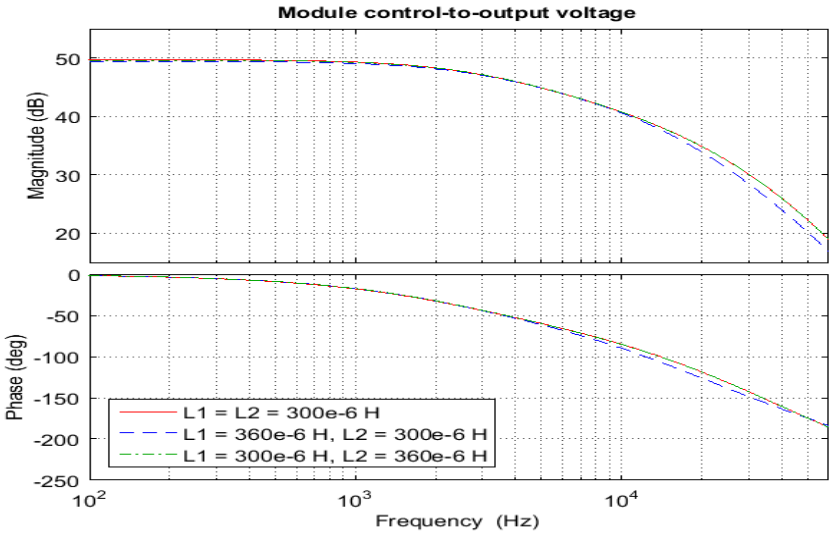


Fig. 10. Derived model results showing module control-to-output voltage responses when identical and mismatched inductors are used with V_{ramp}= 0.5V

TABLE 3
MATLAB POLE-ZERO LOCATIONS (V_{ramp}= 0.5V)

	L_1= 360 µH L_2= 300 µH	Damping ratio	L_1= 300 µH L_2= 360 µH	Damping ratio
Zeros	-1.6e+07 -3.6722e+05 -2.3963e+05 -41434		-1.6e+07 -6.4135e+05 -1.2573e+05 -46300	
Poles	-6.4135e+05 -3.6729e+05 -2.393e+05 -1.2323e+05 -70624 -19821	1.00e+00 1.00e+00 1.00e+00 1.00e+00 1.00e+00 1.00e+00	-6.4135e+05 -3.6729e+05 -2.393e+05 -1.2324e+05 -70623 -19819	1.00e+00 1.00e+00 1.00e+00 1.00e+00 1.00e+00 1.00e+00

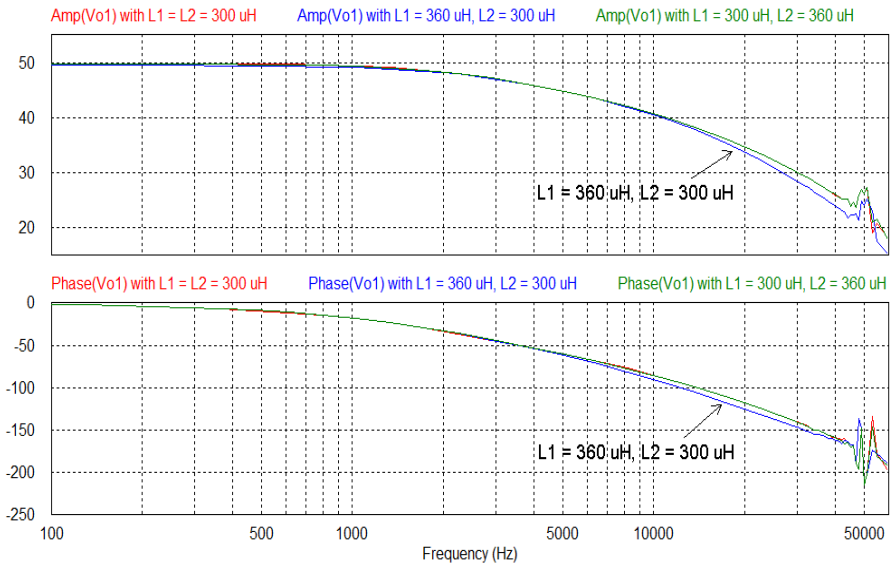


Fig. 11. PSIM results showing module control-to-output voltage responses when identical and mismatched inductors are used with V_{ramp}= 0.50V

IV. CLOSING THE VOLTAGE FEEDBACK LOOPS

The voltage feedback controller design is based on the control-to-output voltage response when critical damping is achieved (i.e. when V_{ramp}= 0.5V). A usual design practice is to choose a crossover frequency for the control loop such that it does not exceed 1/10 of the switching frequency. A controller design based on the assumption that the two inductors are identical will also be suitable for the mismatched cases discussed above. This is so, because the control-to-output responses with mismatched inductors have small deviations from those of the identical inductors over the approximate range 0.1 kHz to 8 kHz as Fig. 11 shows. This range becomes narrower if mismatch increases. For example, a hypothetical mismatch of 50% between the two inductors reduces the bandwidth to around 4 kHz.

PSIM "smart control" facility is employed to design the module voltage feedback controller. A type-2 controller (modified PI controller) is chosen for this purpose. A loop crossover frequency of 8 kHz and a phase margin of 60^o are given as input data for PSIM. A schematic of the controller generated by "smart control" is given in Fig. 12. The closed-loop output voltage and inductor current responses of each module due to ±3A step changes in load current are plotted in Figs. 13 and 14 respectively. The figures compare the responses for three cases, namely (L_1= L_2= 300 µH), (L_1= 360 µH; L_2= 300 µH), and (L_1= 240 µH; L_2= 300 µH). The results demonstrate that the same controller can be used for both the identical and mismatched inductors cases. The two modules produce the same average output voltage at steady state. In other words, the two modules equally share the required DC load voltage. Fig. 13 also indicates an increase in output-voltage ripple when one of the inductors has a lower value than the nominal. This can be treated by resizing the filter capacitors. Although average inductor currents are equal, Fig. 14 shows a mismatch between the inductor current ripple amplitudes, and hence different rms values are expected. This will result in different power dissipation in resistive non-idealities among the modules. The difference in inductor current rms values can be quantified using the following equations which can be found in any textbook on switched-mode dc-dc converters.

$$(I_L)_{rms} = \sqrt{(I_o)^2 + \frac{1}{12}(\Delta I_L)^2} \quad (21)$$

where ΔI_L is the peak-to-peak inductor current ripple:

$$\Delta I_L = \left(\frac{V_s - V_o}{L}\right)\left(\frac{D}{f_s}\right) = \frac{V_s D(1-D)}{L f_s} \quad (22)$$

and I_O is the load current:

$$I_o = \frac{V_o}{R} = \frac{2DV_s}{R} \quad (23)$$

Using (21)-(23) for the case under consideration, a mismatch of 20% in inductance values will cause around 0.05% difference in the inductor current rms values at full load and around 0.2% at half load. These differences are insignificant when power dissipation in resistive non-idealities is calculated. It can be reduced if design constraints permit smaller inductor current ripple.

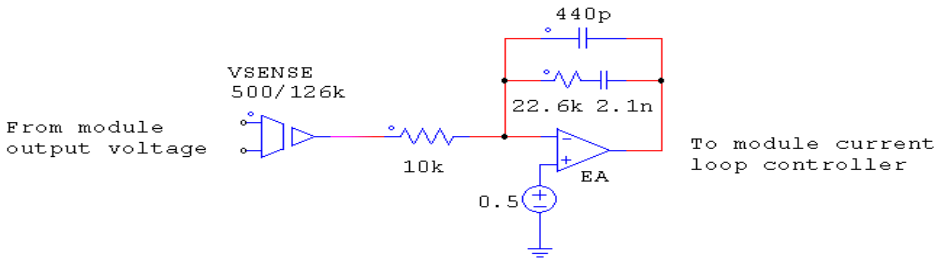
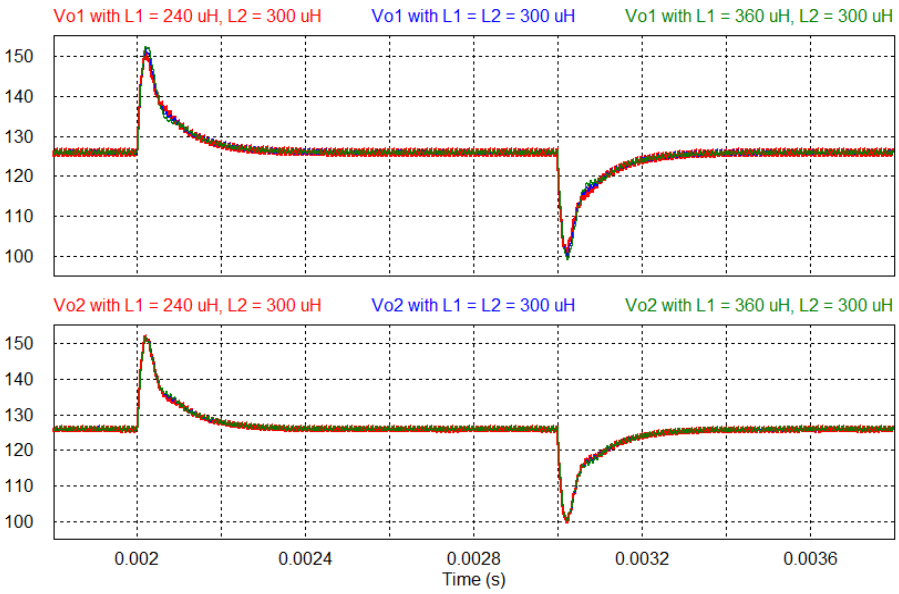


Fig. 12. Schematic of the module voltage feedback controller generated by PSIM

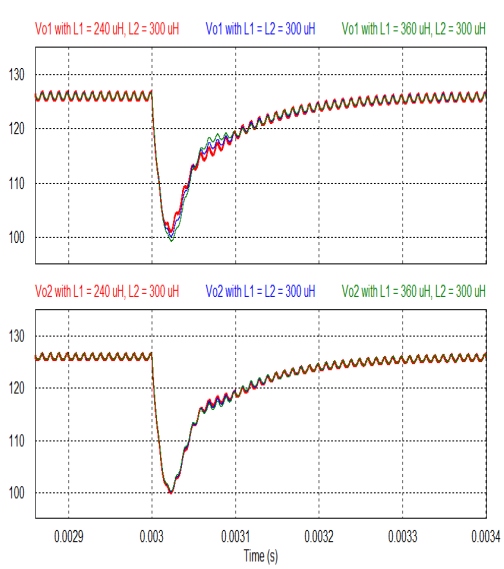
V. CONCLUSION

A more-detailed small-signal model is presented for the two-module peak current-mode controlled parallel-input/series-output buck-derived dc-dc converter operating in the continuous-conduction mode. Parasitic elements in addition to the current-loop sampling action have been included in the model derivation. The proposed model is employed to study the module control-to-output voltage responses of the converter with mismatched output filter inductors. The model predictions, confirmed by PSIM "ac sweep" simulations, have provided a useful tool for the voltage feedback control design.

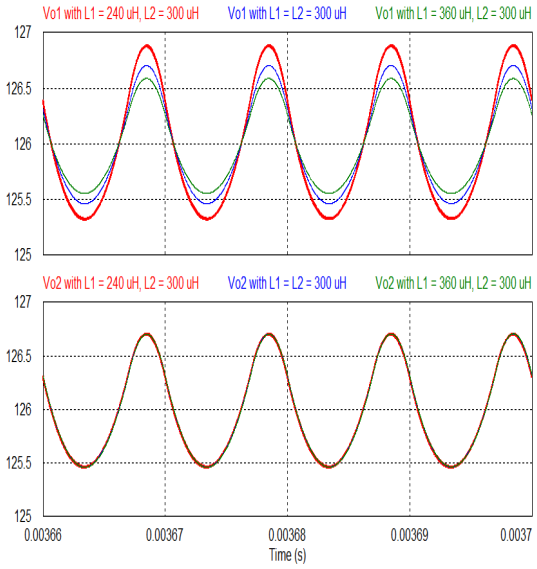
It has been found that a voltage controller design based on the assumption that the two output-filter inductors are identical will also be suitable for the case when a mismatch of ±20% exists between the inductors. Closed-loop cycle-by-cycle simulations following step changes in load current have shown that equal average output voltage sharing between the modules can still be maintained in the presence of mismatched inductors. The difference in output voltage ripple can be eliminated by resizing output-filter capacitors. However, the difference in the rms values of inductor currents due to the different inductor current ripples, although found insignificant for a standard design, may become an issue of concern if inductors of smaller sizes are employed.



(a)

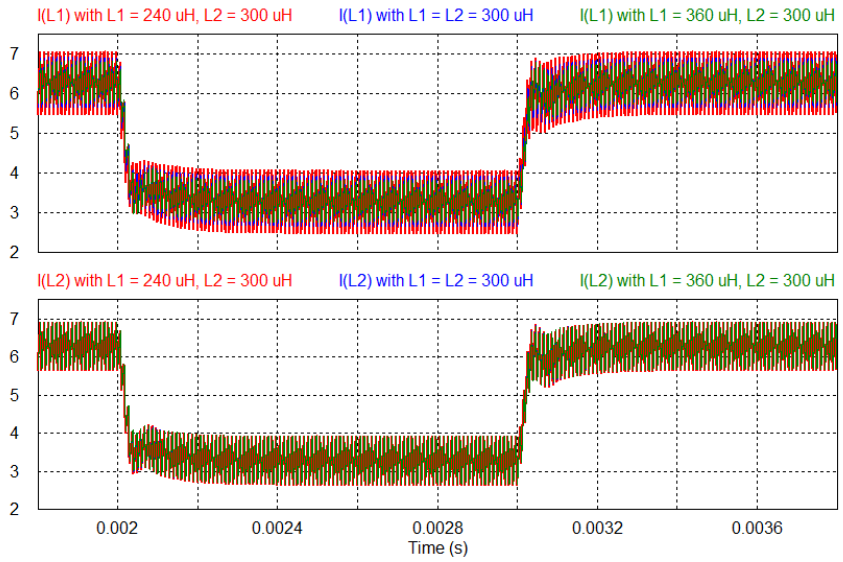


(b)

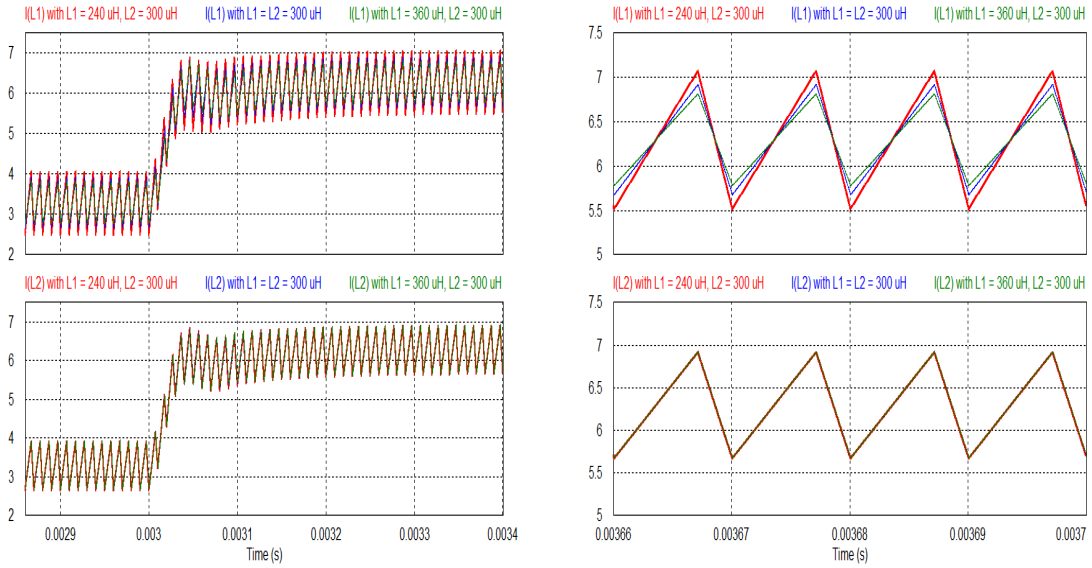


(c)

Fig. 13. a) Closed loop module output voltage responses due to ±3A step changes in load current, b) Zoom-in of Fig. 13a during transients, c) Zoom-in of Fig. 13a during steady state



(a)



(b) (c)

Fig. 14. a) Closed loop module inductor current responses due to ±3A step changes in load current, b) Zoom-in of Fig. 14a during transients; c) Zoom-in of Fig. 14a during steady state

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