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Fast Lock and Settling Time Improvement for Indirect Frequency Synthesizer Phase Locked Loop

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Abstract— Settling time is one of the major quality feature in phase locked loop frequency synthesizer (PLL-FS). Additionally, fast lock is very important for PLL in multiple applications. When PLL in lock range becomes as fast as possible, it gives no error in a comparison process; and the system works probably. In this paper, a new design of indirect Phase locked loop frequency synthesizer circuit is proposed to minimize the settling time at PLL-FS output signal when there is a sudden change in frequency. In this work, a great improvement is achieved to speed up the lock-in time of the circuit. The proposed design improves the settling time up to 80% at output frequency; and the lock- time speed is increased. ORCAD and MATLAB simulators are used to show the proposed design validity.

Keywords— CD4046B, fast lock, MATLAB, ORCAD, output frequency, PHSPLS output, PLL-FS, settling time, VCO output.

I. INTRODUCTION

The main function of Phase Locked Loop (PLL) is to acquire the lock by comparing its inputs and tracking it until there is no difference between inputs. So, PLL is usually used in modulation/demodulation processes to generate a stable and clean carrier signal [1].Fast lock or fast tracking to acquire lock in PLL frequency synthesizers is a significant challenge in modern communications devices and wireless communication systems, which speed up devices and turn them on/off. Furthermore, hopping the frequency from one value to another in mobile systems protects call or data from violation, interference, or interruption. So it is not only a necessity to acquire lock, but also to lock as fast as possible during frequency hopping [2], [3].

During switching from one frequency to another, a sudden change will occur, causing a ripple i.e. (overshoot) and settling time before returning to the steady state. Reducing the settling time and avoiding trade-off between settling time and maximum overshoot is very important to achieve stability and realize the steady state as much as possible.

PLL Frequency Synthesizer is used as a base band frequency source, and a wideband stable carrier frequency source. So, PLL is used in many applications such as data recovery circuits, clock generators, and wireless receivers in mobile, satellite, and GPS systems. It is used in wireless LAN 802.11.a and 802.11b receivers to improve their efficiency, bandwidth, and data rates [4], [5]. In cellular communications systems, Time Division Multiple Access (TDMA) technique uses frequency synthesizer in tuning to the next channel through a small time slot to realize fast lock time and stability in frequency [6].

In this paper, the key improvement is in developing an appropriate model to simulate indirect PLL FS by using ORCAD simulator and MATLAB simulator. In part I, the main purpose is to improve settling time and implement State-Space in MATLAB. Part II proposes a simulation model for PLL-FS using ORCAD by changing some parameters in order to

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improve lock time, and at the same time to realize fast lock time. On the other hand, in part II, the same ORCAD model is used; and a reduction in settling time at PLL-FS output signal is achieved. ORCAD represents an IC's simulator, which can estimate a very complicated IC's and parts. Such a simulator can provide the circuit design with easier performance and faster time than that spent in laboratory.

Many trials have been proposed to speed up the lock-in- time in PLL frequency synthesizers, and improve settling time. Vye in [6] introduced a practical design of 900 MHz PLL synthesizer based on an active loop filter design. Using system-level simulator with help of mathematical analysis demonstrated a 300μs locking time; and it gave a 905 MHz free-running oscillation frequency.

Additionally, Chou and Mou [7] proposed a new filter design method for PLL to achieve good transient response in settling time, overshoot, and bandwidth of noise. On the other hand, authors in [8] presented a design that gave a great reduction in the lock-in time and low power fast-settling frequency of PLL-FS by the 0.18μm CMOS process; this was achieved by developing a mixed signal LC voltage-controlled oscillator (VCO).

Kuang and Shoui [9] introduced a mixed-signal VCO with a direct frequency presetting circuit. This design speeded up the lock-in time and avoided tradeoff between the lock time and phase noise/spurs. Authors in [10] proposed a frequency estimator in (AWGN) conditions; the structure is proposed to solve the problems of conventional phase locked loop (PLL) problems such as overshoot, narrow tracking range, long settling time, double frequency ripples in the loop, and stability. The proposed architecture is designed and modeled using VHDL; and implemented using FPGA circuit.

Yan, Kuang, and Wu in [11] introduced a mixed signal VCO and a digital processor to switch between frequencies. The design results demonstrated less settling time than 3μs.

A novel feedback mechanism is proposed in [12] for PLL phase detectors using the estimated phase angle. The model could reduce the ripple by at least 50% and decrease the settling time of the PLL by 50%. Experimental results and mathematical analyses also were conducted to confirm this model.

Cheng and Rasavi in [13] proposed concepts in a 2.4-GHz RF CMOS synthesizer. The technique settled in approximately 60μs with 1-MHz channel spacing.

Authors in [14] introduced a new adaptive control technique applied on the reference frequency to get low noise and fast settling PLL. The loop bandwidth was enhanced by 16 times; and the fast settling time was reduced to 260μs.

In [15], the lock time is achieved at 12.8 μs over the entire tuning range by a fractional-N PLL synthesizer technique.

Authors in [16] presented novel techniques used in a fully digital frequency synthesizer to achieve<50μs settling time while maintaining an excellent phase noise. In summary, the techniques in all the aforementioned works were proposed to decrease the settling time and to speed up the lock time in a PLL frequency Synthesizer. In this paper, a model of FS-PLL is adopted to improve the lock speed and to acquire fast settling time. It is demonstrated that a small frequency step will decrease the settling time, i.e. by changing frequency step from 100 kHz to 20 kHz, there is an improvement on settling time by 80%. In general, there are two approaches for using PLL-FS model in ORCAD; the first approach seeks to improve the lock time, and speed up the lock-in time simultaneously. However, the second approach uses an external element to improve the settling time at VCO output through oscillation which gives an excellent improvement in settling time.

This paper is organized as follow: a PLL Frequency Synthesizer structure is introduced in section II. Section III presents a specification of the proposed computer simulations. Additionally, section IV analyzes the simulation results. Finally, section V introduces a conclusion.

II. PLL FREQUENCY SYNTHESIZER STRUCTURE

The basic structure of linear indirect PLL-FS in (S-domain) system is seen in Fig. 1. The block diagram of the PLL-FS consists of five main components, which are reference frequency source (F_{ref}), phase detector (PD), Low Pass Filter (LPF), VCO, and a fractional By-N circuit arranged as a feedback loop [17]. As shown in Fig. 1, k_{PD} is the phase detector gain (V/rad); and k_{vco} (Hz/V) is the voltage control oscillator gain. The output frequency is $F_{out}=N\cdot F_{ref}$, where N is the frequency division ratio.

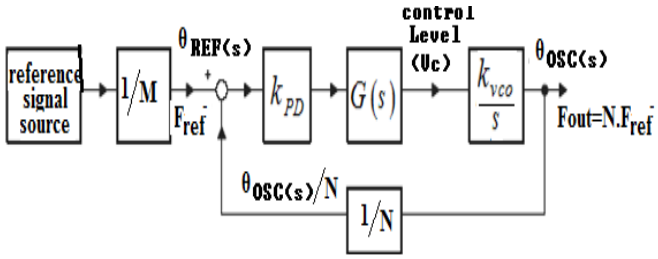

Fig. 1. Linear indirect frequency synthesizer phase locked loop

The product section or Phase detector is widely used in digital and analog systems. For digital signals, a phase detector may be an OR-gate, RS flip-flop, XOR-gates, or 3-states buffer. For analog signals, phase detector may be a modulator or a multiplier circuit [17]. A phase frequency detector mixes two inputs: the incoming reference signal frequency (F_{ref}), and the feedback frequency from voltage control oscillator after dividing it by the programmed value (N) at BY-N frequency divider section. F_{ref} is divided by the programmed value (M). M and N are the frequency division ratios. VCO frequency equals N times the reference frequency, and when N ratio is varied, the frequency error will be detected at phase detector. Output voltage of PD is proportional to the phase difference between its inputs. The phase detector controls the voltage that enters VCO input until the feedback frequency and reference frequency become matched. Then the system will be in lock range; and the locked condition is attempted as follows:

$$F_{ref}=F_{OSC}/N \tag{1}$$

where F_{OSC} is the VCO output frequency. VCO and phase detector are nonlinear devices. PLL is considered a nonlinear device. When PLL is in lock range, its performance is approximated to linear performance [6]. Linear PLL will increase its lock range [4]. So, firstly it is very important to adjust VCO device until it operates in a linear region. In addition, PD gain will be taken as a constant value. Therefore, the closed loop of PLL-FS is described by a linear transfer function in S-domain. For the circuit shown in Fig. 1, the transfer function H(s) can be given as follows:

$$H(s)=\frac{K_{PD}K_{VCO}G(s)}{S+\frac{K_{PD}K_{VCO}G(s)}{N}} \tag{2}$$

where G(s) is the transfer function of low pass filter; N is the frequency division ratio; K_{VCO} is the voltage controlled oscillator gain; and K_{PD} is the phase detector gain constant. In general K_{PD} is given as:

$$K_{PD} = \frac{(V_{OH} - V_{OL})}{4\pi} \tag{3}$$

where V_{OH} is the highest level of the Phase detector output voltage; and V_{OL} is the lowest level of the Phase detector output voltage.

Phase detector output is smoothed by a loop filter; it may be passive or active. Loop filter improves the lock range and the lock-in time speed. However, there are first, second, third, and upper order of loop filters. These types can be analyzed using their parameters; natural frequency (ω_n) and damping factor (ξ). The second order is the most common type that can be used in wireless communication applications [6], [7], [14].

LPF removes high frequency terms to clear noise influence. It can eliminate harmonic terms and ripple noise in the output signal before feeding back to the input [12]. Fig. 2 shows a passive LPF.

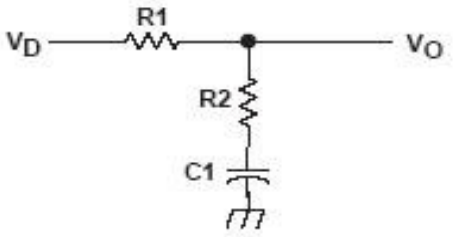

Fig. 2. Passive low pass filter

The LPF circuit in Fig. 2 has the first order transfer function G(s) that can be given as:

$$G(s) = \frac{Vo}{V_D} = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{4}$$

where $\tau_1=R_1C_1$, $\tau_2=R_2C_2$ are the loop filter time constants.

The output of a low pass filter implies the frequency and phase differences, i.e. (error) between the reference signal and feedback signal. This error controls the VCO oscillation. If the error is very small or equal zero, the VCO will produce the center frequency which equal F_{ref}. At this point, PLL will be in lock range. But if there is a difference between the two inputs signals, PLL lacks the lock range; and VCO will produce a frequency and consequently change the operating frequency [10]. At this moment, PLL tries to correct the error in phase and frequency, and make this error as small as possible to attain the lock-in time [6].

VCO is a resonance or tuning circuit, which can oscillate the range of frequencies. This range determines the overall system tuning range. Also, VCO oscillates the resonance frequency, which can be changed by Varactor diode that acts as a capacitor. This capacitor is varied by control voltage.

Usually, PLL order is greater than loop filter order by one [10], so it is expected that the PLL FS has the 2nd order transfer function. By substituting G(s) in (4) with (2), the PLL FS transfer function will be as follows:

$$H(s)=\frac{1+s\tau_2}{(\tau_1+\tau_2)s^2+(\frac{N+K\tau_2}{NK})s+\frac{1}{N}} \tag{5}$$

where $K=K_{PD}K_{VCO}$ is the PLL-FS closed loop overall gain. Rewriting (5) in terms of damping factor ξ and natural frequency ω_n is given as:

$$H(s)=\frac{(\frac{2\xi}{\omega_n}-\frac{N}{K})s+1}{(\frac{1}{\omega_n^2})s^2+(\frac{2\xi}{\omega_n})s+1} \tag{6}$$

where

$$\xi=\frac{1+K\tau_2}{2\sqrt{N(\tau_1+\tau_2)K}} \tag{7}$$

and

$$\omega_n=\sqrt{\frac{K}{N(\tau_1+\tau_2)}} \tag{8}$$

ξ represents the measure of stability, which is usually selected to be between 0.6-0.8. Increasing damping ratio ξ will decrease settling time [4]. Equation (7) indicates that there is an inverse relationship between the damping factor and division ratio N. Equations (5) and (6) show that changing N will force the loop to accept a sudden change in the output signal frequency. As a result, this sudden change causes phase disturbances, loop damping, missing of lock-in time, instability, or ripple in magnitude (or overshoot). Furthermore, settling time (T_s) is acquired before the steady state.

This work is going to examine the following things at the PLL-FS output frequency (F_{out}):

- The lock speed and time-in lock
- The settling time which can be either slow or fast according to multiple parameters in the closed loop.

III. COMPUTER SIMULATIONS

The practical circuit shown in Fig. 3 [17] seeks to reduce the maximum overshoot of the PLL-FS output signal. MATLAB is used to simulate this circuit in order to improve the settling time when a sudden change in PLL input frequency occurs.

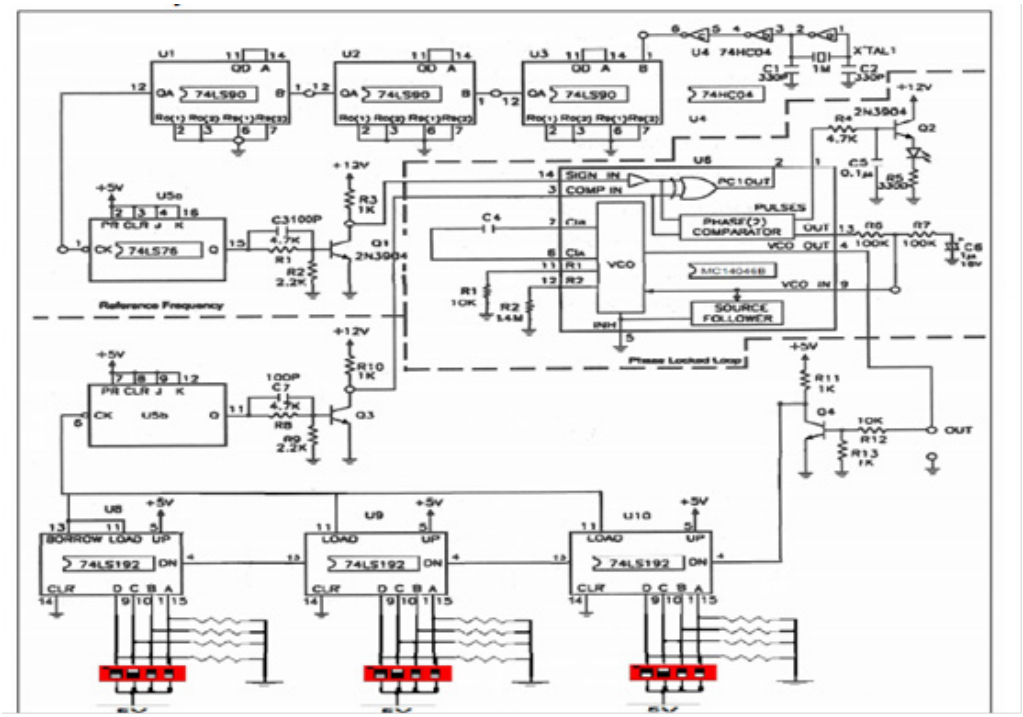

Fig. 3. PLL frequency synthesizer circuit simulated schematic [17]

A) MATLAB Simulated Model

When the frequency is changed at BY-N section, a sudden disturbance in the output signal at VCO output will occur. In [18], N division ratio was changed from (200-300) and from (700-800). The same frequency step of 100k Hz was used. Different values of frequency step, and different results will be reached in this paper because different values of N are proposed.

In MATLAB, this method implements a system whose behavior is defined as:

$$\begin{aligned} x^{\bullet} &= Ax + Bu \\ y &= Cx + Du \end{aligned} \tag{9}$$

where $\dot{x}$ is the input vector derivative; x is the state vector; u is the input vector; and y is the output vector. **A** is n-by-n matrix, where n is the number of states. **B** is n-by-m matrix, where m is the inputs number. **C** is r-by-n matrix, where r is the outputs number. **D** is r-by-m matrix. State-Space is implemented on PLL- FS system whose transfer function H(s) in (6) will be as follows:

$$\mathrm{H(s)}=\frac{\text{output}}{\text{input}}=\frac{y}{u}=\frac{as+1}{bs^2+cs+d} \tag{10}$$

where

$$\mathrm{a}=\left(\frac{2\xi}{\omega_n}-\frac{N}{K}\right),\ \mathrm{b}=\left(\frac{1}{\omega_n{}^2}\right),\ \mathrm{c}=\left(\frac{2\xi}{\omega_n}\right),\ \mathrm{d}=1$$

The State-Space is implemented using 1 kHz input frequency.

To ensure that PLL operates in a linear region, and consequently to ensure that it is approximately in lock range, the linear region of VCO operation is adjusted. This can be made by applying DC voltage sources at VDD input Pin16 of PLL part as in Fig. 3, and disconnecting any other input signals. By measuring the output frequency with respect to

input voltage (VDD), the linear region is shown in Fig. 4. Also, VCO gain (K_{VCO}) is calculated [17] as follows:

$$K_{VCO} = \frac{(F_{max} - F_{min})}{(V_{max} - V_{min})} \quad (11)$$

$$= 8.57 \text{ kHz/V}$$

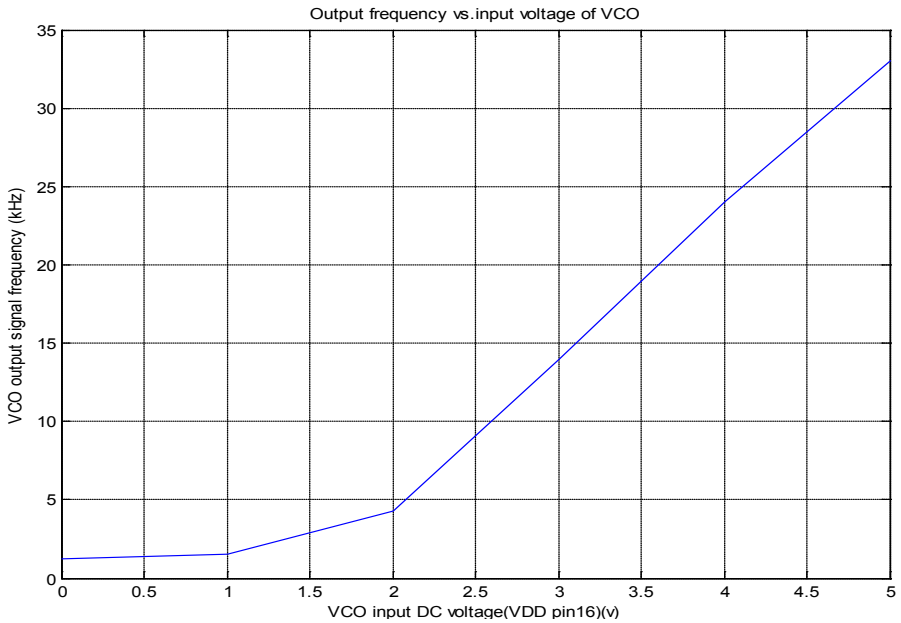

Fig. 4. Output frequency vs input voltage characteristic of VCO

B) ORCAD Simulation Model

Fig. 5 shows the proposed model of PLL-FS in order to achieve lock as quick as possible. Multiple values of resistors and capacitors are connected in a PLL-FS circuit. Also, 74LS192 BCD counterpart is replaced by 7490A part; this IC can provide multiple division ratios. It is connected in a manner to obtain By-2 frequency division. Two frequency dividers are connected to give By-4 frequency division. Fig. 5 shows that the VCO output frequency is divided using 7490A IC part in order to change the frequency between 1-4 kHz.

Single CD4046B IC is used in a PLL simulation model. This part represents the heart of PLL-FS. Practically, CD4046B phase-locked loop IC is a low-power-consumption device which can be used in multiple applications.

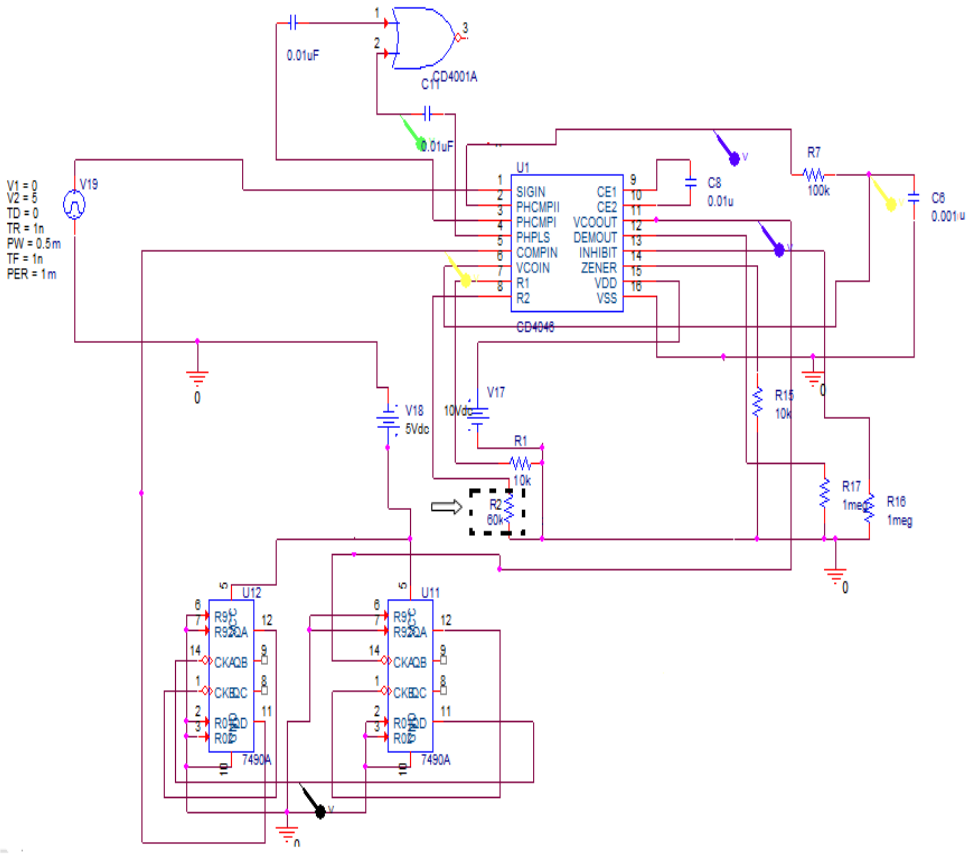

Fig. 5. PLL-FS simulation model in ORCAD

According to CD4046B IC data sheet, PLL-FS mainly consists of VCO and two phase comparators. It has two inputs at PD, one for input signal at pin1 (SIGN) and the other for feedback signal at pin 5(COMPIN). Comparator II output at pin2 (PCOMPII) enters into the loop filter at R7, C6. Output signal (VCOOUT) at pin 11 enters into frequency divider (7490A) stages.

To ensure that CD4046B operates in a linear region, the same steps implemented in part A of this section are applied. Fig. 6 represents the appropriate output for each PLL stage; and it shows when it will be in lock range. PD compares two inputs. The output of the comparison is shown in Fig. 6 at COMPI (pin3), where Comparator I acts as an exclusive OR device. COMPII output (Pin2), and PHPLS (pin 4) are used to test the lock-in-time. When PLL is in lock range, Phase Pulse (PHPLS) output should indicate a high level except for a very short interval pulse. COMPII output should be low except for a very short interval pulse.

From CD4046B data sheet, phase comparator II consists of a digital memory network. This comparator acts only on the positive edges of the input signals. Therefore, its output in Fig. 6 is expected to be in lock range.

Through running a new simulation, and by selecting transient state analysis, it is expected to see some ripple and settling time at the comparator output since a sudden change in frequency occurs, while PLL tries to acquire lock-in time.

By running the ORCAD simulated model of Fig. 5 circuit, two issues should be tested:

- Fast lock and long lock time
- Small settling time before returning to a steady state as quick as possible.

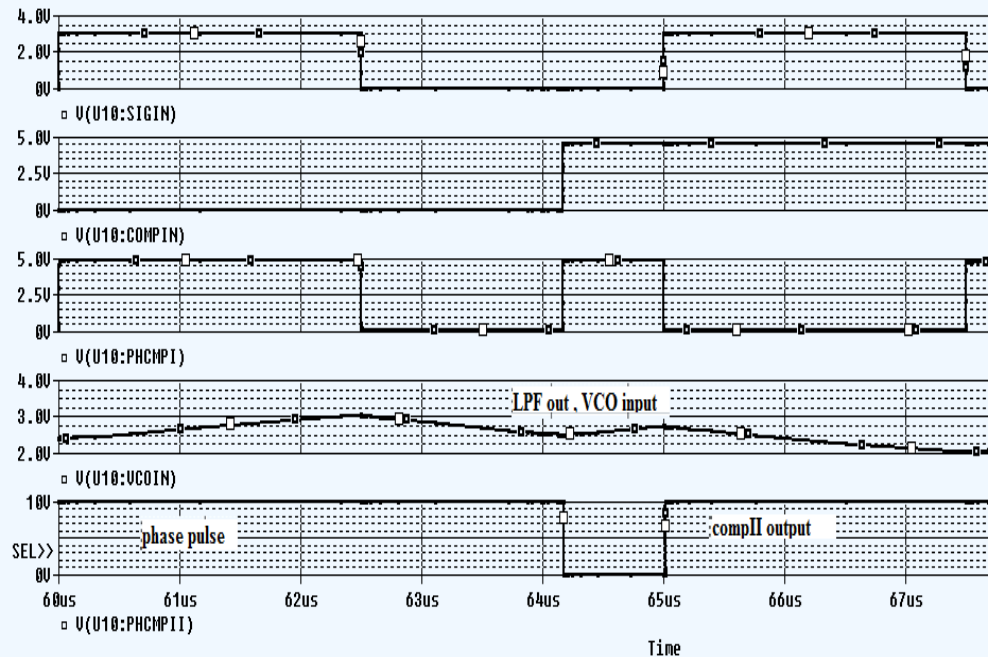

Fig. 6. Output signals from each stage in PLL- FS at lock range

The objective of this study is to speed up the lock time efficiently, improve the settling time and obtain fast lock by changing R2 value in Fig. 5. R2 is connected to pin8 of CD4046B as marked in the dashed area in Fig. 5. According to PLL data sheet, R2 is used to set the offset frequency and the offset phase. In general, offset frequency is defined as the difference between the source frequency and the reference frequency. If there is any difference between the two frequencies, a significant distortion can be created [20]. Consequently, a significant effect on lock time, lock speed, and settling time is made. In the proposed model, R2 helps decrease the time offset. R2 and C8 (between pins 9 and 10) enable VCO to adjust frequency offset, i.e. they determine F_{min}. This will influence the VCO gain, linearity, stability, lock speed, and settling time.

In addition, R1 and C8 that are connected to pin7 are used to determine the range of frequencies in PLL.

Also, it is found that adding an external resistor to VCO output will give a significant improvement in settling time. The next section will analyze and discuss the proposed model results.

IV. SIMULATION RESULTS

The implementation of this study was made using MATLAB and ORCAD simulators. The following sub sections clarify the simulation results. At the end of this section, a comparison between the results obtained in each approach is made.

A) MATLAB Simulation Results

Fig. 7 shows the simulation results, where the frequency division ratio (N) is changed by N=20-40 (for frequency step=20 kHz), and N=200-300 (for 100 kHz frequency step).

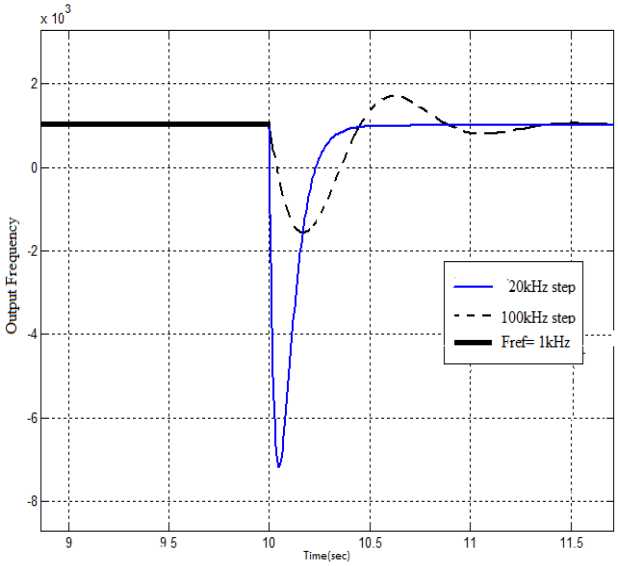

Fig. 7. Output frequency for FS-PLL for 20kHz and 100kHz frequency steps

From the figure above, if a large frequency step is used, the settling time will increase; and using a small frequency step will decrease the settling time, i.e. changing frequency step from 100 kHz to 20 kHz. A great improvement by 80% in settling time is achieved.

B) ORCAD Simulation Results

The following section will discuss the settling time reduction, and speeding up the lock time while keeping the lock as much as possible.

B.1. Lock time and fast lock

As it is illustrated in Fig. 5, the phase pulse output (PHSPLS, pin4) indicates a high level in lock time. So, lock time and fast lock are tested at PHSPLS output. Fig. 8 demonstrates the influence of changing R2 on fast lock and lock time. When R2=40 KΩ, the circuit acquires lock after 46.5 us (46.5 µs), i.e. short time. By zooming-in the peak area, where the arrow is pointing, ripple and settling time change from a low to high level.

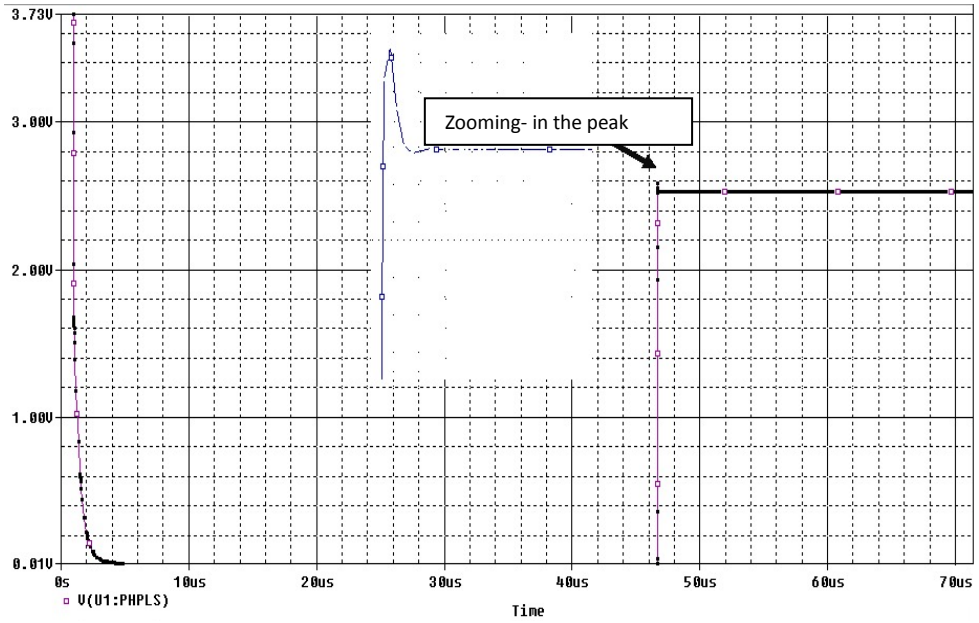

Fig. 8. V(U10 PHSPLS) to test fast lock and lock time

Additionally, Fig. 9 shows VCO out signal, PHPLS, and PHCMPII signals when another value of R2 is taken, i.e R2=50 kΩ. It is obvious that there are short intervals before lock; the system enters lock range after 68μsec to achieve a long lock time range.

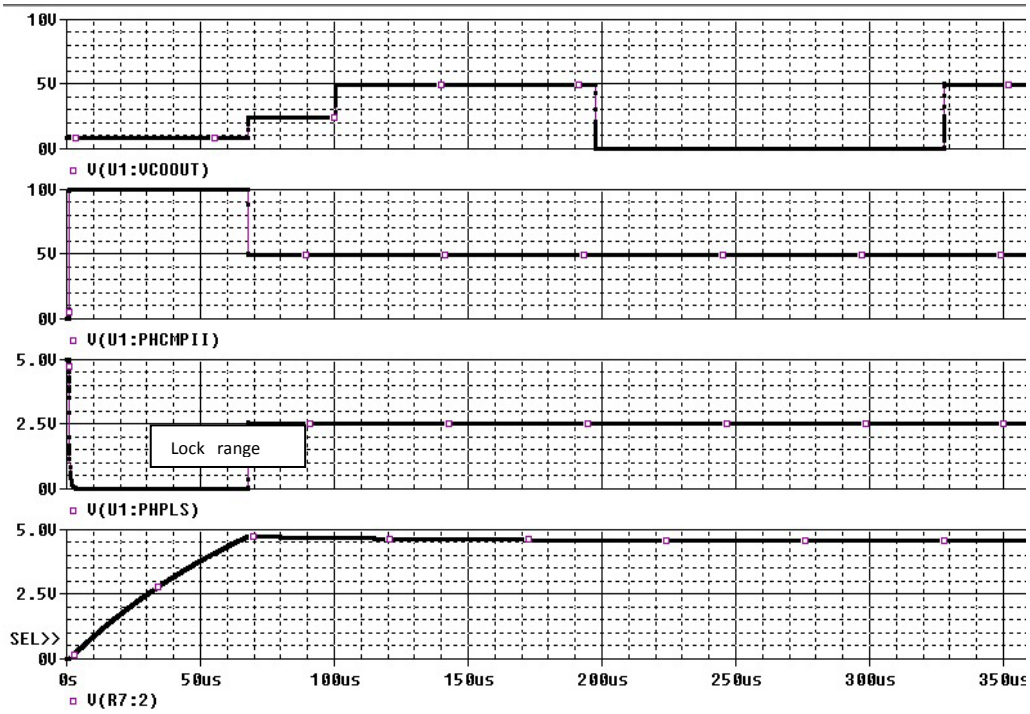

Fig. 9. V(U10(CD4046B)) outputs of several stages at R2=50kΩ

Table 1 represents PHPLS output results for different values of R2.

TABLE 1
LOCK TIME AND SPEED OF LOCK FOR DIFFERENT VALUES OF R2

Value of R2, kΩ	Result of a Sudden Change in Frequency		
	Acquiring Lock after__μsec	Lock Time	Settling Time
20	0	80nsec	0
40	46.5	Long	5nsec
50	68	Long	5nsec
60	70	Long	2.4nsec

As seen in Table 1, when R2=20 kΩ, the system will be locked quickly. This range of lock is missed after a very short time. The lock is only for 80nsec. On the other hand, increasing R2 will decrease the lock speed. When R2= 60 kΩ, the model gives the least speed of lock; and a very short settling time=2.4 nsec is achieved.

B.2. Settling time improvement:

When the lock condition is satisfied, besides settling time, there are some ripples at VCO output signal amplitude (see Fig. 10). Such ripple arises from the circuit parameters, loop gain, and a small difference in phases between input signals.

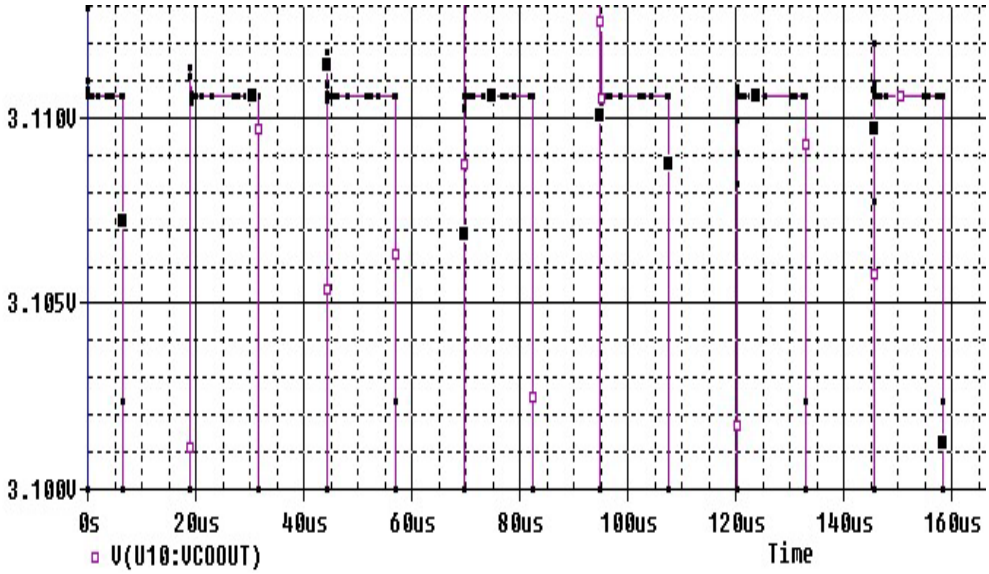

Fig. 10. VCO output with ripple at peaks values

By zooming-in one peak of the above cycles in Fig. 10, an additional improvement in settling time=16 nsec is made as illustrated in Fig. 11. This improvement is achieved due to using an external resistor (Re) in the proposed model between pin 11 and ground.

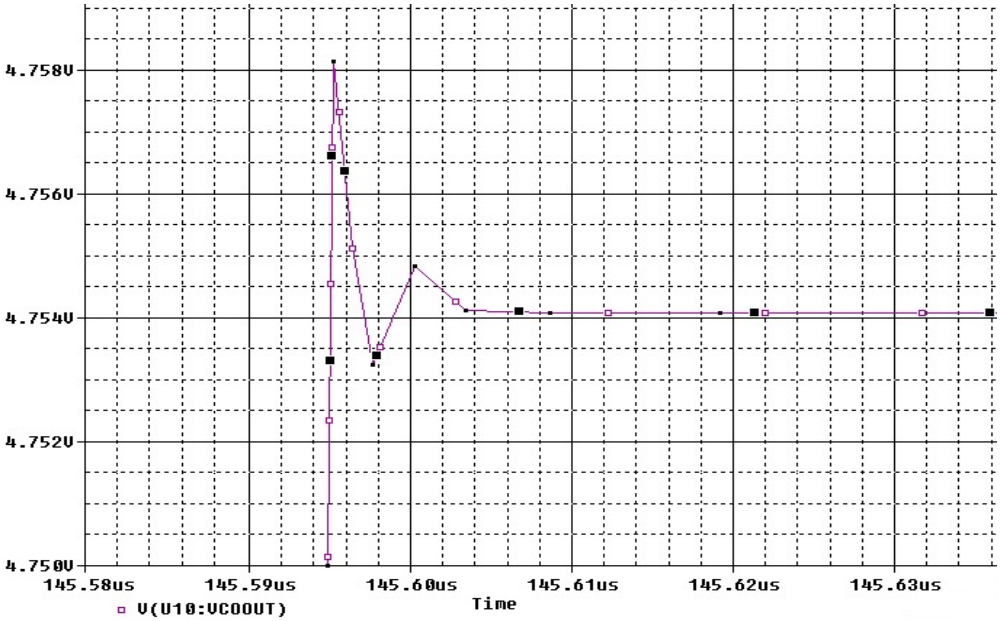

Fig. 11. VCO output with ripple at one peak of output signal

This resistor will improve the settling time either through a sudden change in frequency, or through standing the VCO oscillation.

Fig. 12 shows the VCO output for frequency step=4 kHz after adding the improvement element i.e. (Re). Using multiple values of Re=(30, 100, 1 k)Ω will give the same settling time i.e. (Ts=1.3 nsec).

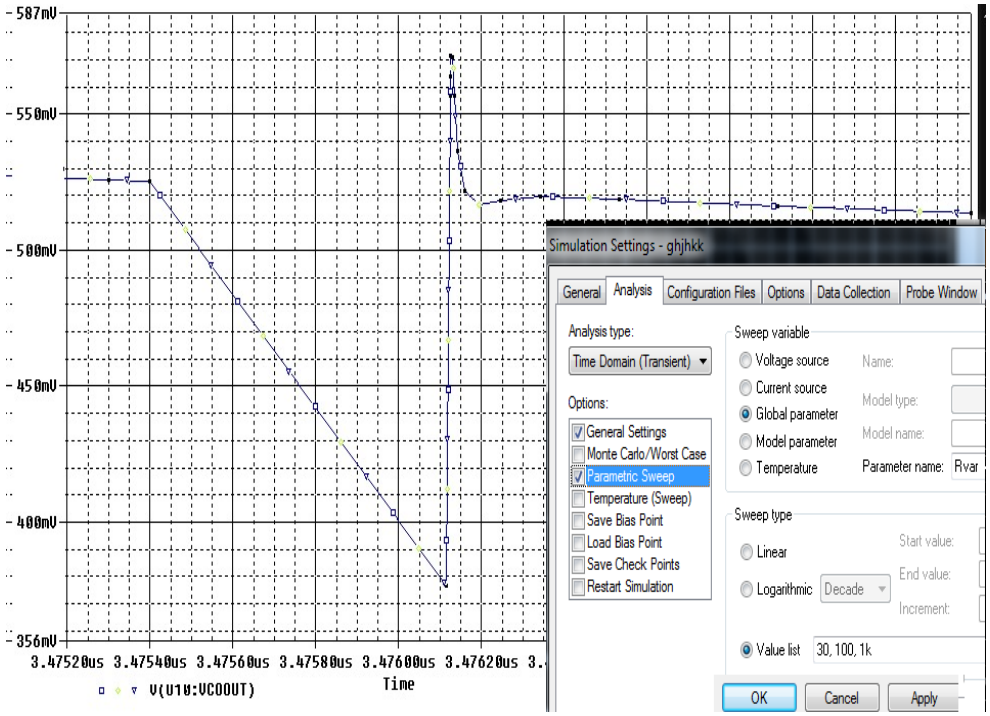

Fig. 12. Parametric sweep transient simulation with different values of Re

C) Comparison between MATLAB and ORCAD Results:

According to the previous results, MATLAB takes different frequency steps. Changing frequency steps leads to a change in PLL transfer function parameter, which consequently influences the settling time. As a result, using a small frequency step can decrease the settling time, while a large frequency step gives long settling time before a steady state.

On the other hand, changing frequency steps in ORCAD is more difficult since BY-N IC's in each change of frequency step needs to be added.

ORCAD is used to simulate the complete system, where the electrical behaviour is demonstrated clearly. This is evident through changing circuit elements values such as resistors values in the proposed model. These changes do not only influence the settling time, but they also acquire long lock time and speed up the lock range. While in MATLAB, these features cannot be obtained easily.

In conclusion, ORCAD gives more complete and accurate results of the proposed model than MATLAB.

V. CONCLUSIONS

This work proposed PLL-FS model to acquire very short settling time and speed up the lock time with long lock thereafter. Settling time is decreased by 80% when frequency steps are changed. Small frequency steps shorten settling time.

Additionally, the proposed approach improves on settling time by changing R2 value. Selecting R2=40 kΩ gives significant results, where settling time=5 nsec is achieved with the best lock speed.

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