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A High-Gain Low Noise Amplifier for RFID Front-Ends Reader

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Abstract— A high gain CMOS Low Noise Amplifier (LNA) for 866 MHz RFID reader has been proposed and simulated in 0.18 µm CMOS technology. A new energy efficient technique along with the current bleeding PMOS devices has been used to reduce the leakage power of the RF signal and increase the gain of the proposed LNA design. Furthermore, the folded cascode with a combination of the partial source degeneration (PSD) is improved; and the current and boosting inductor are reused to enhance the gain and linearity of the proposed design. The simulation results show that the proposed LNA design outperforms the conventional fold cascode LNA in terms of gain (S21) and Noise Figure (NF). The proposed LNA achieves a forward gain of 24.8 dB with a NF of 0.38 dB with 10.6mW drawn from a 1.2V source supply; and a high linearity Input Third-Order Intercept Point (IIP3) of -3dBm.

Keywords— 0.18µm CMOS technology, Boosting inductors, Gain, Linearity, Partial source degeneration PSD, Radio frequency identification RFID.

I. INTRODUCTION

With the recent advances in global standardization, Radio Frequency Identification (RFID) technology has risen to prominence over the last decade. RFID has become an important tool for supply chain management and Mobile RFID applications. The clear advantage of this technology over conventional ones, along with mandates from supply chain such as Wal-Mart to the Military Defense, led it to be a hot spot area [1]-[3].

Generally, RFID relies on unlicensed bands for such communications as Industrial, Scientific and Medical (ISM) bands. The use of UHF band (860-960MHz or 2.4GHz) has been growing and efficiently reaching longer distance and lower cost tags. As the application is expanded, customers' demand requires RFID readers that are cheap, and has a small size and light weight, as well as long battery life; the front-end transceiver is becoming more and more important in RFID system. Specifically, customers intend to have low cost, low-voltage and small-scaled personal wireless communication equipment. These requirements can be met by utilizing a CMOS technology to integrate the RF frontend functions on a single die [1]. In terms of practical implementation, a single-chip reader is feasible for UHF RFID since the higher operating frequency results in a smaller size of antennas and passive components [2], [4]. The common challenge in the RFID transceiver is needed to handle a large transmitter leakage during tag reception. Thus, the receiver front-end implementation requires a high compression point and low noise.

In terms of RFID LNA design, low power dissipation is a handheld RFID criterion operating at the standard frequency band. Therefore, in this paper, linear, low power LNA is designed to provide a great trade-off between power consumption, noise, linearity and sensitivity for achieving optimal performance [5]-[10]. The first active device to amplify the signal in the RF front-end is the LNA which significantly influences noise performance in the receiver. Because the first stage in the cascaded system has dominated input-referred noise, LNA has a major impact on the front-end receiver as well. The vital block of the RF front-end receiver is

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the low noise amplifier (LNA) which plays a critical role in determining the noise figure of the system.

Fig. 1 shows a front-end block of a typical RFID Reader. Recently, several LNA designs based on the micron CMOS technologies have been presented [7]-[20]. In literature, there are various topologies of LNAs for different applications, such as narrow band, multiple bands and wide-band LNAs [2], [14], [15], [20], [21]. The proposed common gate (CG) LNA in [20] has good linearity and good I/O isolation property, but the parasitic components of the transistor result in higher NF and higher power consumption. Moreover, some other LNA designs employ input matching network and extra noise figure cancellation techniques [10]-[15].

For the narrow band LNA design [15], [22], a cascode common-source with inductive degeneration has been used to perform isolation between ports and match the LNA input to the preceding antenna. However, the inductive degeneration of LNA has the shunt-input resistor that degrades NF of the LNA.

This paper discusses the complete design and optimization of a low-power 866 MHz CMOS Common Gate cascode LNA using an enhanced power source degeneration PSD technique based on energy metric. Unlike most other optimization techniques in the literature, the energy metric of the CMOS transistor is included in this design, which results in additional performance improvements. This energy metric [8] defines the critical width which can be used to get a higher gain with lower power consumption. Also, the proposed LNA has lower power consumption and uses a modified version of the current reused and current bleeding topologies. Moreover, the new Partial Source Degeneration (PSD) technique of a folded cascode amplifier is adopted to share the operating current and enhance the performance and gain of the amplifier at 866MHz.

The organization of this paper is described as follows. Section 2 briefly discusses design parameters. Section 3 presents energy efficient metric for RF tuned circuit. In section 4, the theoretical analysis and schematic design of the proposed LNA are discussed and presented. Simulation results for the proposed LNA are proposed in section 5. Finally, the conclusion is summarized in section 6.

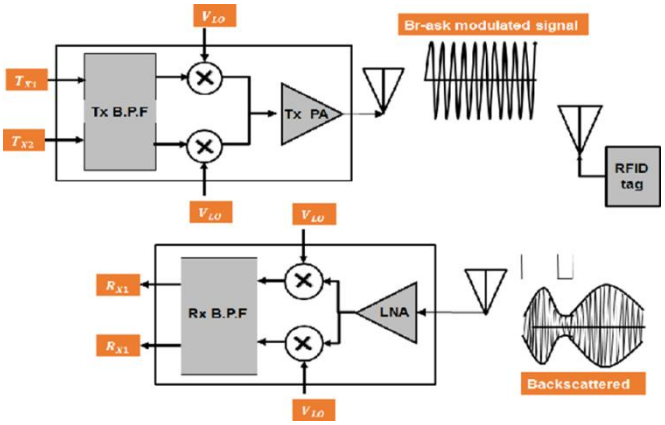

Fig. 1. The front-end block of a typical RFID reader

II. DESIGN PARAMETERS

A. Scattering Parameters

In this subsection, the two-port network and *S*-parameter are briefly discussed. There are several methods to characterize the behavior of a two-port network. In radio frequency range,

scattering parameters (*S*-Parameters) are usually used. It is based on incident and reflected waves as shown in Fig. 2. Fig. 2 describes a two-port network, where x_1 and x_2 are incident waves and y_1 and y_2 are reflected waves. One can express their relation as follows:

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = [S] \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \quad (1)$$

where matrix $[S]$ represents the scattering matrix; S_{11} is the input reflection coefficient; S_{12} is the reverse transmission coefficient; S_{21} is the forward transmission coefficient; and S_{22} is the output reflection coefficient. One can obtain these parameters according to the following equations:

$$S_{11} = \frac{y_1}{x_1}\Big|_{x_2=0} \quad (2)$$

$$S_{12} = \frac{y_1}{x_2}\Big|_{x_1=0} \quad (3)$$

$$S_{21} = \frac{y_2}{x_1}\Big|_{x_2=0} \quad (4)$$

$$S_{22} = \frac{y_2}{x_2}\Big|_{x_1=0} \quad (5)$$

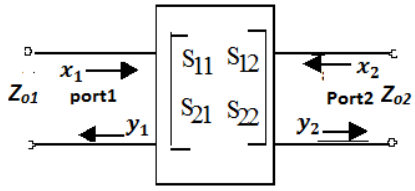

Fig. 2. *S* parameter of two-port network

From the view point of LNA design, S_{11} and S_{22} represent how well the input and output impedances are matched to the reference impedance. S_{21} represents the amplification gain of the amplifier while S_{12} represents isolation between output and input ports.

B. The Third Order Intercept Point

In the RF system, we commonly use the third order intercept point to measure the non-linearity behavior of the system. In this paper, we obtained the third order intercept point by a "two-tone" test [2].

Let us consider two signals with different frequencies are applied to a non-linear system as shown in Fig. 3. The output shows some components that are not harmonics of the input frequencies. This phenomenon, called intermodulation (IM), arises from mixing two signals. The IIP3 has been determined to characterize the corruption of signals due to third-order intermodulation of two nearby interferers. It is measured by a two-tone test, where A_1=A_2=A. The input signal level, where the power of the third-order IM product equals to that of the fundamental, is defined as an input-referred third-order intercept point (IIP3) [2].

In order to measure the third order intermodulation point (IP3), we apply two sinusoidal tones of identical amplitude to the input of the LNA with different frequencies, ω_1 and ω_2. The output of the LNA circuit will have intermodulation components, not harmonics with the introduced frequencies. At the output, the powers of the introduced tones, ω_1 and ω_2, as well

as the ones of the third order intermodulation products, $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$, will be measured as the closest ones to the bandwidth used by the LNA. The third order products as well as the rest of the signals, excluding the tones which are in the ω_1 and ω_2 frequencies, form the distortion of the circuit and appear as a consequence of the non-linear behavior of the LNA. The IIP3 represents the input power, where the output power of the main tone and the intermodulation product, are the same.

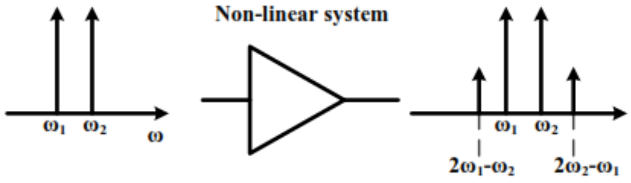

Fig. 3. Intermodulation in a nonlinear system

III. ENERGY EFFICIENT METRIC

We use the same metric in [8] to quantify energy efficiency of the gain in our design. The aim of this metric is to identify the width of the transistor which has the lowest power consumption and highest gain. Based on this metric, one can estimate the size of a transistor and the appropriate biased voltage as shown in Fig. 4 and 5 [8], [17]. A fundamental tenet of the metric is that only the total gain and power consumption affect energy efficiency. The general energy-efficiency metric is as follows:

$$Efficiency(E) = f(Gain, Power) = \frac{\log(gain)}{Power} \tag{6}$$

Fig. 4 presents the tuned LC amplifier circuit, which has a resonance frequency at the 866MHz. Fig. 5 presents the corresponding energy efficiency using the metric in (1) for the tuned LC amplifier circuit in Fig. 4. We see that at the 866MHz in the 0.18µm CMOS process, the maximum energy efficiency of an amplifier happened at a specific size to show a maximum gain with lower power consumption. This result helps us choose the specific width at an appropriate bias voltage to have the maximum efficiency of the LNA.

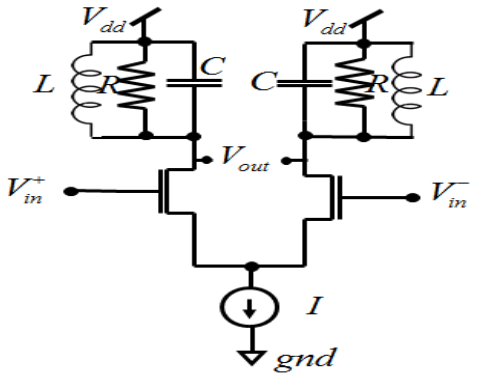

Fig. 4. Tuned LC amplifier circuit

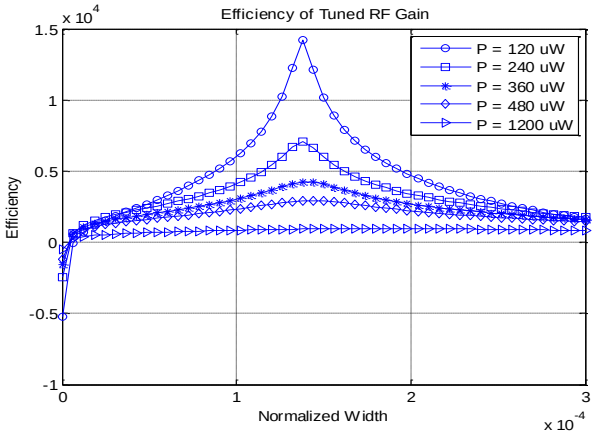

Fig. 5. Efficiency of tuned RF gain versus input transistor width

IV. LOW NOISE AMPLIFIER (LNA) DESIGN

In the LNA circuit design, the gain and the NF are the main factors to consider. However, system linearity is the crucial issue, which influences the performance and stability of the system. Additionally, these parameters have to be considered simultaneously since they are related to other parameters in communication such as the relationship between power supply and the gain of LNA or nonlinearity.

The most important parameter in the LNA design and RF integrated circuit is the thermal noise when operating at high frequencies; the thermal noise is more influential than the flicker noise. As we know, most of the thermal noise comes up from resistance. To that end, we have to trade-off among these two parameters. The main challenge in the front-end receiver lies in maintaining high gain, NF, and linearity at a minimum power consumption with a lower supply voltage. We start our design by defining the length of the transistor to the minimum technology and using the metric in [8] to find the best width, as in the previous section. Once we determine the total width, the inductors are chosen to better fit the impedance matching. We can present the partial source degeneration technique by using two parallel transistors in a common source configuration as shown in Fig. 6.

Fig. 6 shows the proposed LNA design using a current reuse to achieve minimum power consumption, current bleeding, partial source degenerating and boosting inductors topologies. M_{N1} and M_{N2} transistors are both common source configurations. M_{N1} and M_{N2} cascade common source amplifiers which use the same supply current to reduce dc M_{N2}transistors, produce high gain and improve input output reverse isolation with cascaded M_{N3}transistor.

To that end, we deploy the L_b mutual coupled degenerated resonant tank to enhance the choke isolation. Furthermore, we used partial source degenerated method to advance the input match with a partial degenerated source M_{N2}, boost linearity and raise high reverse isolation [4], [8]. The transistors M_{P5}, M_{N6} and M_{N7} form a CMOS voltage divider to provide a bias voltage to the gate of the amplifier. A choke inductor in parallel with a tank capacitor forms a resonant tank to increase the choke isolation.

To mitigate the inductive degeneration effect, we employ C_e capacitor parallel with the gate-source capacitor of the transistor. Furthermore, the folded-cascode structure reduces power consumption and enhances the linearity of the proposed LNA.

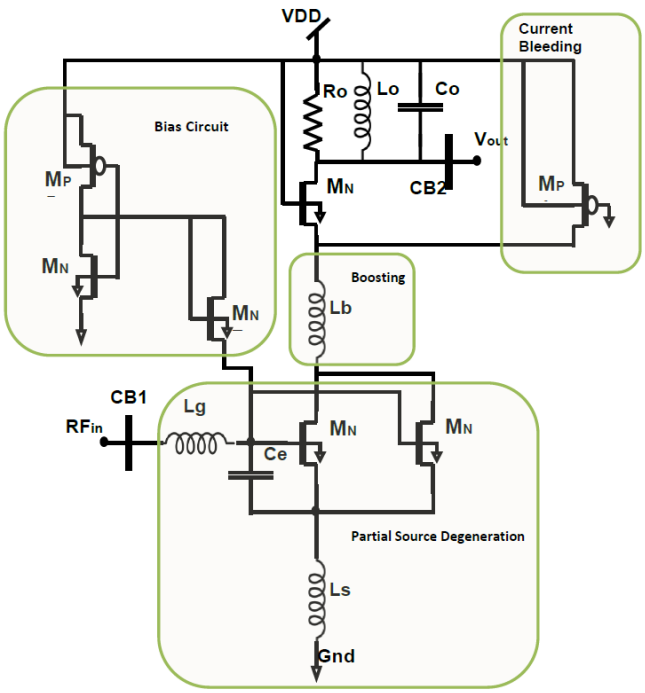

Fig. 6. The proposed 866MHz LNA schematic

One can easily derive the input impedance matching of the proposed design at the resonance as follows:

$$Z_{in} \cong \frac{(g_{m1}+g_{m2})}{(C_e+C_{gs1}+C_{gs2})}\frac{(L_s+L_b)g_{m3}}{(g_{m3}+g_{ds1}+g_{ds2})} \quad (7)$$

where $g_{ds1}(=1/r_{o1})$ and $g_{ds2}(=1/r_{o2})$ are the output conductance of M_{n1} and M_{n2}, respectively; g_{m1}, g_{m2} and g_{m3} are the transconductances of the cascode transistors M_{n1}, M_{n2} and M_{n3}, respectively.

Finally, the PMOS transistor M_{P4} is used as a modification of the current bleeding method to make a fraction of the current to flow through the current bleeding branch and, consequently, reduce the dc current that would have flown through the load resistor. Dimensions of the transistor in Fig. 6 are given in Table 1.

TABLE 1
TRANSISTOR SIZES FOR THE SCHEMATIC IN FIG. 6

Transistor	Width, µm	Length, µm
M_{n1}	100	1.8
M_{n2}	45	1.8
M_{n3}	400	1.8
M_{p4}	150	1.8
M_{p5}	3	1.8
M_{n6}	40	1.8
M_{n7}	40	1.8

V. SIMULATION RESULTS

In this section, we report the simulation results of LNA circuit. The presented LNA circuit is designed by 0.18µm CMOS RF process and simulated by ADS tool. The proposed LNA design described in Section 3 is operated at 866MHz. The circuit is biased at 1.2V supply

voltage. All simulation results are performed with 50 ohms input port and 50 ohms output port. The *S*-Parameters are used to measure the small signal gain. As clearly shown in Fig. 7, the circuit has a gain of 24.8dB at 866MHz.

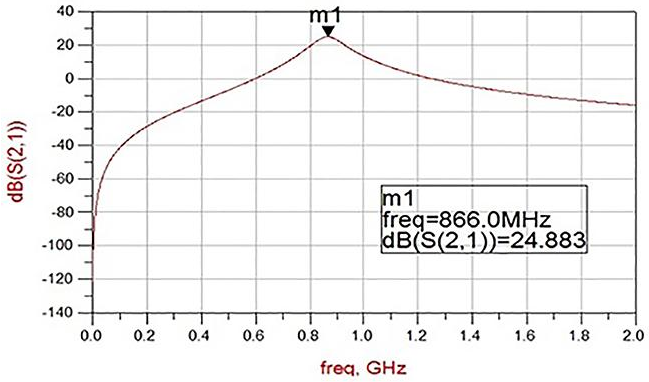

Fig. 7. Forward gain S_{21}

As shown in Fig. 8 and 9, the proposed LNA achieves the input S_{11} and output S_{22} return losses of -6.3dB and -25.5dB, respectively. Moreover, the design consumes 8.83mA from a 1.2V supply source. For any LNA design, it is ideal to keep NF as low as possible. *S*-parameter is used to find the NF as shown in Fig. 10. As clearly shown in Fig. 10, the designed LNA has NF of 0.361dB at 866MHz.

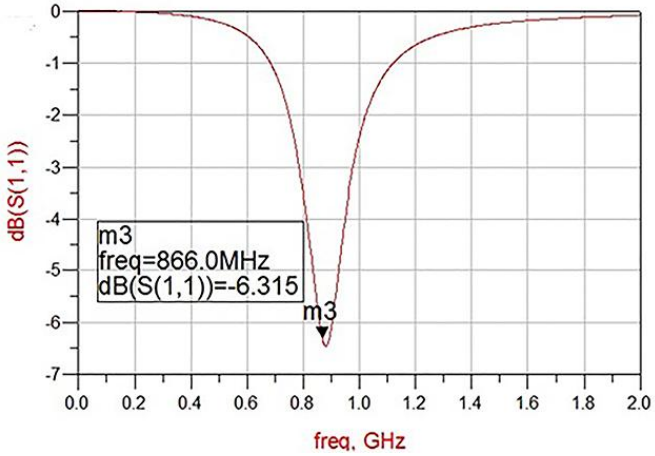

Fig. 8. Input return loss S_{11}

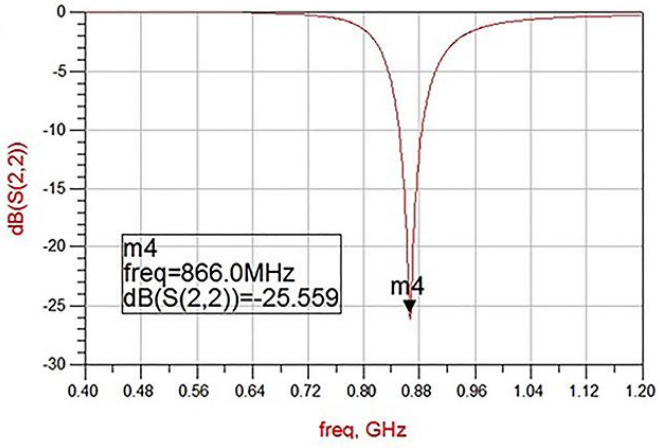

Fig. 9. Output return loss S_{22}

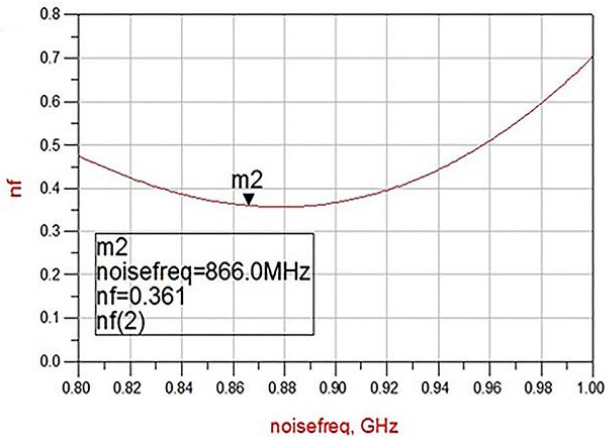

Fig. 10. Noise figure

At that end, the 3-dB compression point indicates the LNA linearity. As shown in Fig. 11, an IIP3 of -3dBm at 866MHz is obtained. The results shown in Fig. 11 are reached by using two tones technique. Table 2 compares the proposed LNA performance with some recently published LNAs indicating the comparative enhancements achieved.

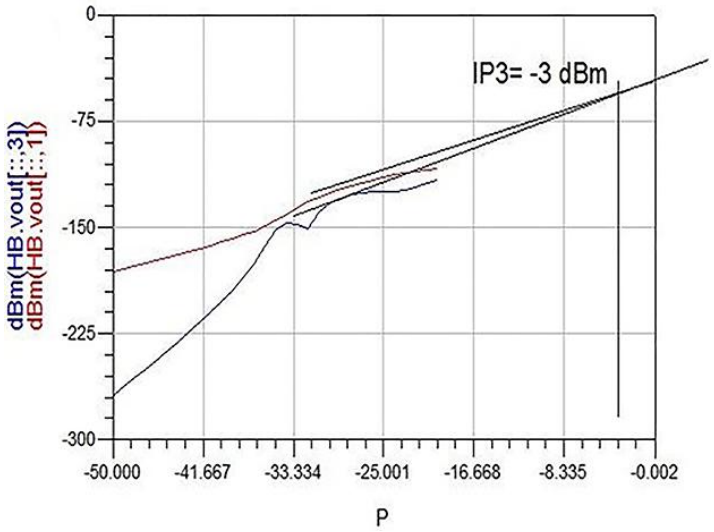

Fig. 11. IIP3 versus input power

TABLE 2
SUMMARY OF THE PROPOSED LNA PERFORMANCE COMPARED WITH RECENTLY PUBLISHED DESIGNS

Specification	Proposed Work	[20]	[19]	[23]	[21]
Technology, µm	0.18	0.13	0.13	0.18	0.13
Frequency, GHz	0.866	0.866	0.866	2.4	2.4
Gain, dB	24.8	17	17	18.5	13
I/O return Loss, dB	-6.3	-19.5	-30	-15	-11
Reverse Isolation, dB	-44.5	-	-34	-	- 42
Noise Figure, dB	0.36	7.5	2.2	4.6	2.2
Supply Voltage, V	1.2	1.2	0.7	1.8	1.5
Power Consumption, mW	10.6	6	0.85	10.8	1.5
IIP3	- 3.21dBm	-4.1dBm	-11.5dBm	-15dBm	1.17dBm

VI. CONCLUSIONS

The vital goal of any LNA is to achieve a high gain with a very low noise. In this paper, we report LNA design obtains a high gain 24dB and 0.34dB low noise factor and improves linearity IIP3. Theoretical analysis and transistor level simulation results using level 0.18µm CMOS process are presented to demonstrate the proposed design. Furthermore, the LNA demonstrates a high stability and a very low noise figure, which shows its suitable and a competitive linearity. An LNA combines a low noise figure, reasonable gain, and stability without oscillation over an entire useful frequency range. The proposed LNA has produced sufficient gain with an improved noise figure; and it is suitable for RFID applications.

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