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A New Reduced Switch Count Three Phase Series Parallel Switched Multilevel Inverter

R. Geetha[a], M. Ramaswamy

Department of Electrical Engineering, Annamalai University, Tamilnadu, India
[a]e-mail: geethaelectrical@yahoo.com

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Abstract— The paper brings out a new three phase cascaded multilevel inverter (CMLI) with a reduced number of power switches over similar other topologies to reach a desired number of levels for the output voltage. It allows following a series parallel path for the flow of current and engages a change in the modulation index to extract a variable output voltage. The operation pronounces the benefits of a new pulse width modulation strategy to leave way for lowering the total harmonic distortion of the output voltage. The phase disposition type of modulation scheme adds substance in shaping the voltage waveform to a nearly sinusoidal pattern in the sense it forays to mitigate the higher frequency components of the output voltage. The modulating mechanism further enables a significant increase in the fundamental component of both the output line and phase voltage. The hardware based investigative study attempts to validate the simulated results and evince the significance of the proposed reduced switch count multilevel inverter (MLI) in terms of the lowering of the capital cost and improvement in the quality of the target voltage.

Keywords— Multilevel inverter, Phase disposition, Pulse width modulation, Total harmonic distortion.

I. INTRODUCTION

A multilevel inverter (MLI) orients at synthesizing a staircase waveform through the help of appropriately connected power switches from multiple input dc levels. The switching action of semiconductor devices plays a crucial role to achieve a multistep waveform with controllable amplitude, frequency and phase [1]-[4]. It inherits an ability to operate at higher voltages, face smaller *dv*/*dt* stresses and offer a possibility of a fault-tolerant operation.

The slew of MLI topologies accrues several advantages in terms of lower total harmonic distortion (THD), electromagnetic interference (EMI) generation and voltage ratings of the power switching devices [5]-[8] .The stepwise output voltage heaves out the need for filters and attaches a capability to operate on low and high switching frequencies.

Although the classical MLI structures that include the flying capacitors (FC) converters, Neutral point clamped (NPC) converters [9] and Cascaded H- bridge (CHB) inverters [10] continue to find wide spread applications, still the device count appears to increase significantly with the increase in the number of voltage levels [11]-[13].

A new topology based on non-insulated dc voltage sources has been proposed for a MLI. It has been derived to involve reducing the number of switching devices and eliminating control complexity for the gate driver circuits [14]. The operation has been verified by using both simulation and experimental prototypes of 15-level model.

A new MLI configuration with reversing voltage component has been drafted to improve performance in terms of the reduced harmonic distortion, lower electromagnetic interference and simpler PWM control technique [15] and the performance of the seven-level prototype tested to illustrate the results.

A novel cascaded transformer reduced switches inverter (CTRSI) has been presented for a MLI with one dc source and seven single phase transformers [16]. The results obtained from

Corresponding author's e-mail: geethaelectrical@yahoo.com

simulation and a low power experimental setup has been shown to offer a higher quality of output voltage.

A new MLI circuit has been suggested for a three phase voltage source inverter to operate with the low switching frequencies. It has been conquered from a conventional three phase full bridge configuration with addition of five bidirectional switches [17]. The simulated results have been verified through a seven-level hardware module controlled through the use of a digital signal processor (DSP).

A single phase cascaded MLI based H-bridge units have been proposed [18] and different algorithms outlined to determine the magnitude of the dc voltage sources. The performance of the topology has been verified using experimental results of the prototype model.

Two optimal topologies with minimum number of switches and dc voltage sources have been brought out to produce maximum number of output voltage levels [19].The simulation results have been compared with those obtained experimental to establish the correctness in the operation of the topologies.

The load side of a hybrid seven-level inverter has been constituted of a high voltage slow switching and low voltage fast switching inverter. A novel hybrid modulation technique has been analyzed to incorporate step synthesize in conjunction with variable pulse width for the consecutive steps [20]. The performance has been evaluated using computer simulation and validated through experimental setup.

Two new topologies consisting of a combination of conventional series and switched capacitor inverter units have been proposed to reduce the number of switches and isolated dc voltage sources for a multilevel inverter [21]. The results have been obtained to prove that the doubling of the input voltage without a transformer.

A new single phase switched capacitor MLI with switched capacitor convertor units as virtual DC link has been suggested to operate with reduced number of power switches, diodes and isolated DC power supplies [22]. The PSCAD/ EMTDC based simulation and experimental results have been presented to show its superior performance over similar conventional topologies.

A novel single phase solution has been described to derive increase inverter voltage levels through the use of nonstandard inverter configuration and impendence source networks. The simulation and experimental verification has been detailed to illustrate the operating principles based on special modulation techniques [23].

A new family of cascaded MLI composed of capacitor based unit with two floating capacitor, one embedded DC voltage sources and three power switches has been developed [24].The hybrid structure has been shown to work under mixed switching frequency and provide high quality of output voltage waveform.

Two multicarrier PWM strategies have been laid down to synthesize waveform and carve out improved harmonic spectrum [25]. The theory has been explained using three phase five-level cascaded inverter with multiple modulating signals and a single carrier. The harmonic analysis has been detailed to bring out the merits and the methodology elucidated through the experimental results.

Besides the issues relating to the increased power rating of semiconductor devices, increased number of power sources, reduced number of redundant states and complex modulation and control schemes invite a need to explore new topological origins for maximizing the number of levels with the available input dc sources.

II. PROBLEM STATEMENT

The attempt endeavors to reduce the switch count for a specified voltage level and spring up a new topology for a three phase MLI to produce a variable output voltage. It forges to attempt the use of a new Multicarrier- 60^o PWM strategy in an effort to lower the THD levels of the output phase voltage. The exercise adjoins the use of a field programmable gate array (FPGA) to realize the formative mechanism and evaluate performance by using simulation and experimental prototypes.

III. THE PROPOSED METHODOLOGY

The primary effort transpires to conceive a new series parallel switched MLI in order to synthesize a sinusoidal voltage from isolated dc sources through the passage of a minimum number of active switches in the path for the current to reach each level. The theory encapsulates a rhetoric sequence to engage the use of semiconductor devices for allowing the current to travel through the specific sections in the inverter.

The topology displayed in Fig. 1a cascades the H-bridge in each phase along with similar arrangements that include dc voltage sources and diodes on each of the arms and a switch in the cross arm on either side to form the basic power module. It necessitates adding structures on both sides to increase the number of levels in the output voltage.

IV. OPERATING MODES

The theory encircles the use of bidirectional switches (S_1 to S_4), (S_7 to S_{10}), (S_{13} to S_{16}) that form the H-bridge inverters and unidirectional switches ($S_{a1}\ldots S_{a(n-1)}$), ($S_{b1}\ldots S_{b(n-1)}$), ($S_{c1}\ldots S_{c(n-1)}$), ($S_{A1}\ldots S_{A(n-1)}$), ($S_{B1}\ldots S_{B(n-1)}$), ($S_{C1}\ldots S_{C(n-1)}$), S_5, S_6, S_{11}, S_{12}, S_{17}, S_{18} and the diodes ($D_{a1}\ldots D_{a(n-1)'}$), ($D_{b1}\ldots D_{b(n-1)'}$), ($D_{c1}\ldots D_{c(n-1)'}$), ($D_{A1}\ldots D_{A(n-1)'}$), ($D_{B1}\ldots D_{B(n-1)'}$), ($D_{C1}\ldots D_{C(n-1)'}$) in the arms on either side to create the flow of the current through the *RL* load. Bidirectional devices serve to prevent the flow of the circulating current around the cell.

Fig. 1b shows the part of the power module belonging to phase- *A* in the nine-level MLI. The connection diagrams seen in Fig. 1c and 1d explain the modes of operation for the nine-level MLI to generate $+4V_{dc}$ and $-4V_{dc}$ for the phase- *A* output. While the path for the current to reach $+4V_{dc}$ encompasses the switches S_{a1}, S_{A1}, S_1, S_3, S_6, the switches S_{a1}, S_{A1}, S_2, S_4, S_5 carry the current to accomplish $-4V_{dc}$. The entries in Table 1 relate to the switches involved in each operating mode for the first phase of the three-phase MLI.

TABLE 1
CONDUCTION SEQUENCE FOR PHASE- *A* NINE-LEVEL OPERATION

Output Voltage Levels	Conduction of Switches							
	S_{a1}	S_{A1}	S_1	S_2	S_3	S_4	S_5	S_6
$+V_{dc}$			√	√				√
$+2V_{dc}$	√		√	√				√
$+3V_{dc}$	√		√		√			√
$+4V_{dc}$	√	√	√		√			√
$0V_{dc}$			√		√		√	
$-V_{dc}$			√	√			√	
$-2V_{dc}$		√	√	√			√	
$-3V_{dc}$	√			√		√	√	
$-4V_{dc}$	√	√		√		√	√	

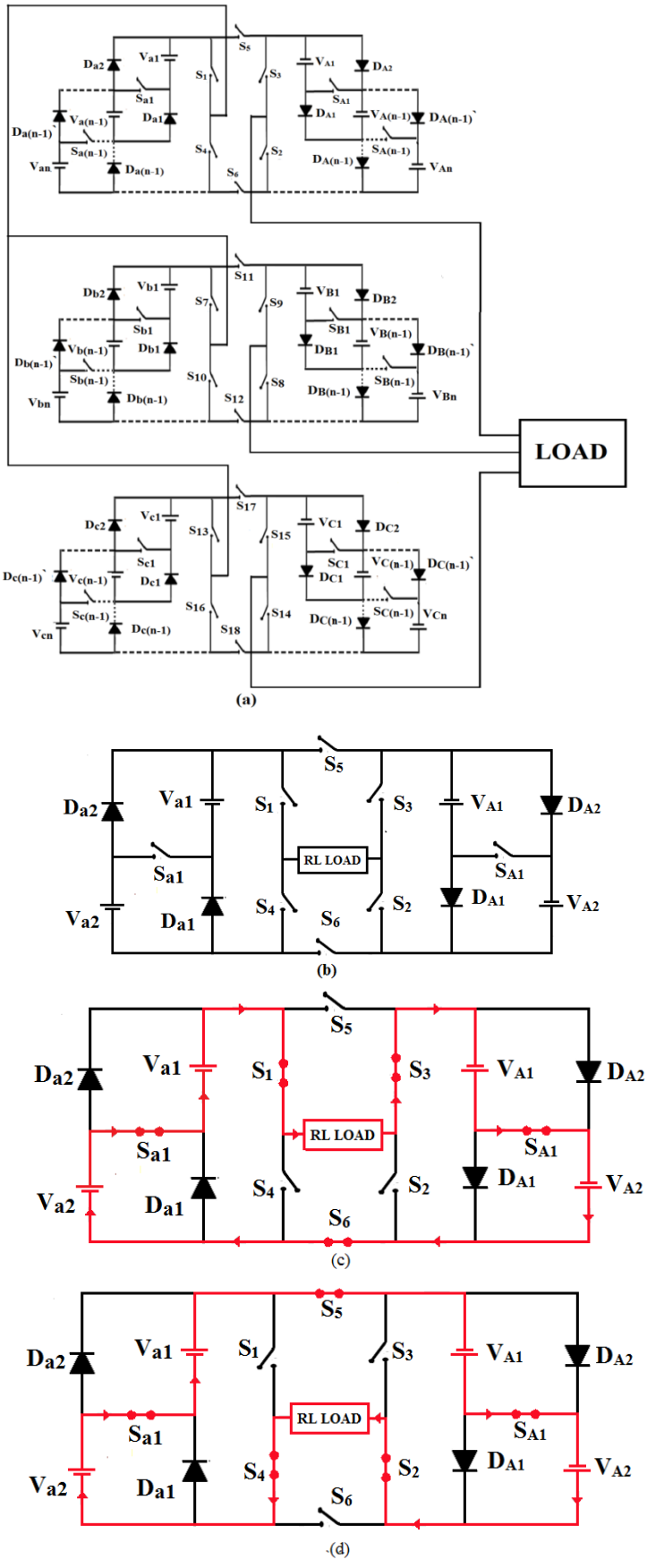

Fig. 1. a) Generalized structure of the proposed three phase CMLI, b) Proposed CMLI topology for phase- *A* nine-level output, c) Mode of operation for $+4V_{dc}$ output, d) Mode of operation for $-4V_{dc}$ output

The entries in Table 2 compare the number of main switches, bypass diodes, clamping diodes, dc split capacitors, clamping capacitors and dc sources among similar other topologies. To reach the nine level output voltage per phase, the new MLI requires eight switches while the cascaded H-bridge multilevel inverter (CHBMLI) with the same number of dc sources needs of 16 switches.

TABLE 2
COMPARISON BETWEEN PROPOSED AND CONVENTIONAL TOPOLOGIES FOR 'M' LEVEL

Multilevel Inverter Topology	Cascaded H-Bridge	Diode Clamped (1981)	Flying Capacitor	Multilevel dc-Link Inverter			Proposed CMLI
				Cascaded half bridge	Diode clamped	Flying capacitor	
Main switches	2(m-1)	2(m-1)	2(m-1)	(m-1)+4	(m-1)+4	(m-1)+4	(m+7)/2
Bypass diodes	-	-	-	-	-	-	-
Clamping diodes	-	2(m-3)	-	-	(m-3)	-	-
DC split capacitors	-	(m-1)/2	(m-1)/2	-	(m-1)/2	(m-1)/2	-
Clamping capacitors	-	-	(2m-6)/2	-	-	(2m-6)/4	-
DC sources	(m-1)/2	1	1	(m-1)/2	1	1	(m-1)/2

Owing to the fact that the proposed topology requires a lower number of switches, it benefits with a smaller number of associated gate drivers and ends up with a relatively lower capital cost. Any increase in the number of switches for increasing the levels of per phase output voltage goes with the expression n+4 and 4n for the proposed CMLI and CHBMLI respectively, where n refers to the number of dc sources.

V. MODULATION STRATEGY

The pulse width modulation schemes spring up to arbitrate on an effective solution for increasing power and reducing the harmonic content in the output voltage of the new CMLI. The multilevel carrier-based PWM offers a higher degree of freedom over the traditional two-level PWM [26]-[29]. It enjoys an option for the switching frequency to be either lower or greater than the carrier frequency and turns out to be a function of the displacement phase angle between the carrier set and the modulation waveform.

The width of the pulses almost remains the same around the peak portion of the sinusoidal reference, and accordingly the attempt incites to inhibit the existence of a carrier signal in that region. The process of modulation features only on either side of the reference signal to realize a change in the modulation index and increase the fundamental component and lower the levels of THD.

The methodology explained in Fig. 2a owes to offer pulses in the first and last 60 degree interval of every half cycle of a full sinusoidal wave; however, it is ascribed to the theory of a sinusoidal pulse width modulation (SPWM) technique.

The operation of MLIs relies on carrier disposition PWM mechanisms, which revolve around the phase disposition (PD) that allows the carriers to remain in phase, alternative phase opposition disposition (APOD) that beholds each carrier to experience a phase shift of 180 degree from its adjacent carrier, and carrier polarity variation (CPV) that varies the polarity to accommodate carriers in a band. The PD modulation scheme acclaims a superior spectral performance compared to the other techniques because it places the significant harmonic energy within the purview of the main carrier [30].

The digital operators seen in Fig. 2b imbibe to identify the intersecting points of the triangular carrier waves superimposed on either side of the sinusoidal reference to extract the PWM pulses for the active switches in tune with the change in the modulation indices to augur a

reduction in the THD. Table 3 displays the location from where the scheme through a combination of logical functions generates the switching pulses to turn on the power devices in phase- *A* and follows a similar approach for the switches in the remaining two phases.

TABLE 3
SWITCHING TABLE FOR THE GENERATION OF PD MULTICARRIER- 60^{O} PWM PULSES FOR PHASE- *A*

Switches	Logical Functions
S_{a1}	B (OR) C (OR) D (OR) D'
S_{A1}	B' (OR) C' (OR) D'
S_1	A (OR) B (OR) C (OR) D (OR) X (OR) A' (OR) B'
S_2	A (OR) B (OR) A' (OR) B' (OR) C' (OR) D'
S_3	C (OR) D (OR) X
S_4	C' (OR) D'
S_5	X (OR) A' (OR) B' (OR) C' (OR) D'
S_6	A (OR) B (OR) C (OR) D

VI. SIMULATION RESULTS

The methodology engages to provide a nearly sinusoidal variable voltage of 415V to support an *RL* load of 150Ω and 100mH, respectively. It evaluates the performance of the proposed new PD based Multicarrier- 60^{o} PWM scheme used for firing the switches in the new three-phase nine-level MLI topology powered from equal magnitudes of dc source in the four arms on a MATLAB/SIMULINK platform.

Fig. 3 and 4 compare the output phase voltage along with phase- *A* THD spectra for a modulation index of 1 obtained using MCPWM, variable frequency carrier band pulse width modulation (VFCBPWM), inverted sine carrier pulse width modulation (ISCPWM) and new Multicarrier- 60^{o} PWM with a carrier frequency of 2 kHz, respectively.

The phase voltage waveform derived from the new modulation strategy showcases the reduction in the switching action around the peak portion to highlight the reason for the increase in the fundamental component and a consequent decline in the THD over a range of modulation indices. Table 4 brings out a variation of the THD values of the target fundamental output voltage for the four PWM schemes to establish the supremacy of the new approach in terms of lower THDs for the same output.

TABLE 4
VARIATION OF THD WITH TARGET FUNDAMENTAL OUTPUT VOLTAGE (PEAK)

Modulation index	Target voltage	%THD of fundamental output voltage (Peak)			
		PD MCPWM	PD VFCBPWM	PD ISCPWM	PD Multicarrier - 60^{o} PWM
1	340	15.61	14.47	14.08	11.03
0.95	320	15.95	15.66	14.69	11.97
0.9	300	16.91	16.32	15.44	12.62
0.85	280	17.53	17.28	16.12	13.16
0.8	260	18.78	18.41	17.39	15.22
0.75	240	19.84	19.28	18.28	16.85

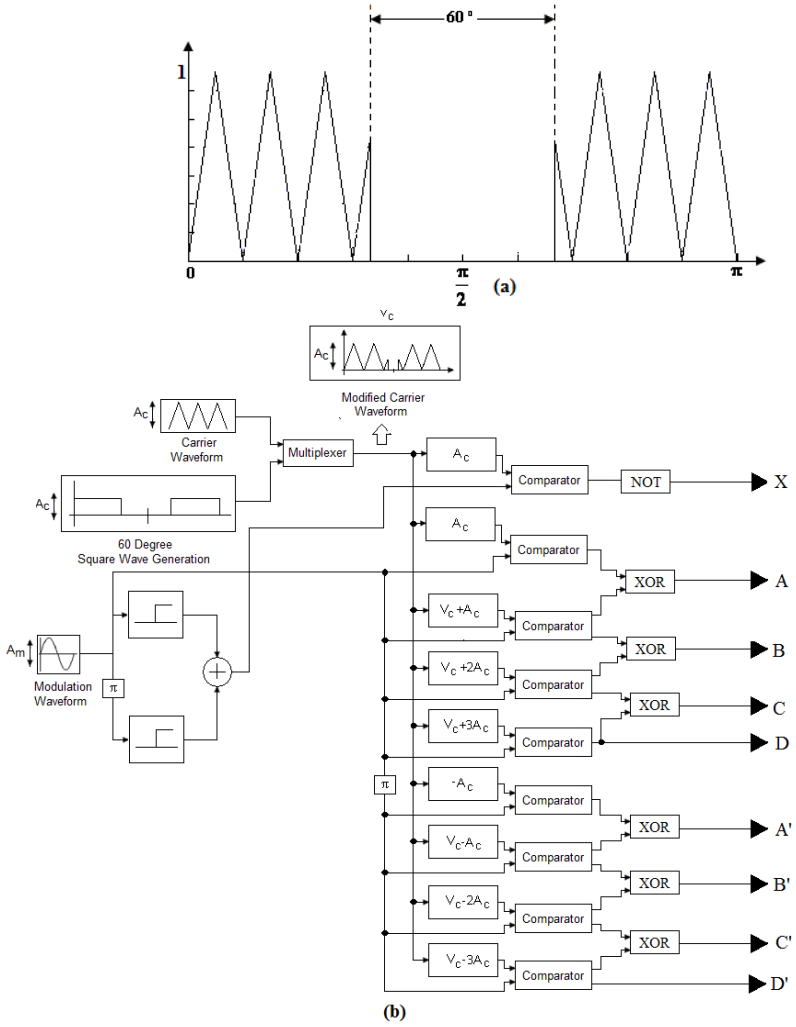

Fig. 2. a) Modified carrier band- 60° PWM, b) Generation of PD multicarrier- 60° PWM pulses for Phase- *A*

VII. HARDWARE IMPLEMENTATION

The Spartan-3A FPGAs form part of the extended Spartan-3A family, which imbibes the non-volatile Spartan-3AN and the higher density Spartan-3A DSP FPGAs. It incites to be a superior alternative to mask the programmed ASICs, enjoy the inherent inflexibility of conventional ASICs and permit field design upgrades with smaller development cycles.

The programmable mode evokes the load of configuration data into robust, reprogrammable static CMOS configuration latches (CCLs) that collectively control the functional elements and routing resources. It employs very fast I/Os and bidirectional data buses and augurs an emphasis to ensure the correct timing of valid data within setup time and hold time. A hardware description language (HDL) serves to specify the configuration of the FPGA; the program enables the realization of any digital function.

The unipolar (IRG4BC20UPBF), bipolar (FIO 50-12BD), insulated gate bipolar transistor (IGBT), bypass diodes (BYQ 28E) and dc voltage sources chosen with exact ratings used for simulation constitute the experimental prototype seen through the photograph in Fig. 5. It embeds a FPGA processor for generating the PWM pulses to examine the performance of the proposed strategy on the new CMLI. The flow diagram in Fig. 6 explains the procedure for

producing the pulses seen in Figs. 7 to 9 through the artifacts of Xilinx Spartan XC3SD1800A-FG676-4 Spartan 3A DSP FPGA board.

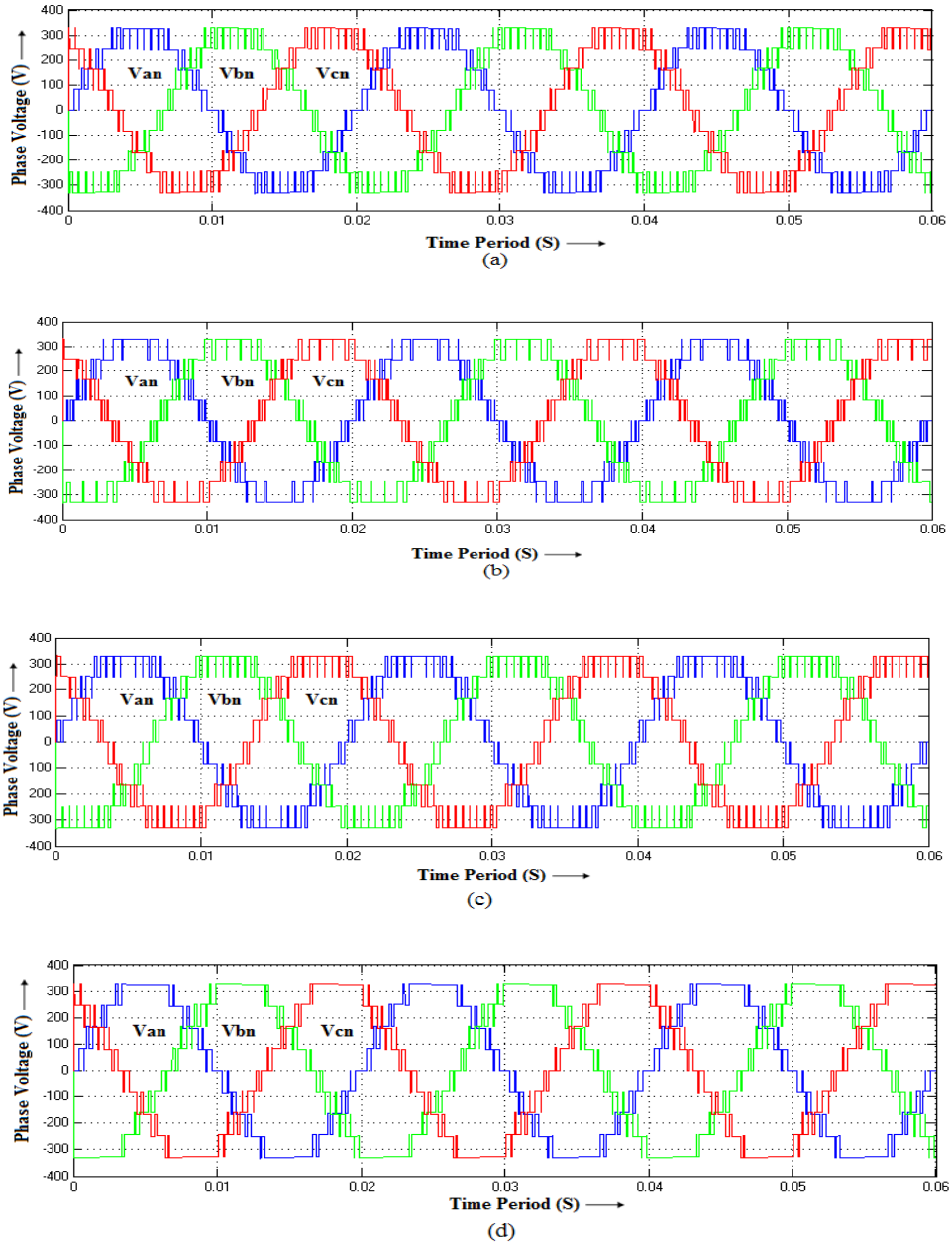

Fig. 3. Phase voltage waveform for: a) PD MCPWM, b) PD VFCBPWM, c) PD ISCPWM, d) PD Multicarrier- 60^{o} PWM

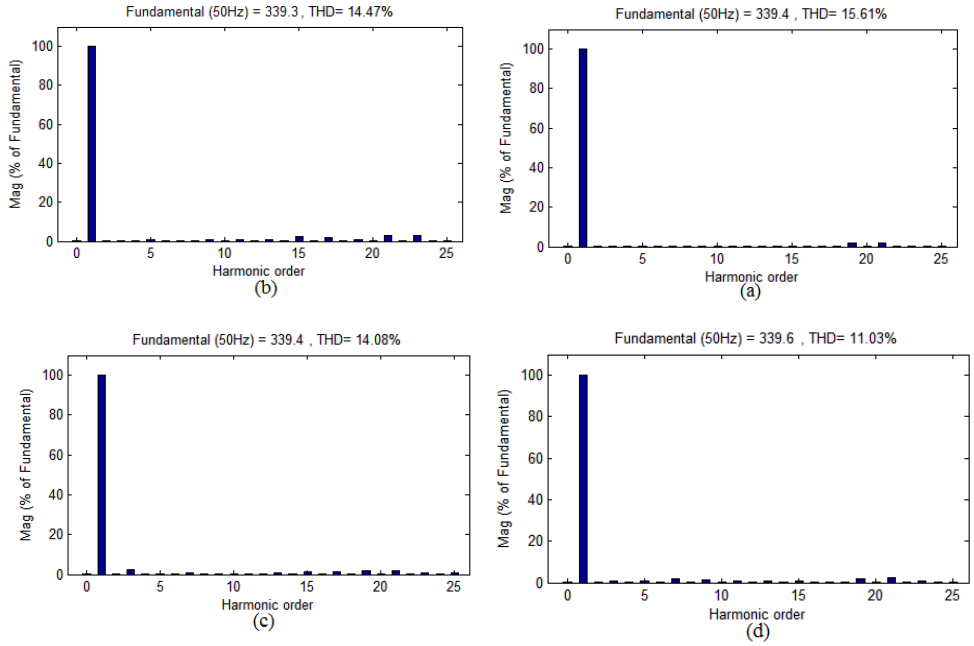

Fig. 4. Phase voltage spectrum V_a for: a) PD MCPWM, b) PD VFCPWM, c) PD ISCPWM, d) PD multicarrier-60° PWM

Fig. 5. Experimental setup

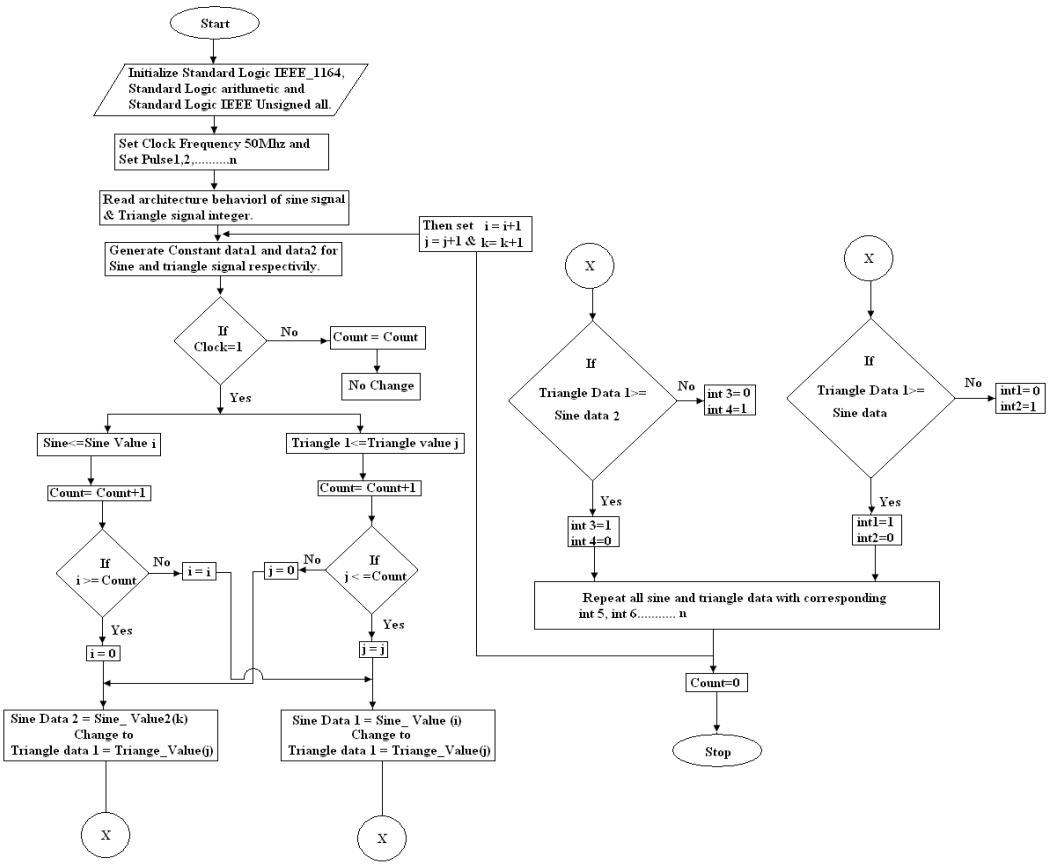

Fig. 6. Flow diagram for the generation of gating pulses using PD multicarrier- 60^{o} PWM

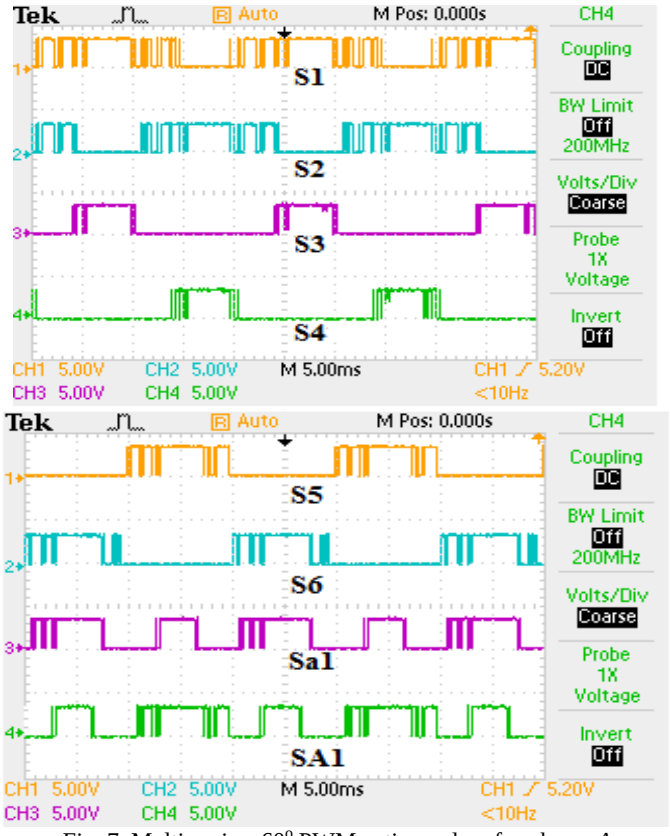

Fig. 7. Multicarrier- 60^{o} PWM gating pulses for phase- *A*

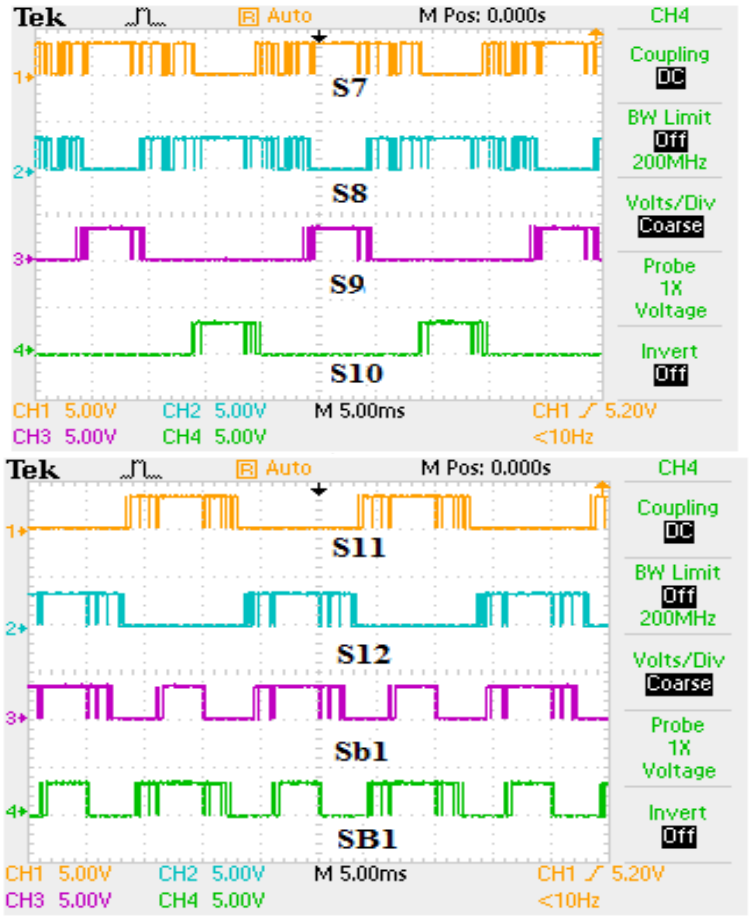

Fig. 8. PD multicarrier- 60^{o} PWM gating pulses for phase- *B*

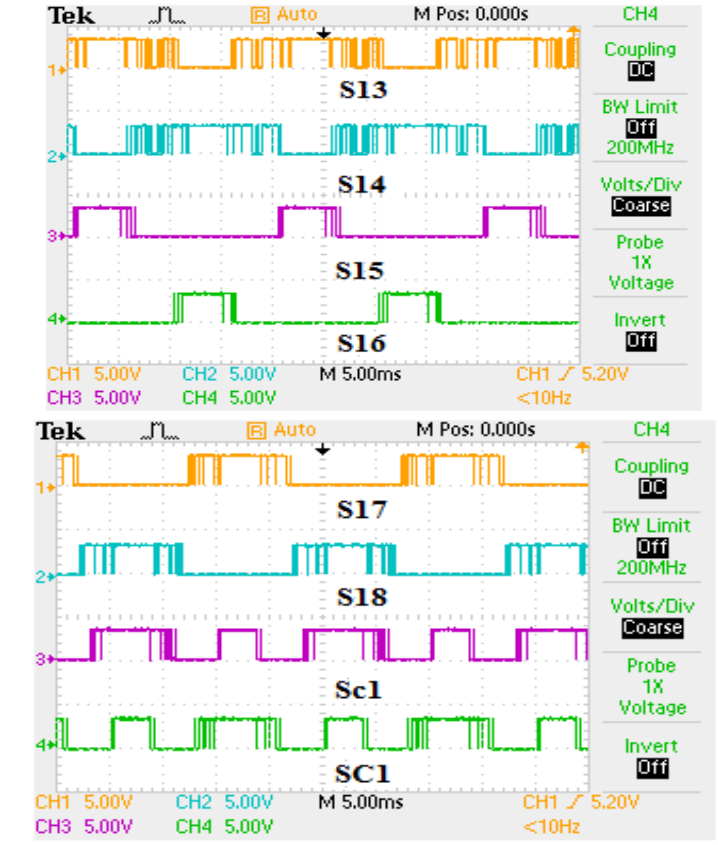

Fig. 9. PD multicarrier- 60^{o} PWM gating pulses for phase- *C*

The Figs. 10 and 11 compare the nine-level phase output voltage along with the respective THD spectra at the modulation index of 1 to validate and establish the merits of the PD based new Multicarrier- 60^o PWM and the MCPWM in terms of a lower THD. Phase- *A* current together with the corresponding phase voltage obtained at the same modulation index displayed in Fig. 12 augurs the phase alignment nature between the current and voltage and enumerates the suitability of the MLI to support a wide variety of applications.

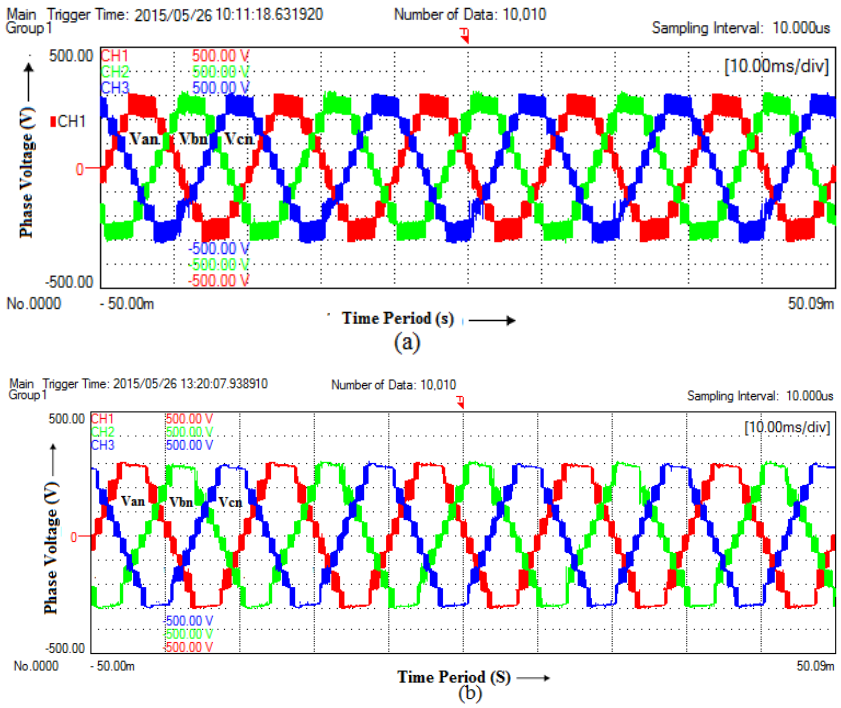

Fig. 10. Phase voltage waveforms for: a) PD MCPWM, b) PD Multicarrier- 60^o PWM

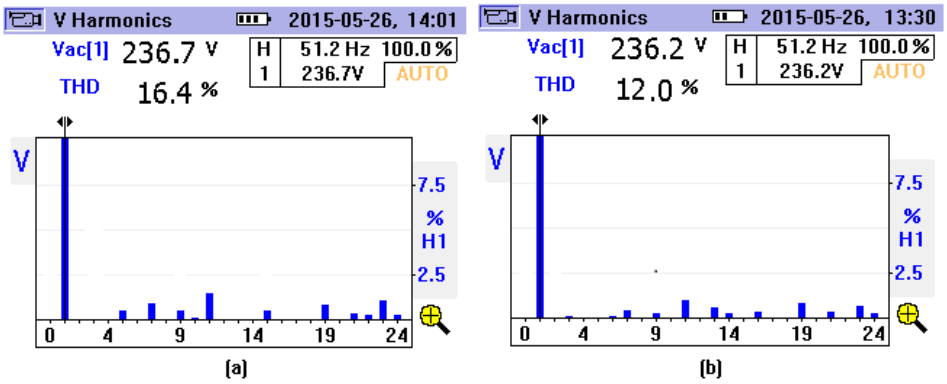

Fig. 11. Phase voltage spectrum V_a for: a) PD MCPWM, b) PD multicarrier- 60^o PWM

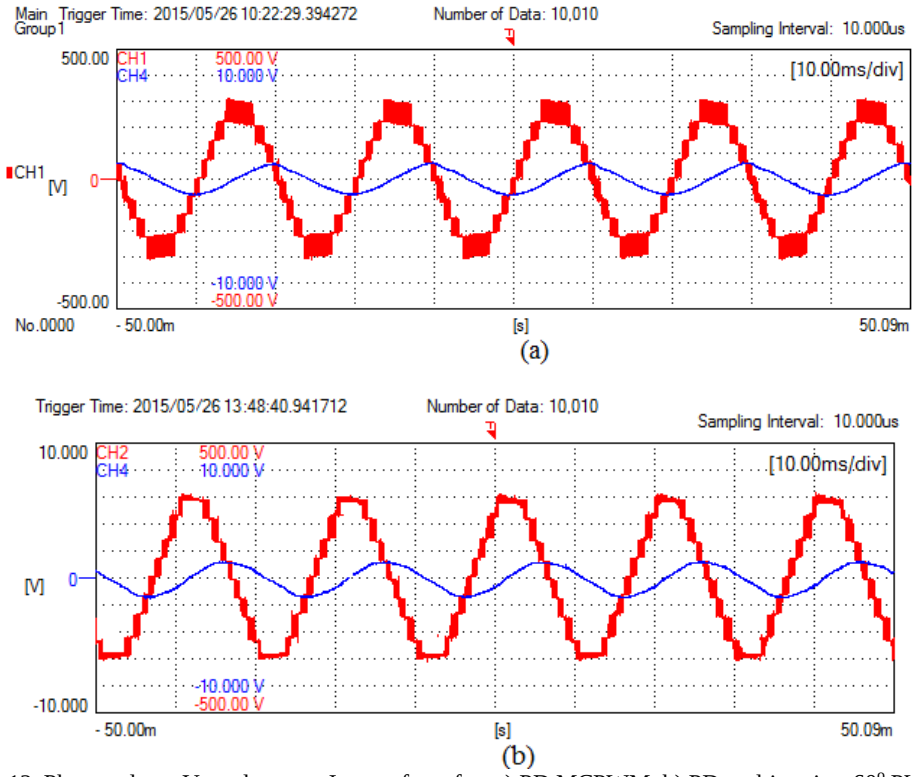

Fig. 12. Phase voltage V_a and current I_a waveform for: a) PD MCPWM, b) PD multicarrier- 60° PWM

VIII. CONCLUSION

A new three phase series parallel switched MLI has been developed to facilitate reduction in the switch count along the path for the current to reach different levels of the output voltage. The reduced switch count topology has been espoused as a viable method for generating a nearly sinusoidal voltage. A new approach has been introduced to the process of generating the PWM pulses for the switches in the MLI. The simulation results have been extricated with a comparative study of the new Multicarrier- 60° PWM over the existing MCPWM, VFCBPWM and ISCPWM to show a rise in the fundamental component of the phase voltage along with a systematic lowering of the THD levels. The FPGA based experimental prototype has been realized to establish the viability of the new CMLI topology and find a space in real world applications. The exquisite operation of the MLI will explore new areas of applications and carry the benefits of the formulation to reach industrial utilities.

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