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Reduce the Component Count of Three-Phase T-Type Multilevel Inverter Based on Matrix Converter

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***Abstract*—** This study provides a T-type multilevel inverter-matrix converter topology that minimizes hardware complexity while providing additional levels of output voltages for three-phase converters. The T-type multilevel inverter (TMLI) configuration utilizes three asymmetric T-type multilevel inverters and a 3×3 matrix converter (3TMLIMC) for voltage sharing and additional output levels without increasing the count of active power components. A VSA is proposed to manage the switching states to guarantee proper voltage converter function. Two cases are examined: a configuration with three three-level TMLIs (3L-TMLI) for a seven-level (7L) converter and a configuration with three five-level TMLIs (5L-TMLI) for a thirteen-level (13L) converter. The proposed architecture and control strategy are verified through theoretical analysis and MATLAB/Simulink simulations. The design is confirmed to be feasible through an evaluation of its performance. A component count (CC) analysis of the proposed architecture and conventional multilevel inverter topologies demonstrates the proposed architecture's reduced component count and overall improved efficiency. Therefore, the proposed 3TMLIMC topology stands out as very promising for innovative applications in medium to high-power electronics.

***Keywords*—** Matrix converter; T-type multilevel inverter (TMLI); DC-AC converter; Multilevel voltage generation; Voltage selection algorithm (VSA); Total harmonic distortion (THD); Component count (CC); MATLAB/Simulink.

1. INTRODUCTION

Multilevel inverters (MLIs) have been created and used for more and more applications in medium- and high-voltage power conversion in the last few decades [1, 2]. MLIs accomplish high power quality, harmonic distortion, and operational flexibility by combining discrete voltage levels and synthesizing voltage waveforms of different quality [3]. Some of the most commonly used topologies are the diode-clamped MLI (DCMLI) [4], flying-capacitor MLI (FCMLI) [5], and cascaded H-bridge MLI (CHMLI) [6]. Although these configurations possess high-voltage output capabilities, they are high in component count (CC), use a lot of passive components, and have DC-link voltage balancing and stabilization problems.

These issues are the reason T-type multilevel inverters (TMLIs) have gained so much attention in the last several years. These have successfully combined the advantages of conventional two-level converters with multilevel topologies [7, 8]. TMLIs decrease the amount of switching and conduction losses, have fewer semiconductor devices, and use a considerably

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lower amount of bulky passive components [9]. In addition, unlike traditional AC-DC-AC converters, matrix converters (MCs) offer more power density and reliability because they allow direct AC-AC power conversion without a DC-link capacitor [10]. MCs are compact systems that perform bidirectional power conversion with high reliability and power density. More specifically, the indirect matrix converter (IMC) performs AC–DC–AC conversion with an embedded rectifier and inverter with no energy storing intermediate link. This topology leads to well controlled sinusoidal input and output currents, a power factor at the input with a value of one, and high control flexibility [11, 12].

There are still research gaps to be filled, however advances in the integration of TMLI with MC still needs to be done, achieving the fundamental goal of maintaining high quality waveforms, maintaining high efficiency and compactness, while reducing CC. For advanced energy conversion systems to be developed, compactness, efficiency, and cost-effectiveness for industrial applications and for recycling electrical energy will be essential. As a result, there has been rigorous work to limit the amount of active and passive power electronic components in the topologies of MLIs. Constructively, asymmetrical configurations and hybrid setups with disparate values of DC-link voltage have been able to yield multilevel outputs with fewer elements. For example, in the case of a five-level T-type inverter, clamping diodes and flying capacitors can be eliminated leading to a structure that is more simplified and attractive especially for applications with high–power-quality and low-voltage. In recent reviews, reduced CC topologies show that the overall cost and device count, along with the performance, can be maintained and even improved by optimizing the number of components per output voltage level [13, 14].

Additionally, the cross-square-switched T-type modular structures show that, with the innovative switching methods and few voltage sources, high performance at low total harmonic distortion (THD) is achievable [15]. These results reinforce the idea of lower CC not necessarily leading to worse output performance [16, 17].

This paper puts forth a new converter architecture, the three T-type multilevel inverter matrix converters (3TMLIMC), aimed at generating AC output voltages from DC sources. The design is analyzed through two configurations, a seven-level (7L) and a thirteen-level (13L) 3TMLIMC. In the 7L scenario, three unbalanced three-level (3L) TMLIs are linked to a MC, while in the 13L scenario, three unbalanced five-level (5L) TMLIs are used. A voltage selection algorithm (VSA) is designed to manage the functions of the TMLIs and the MC. The proposed topology attains greater voltage levels with a minimal number of components and the output served shows a lower THD compared to the conventional MLI topologies. A complete comparative analysis will be carried out to compare present designs with the new proposed design to illustrate the advantages.

2. METHODOLOGY OF PROPOSED DESIIGN

In this section, the theory of the proposed design is presented, the main idea of proposed design is generate three-phase MLI with minimum CC at low switching frequency, where low switching frequency save more in power loss of switching and no need for high quality of low pass filter. The common TMLI is used at 3L and 5L, respectively. After that, a common 3x3 MC is presented separately, then linked to the proposed unbalanced TMLI [18, 19].

2.1. T-type multilevel inverter at 3L and 5L

The power electronics circuit of single-phase 3L TMLI is presented in Fig. 1, as is well known, the TMLI at 3L has three output voltages: V1, 0V, and −V2. Four IGBT switches are used and controlled by switch states as presented in Table 1. Where the proposed design use three of TMLI; TMLI1, TMLI2, and TMLI3.

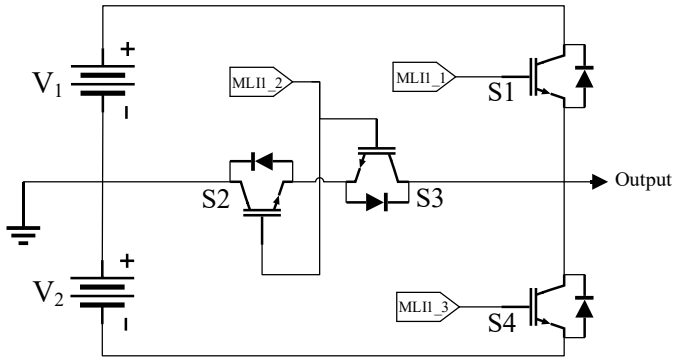


Fig. 1. Single-phase 3L TMLI.

Table 1. Switching states of a single-phase 3L TMLI.

Step	Switches State (ON / OFF)			Output Voltage [V]
	S1	S2 & S3	S4	
1	ON	OFF	OFF	+V1
2	OFF	ON	OFF	0
3	OFF	OFF	ON	-V2

The power electronics circuit of single-phase 5L TMLI presented in Fig. 2, has three output voltages: (V1+ V2), (V2), (0V), (V3), and −(V3+V4). Eight power electronics switches are used, the switched state control is illustrated in Table 2.

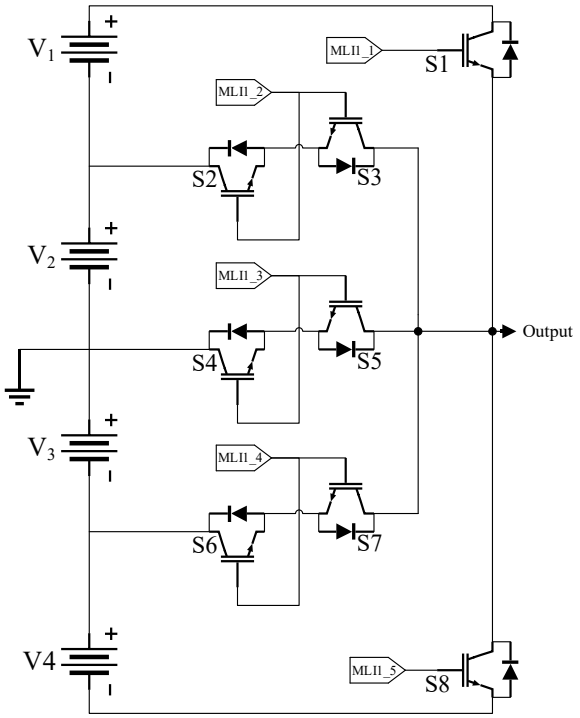


Fig. 1. Single-phase 5L TMLI.

Table 2. Switching states of a 5L TMLI.

Output No.	Switches State (ON / OFF)					Output Voltage [V]
	S1	S2 & S3	S4 & S5	S6 & S7	S8	
1	ON	OFF	OFF	OFF	OFF	+(V1 + V2)
2	OFF	ON	OFF	OFF	OFF	+V2
3	OFF	OFF	ON	OFF	OFF	0
4	OFF	OFF	OFF	ON	OFF	−V3
5	OFF	OFF	OFF	OFF	ON	−(V3 + V4)

2.2. Matrix Converter

A general AC-AC MC is used, Fig. 3 shows the nine switches of the MC as follows MC11, MC12, MC13, MC21, MC22, MC23, MC31, MC32, and MC33. In the proposed design, the input signal received from three of TMLI as follows; TMLI1, TMLI2, and TMLI3. That is, as TMLI1 circuit connected to MC11, MC12, and MC13; TMLI2 is connected to MC21, MC22, and MC23; and TMLI3 is connected to MC31, MC32, and MC33, respectively.

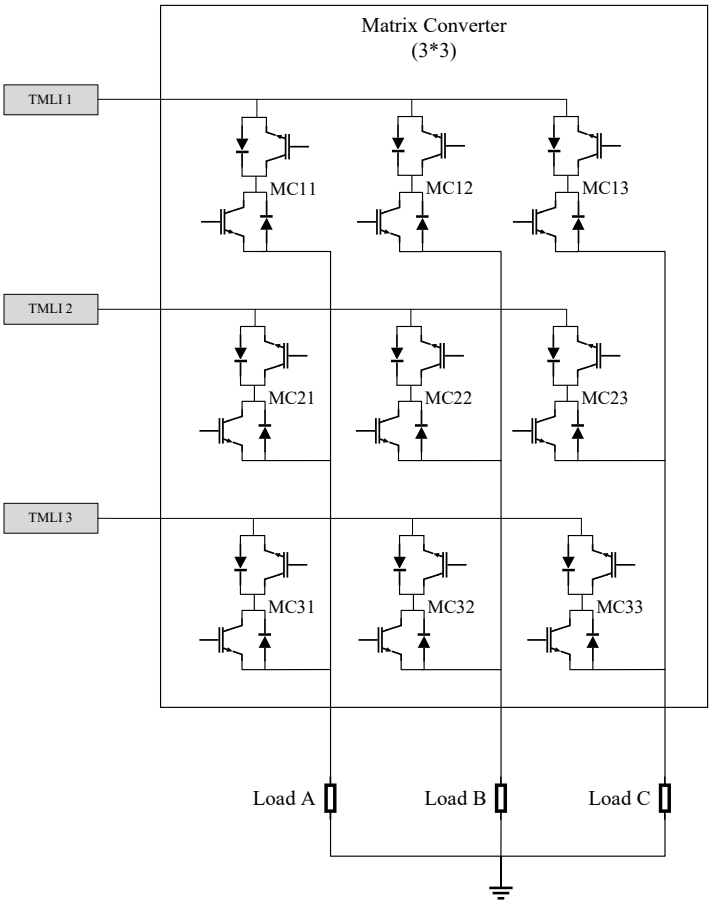


Fig. 2. Design of 3X3 MC.

The MC uses a different mode (M) operation to operate the MC. Equation (1) presents the location switch of MC in matrix mode, where Eqs. (2) to (13) present the equations mode of the proposed design to run the 3TMLIMC at 7L and 13L [20, 21].

$$M = \begin{bmatrix} MC11 & MC12 & MC13 \\ MC21 & MC22 & MC23 \\ MC31 & MC32 & MC33 \end{bmatrix} \quad (1)$$

$$M1=\begin{bmatrix}1&0&0\\0&1&0\\0&0&1\end{bmatrix} \quad (2) \qquad M2=\begin{bmatrix}0&0&1\\0&0&0\\1&1&0\end{bmatrix} \quad (3) \qquad M3=\begin{bmatrix}0&1&0\\1&0&0\\0&0&1\end{bmatrix} \quad (4)$$

$$M4=\begin{bmatrix}1&0&0\\0&1&1\\0&0&0\end{bmatrix} \quad (5) \qquad M5=\begin{bmatrix}0&0&1\\1&0&0\\0&1&0\end{bmatrix} \quad (6) \qquad M6=\begin{bmatrix}0&1&0\\0&0&0\\1&0&1\end{bmatrix} \quad (7)$$

$$M7=\begin{bmatrix}1&0&0\\0&0&1\\0&1&0\end{bmatrix} \quad (8) \qquad M8=\begin{bmatrix}0&0&1\\1&1&0\\0&0&0\end{bmatrix} \quad (9) \qquad M9=\begin{bmatrix}0&1&0\\0&0&1\\1&0&0\end{bmatrix} \quad (10)$$

$$M10=\begin{bmatrix}1&0&0\\0&0&0\\0&1&1\end{bmatrix} \quad (11) \qquad M11=\begin{bmatrix}0&0&1\\0&1&0\\1&0&0\end{bmatrix} \quad (12) \qquad M12=\begin{bmatrix}0&1&0\\1&0&1\\0&0&0\end{bmatrix} \quad (13)$$

2.3. Voltage Selection Algorithm

The VSA is applied to synchronize the operation of TMLI1, TMLI2, and TMLI3. Table 3 presents the VSA at 7L 3TMLIMC, three VSA groups are used: VSA1, VSA2, and VSA3. At VSA1 the voltage groups contain 200V, 0V, and −200V, where VSA2 contains 300V, −100V and −100V. The VSA3 contains 100V, 100V, and −300V.

At 13L 3TMLIMC, five different groups of VSA are required: VSA1, VSA2, VSA3, VSA4, and VSA5. The same value of VSA1, VSA2, and VSA3 that are used in 7L is used in 13L and namely VSA1, VSA3, and VSA5, respectively. At 13L, the VSA 2 contains 150V, 50V, and −250V, where VSA4 contains 250V, −50V, and −150V.

Table 3. Proposed groups of the voltage selection algorithm .

# of levels / Groups	VSA1	VSA2	VSA3	VSA4	VSA5
7L 3TMLIMC	200	300	100		
	0	−100	100		
	−200	−100	−300		
13L 3TMLIMC	200	150	300	250	100
	0	50	−100	−50	100
	−200	−250	−100	−150	−300

VSA simplified the proposed design operation, as will be presented in complete operation in the following section. Knowing that, an increasing number of levels causes to increase number of VSAs. Equation 14 presents the number of VSA groups required to design based on the number of levels.

$$VSA_{groups}=\frac{\#\ of\ levels+2}{3} \quad (14)$$

2.4. Proposed 7L 3TMLIMC

The proposed circuit design of 7L 3TMLIMC is shown in Fig. 4, where three of the unbalanced TMLI are connected to MC. To simplify the methodology, different voltage source values are connected to TMLI1, TMLI2, and TMLI3. TMLI1 generates 300V and −300V, where TMLI2 generates 200V and −100V, and TMLI3 generates 100V and −200V output voltages. The output of MC is connected to Load A, Load B, and Load C, where Load A receives the signal of TMLI1, TMLI2, and TMLI3 by MC switches MC11, MC21, and MC31, respectively.

Consequently, Load B and Load C are linked to TMLI1, TMLI2, and TMLI3 by certain MC switches presented in Fig. 4.

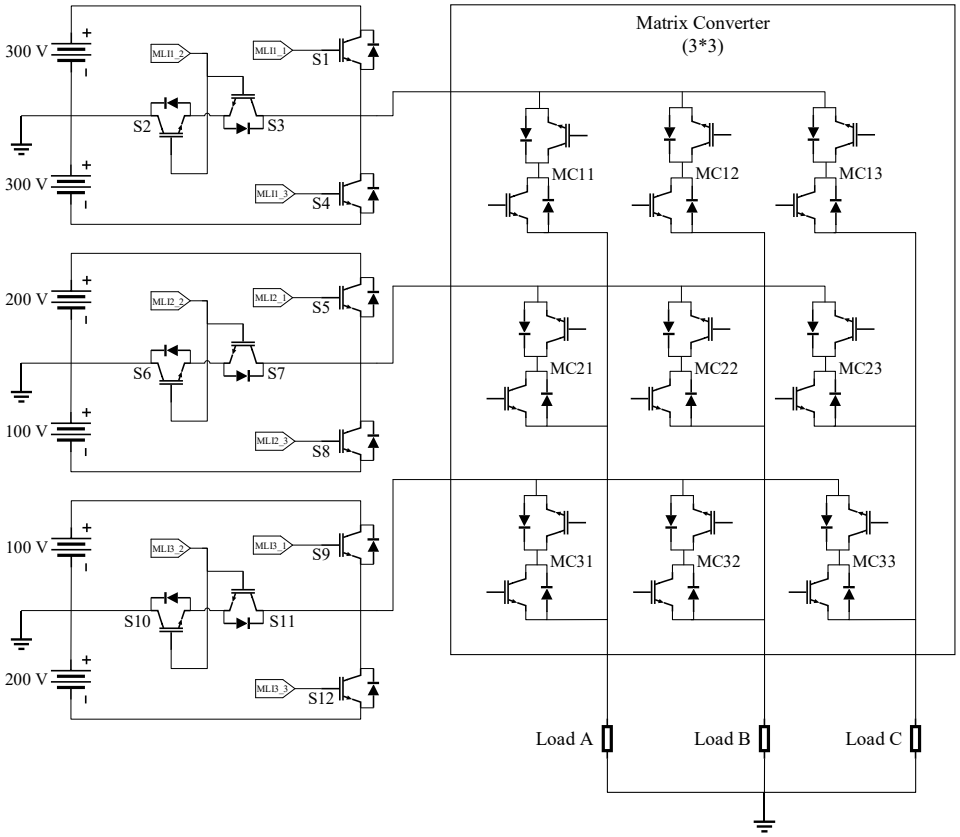
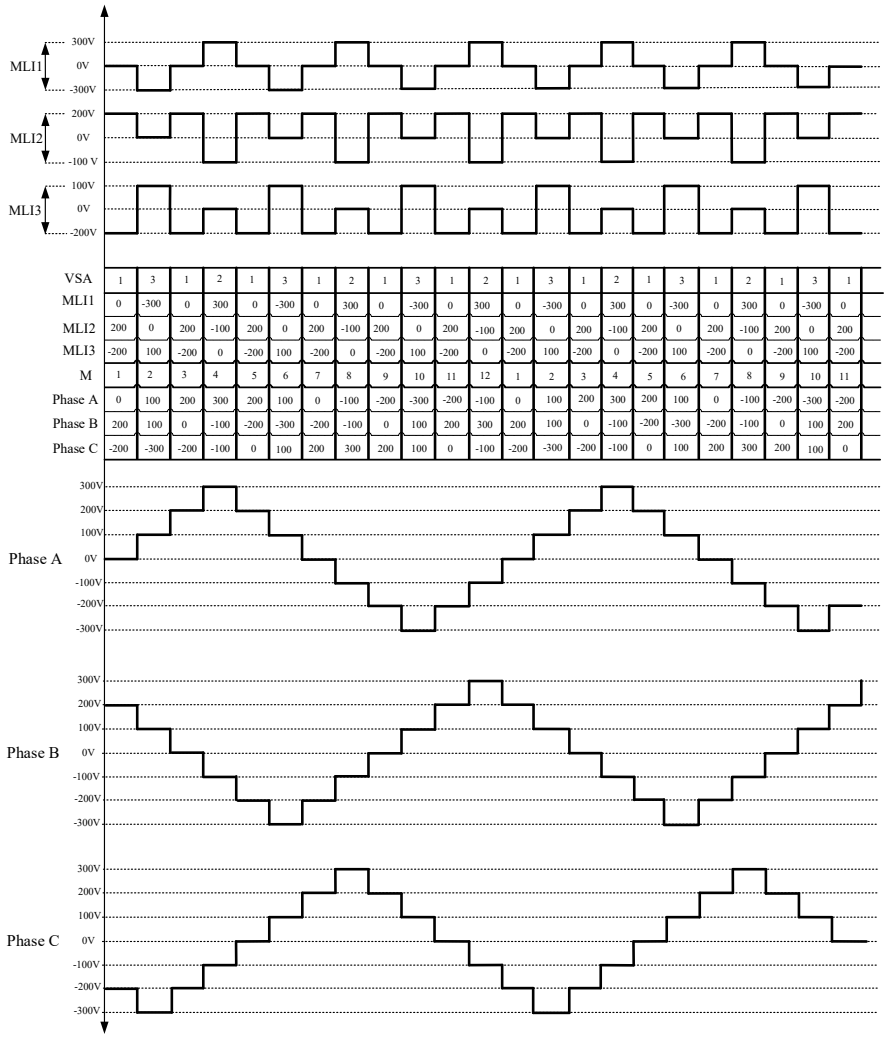


Fig. 3. Circuit design of proposed 7L 3TMLIMC.

The complete operation of 7L 3TLIMC is presented in Fig. 5. The output signal of TMLI1, TMLI2, and TMLI3 is shown, and VSA is also presented in the figure. As previously mentioned, three VSAs are used: VSA1, VSA2, and VSA3. Each VSA used to operate the TMLI and synchronize it by MC modes. VSA1 is synchronized with an odd number of MC modes: M1, M3, M5, M7, M9, and M11. Where VSA2 and VSA3 are linked with even modes of MC, VSA2 is linked to MC mode; M4, M8, and M12, the VSA3 is linked to M2, M6, and M10, respectively. As a result, a three-phase output signal of Load A, Load B, and Load C is generated. The output triangular signal of 7L 3TMLIMC is found at the end of Fig. 5. The waveform of the triangular signal has high THD, thus improved output signal will be presented after 13L 3TMLIMC.

2.5. Proposed 13L 3TMLIMC

The power electronics circuit of the proposed design 13L 3TMLIMC is presented in Fig. 6, where three of the unbalanced TMLI are connected to MC. Different voltage source value is connected to TMLI1, TMLI2, and TMLI3. TMLI1 generates 300V, 250V, −250V and −300V, where TMLI2 generates 200V, 150V, −50V and −100V, and TMLI3 generates 100V, 50V, −150V and −200V output voltages. The output of MC is connected to Load A, Load B, and Load C, where Load A receives the signal of TMLI1, TMLI2, and TMLI3 by MC switches MC11, MC21, and MC31, respectively. consequently, Load B and Load C are linked to TMLI1, TMLI2, and TMLI3 by certain MC switches presented in Fig. 6.



VSA	1	3	1	2	1	3	1	2	1	3	1	2	1	3	1	2	1	3	1	2	1	3	1
MLI1	0	-300	0	300	0	-300	0	300	0	-300	0	300	0	-300	0	300	0	-300	0	300	0	-300	0
MLI2	200	0	200	-100	200	0	200	-100	200	0	200	-100	200	0	200	-100	200	0	200	-100	200	0	200
MLI3	-200	100	-200	0	-200	100	-200	0	-200	100	-200	0	-200	100	-200	0	-200	100	-200	0	-200	100	-200
M	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11
Phase A	0	100	200	300	200	100	0	-100	-200	-300	-200	-100	0	100	200	300	200	100	0	-100	-200	-300	-200
Phase B	200	100	0	-100	-200	-300	-200	-100	0	100	200	300	200	100	0	-100	-200	-300	-200	-100	0	100	200
Phase C	-200	-300	-200	-100	0	100	200	300	200	100	0	-100	-200	-300	-200	-100	0	100	200	300	200	100	0

Fig. 4. The complete operation of 7L 3TMLIMC.

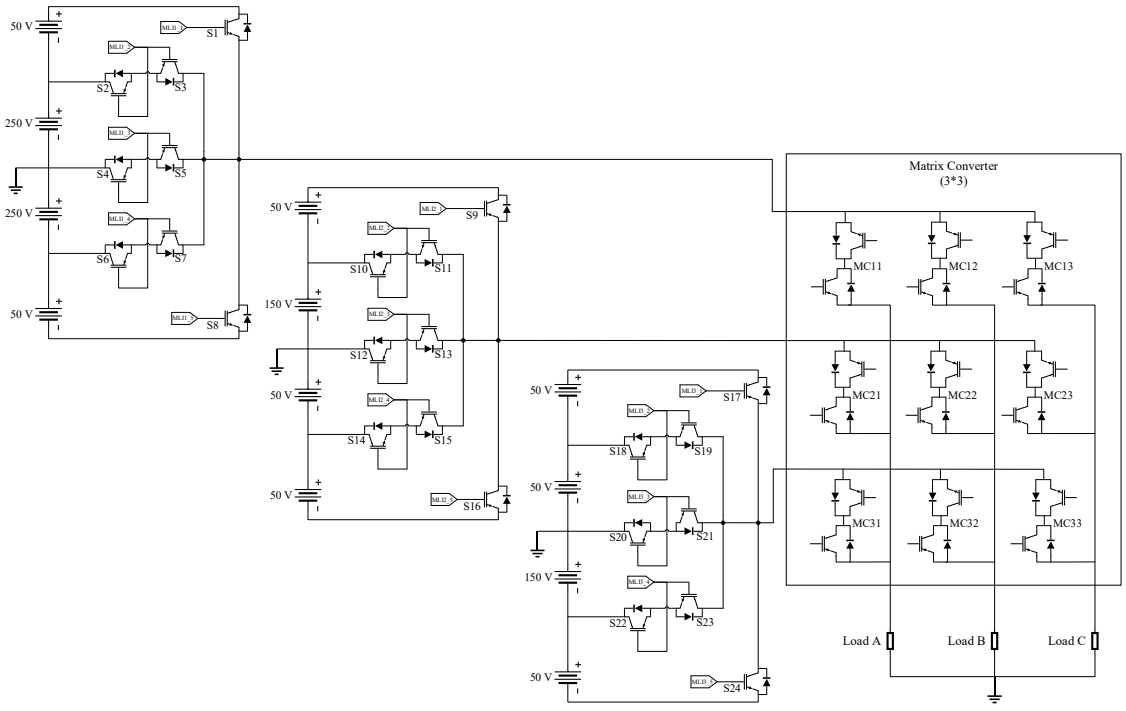


Fig. 5. Circuit design of proposed 13L 3TMLIMC.

The complete operation of 13L 3TLIMC is shown in Fig. 7. Output signals of TMLI1, TMLI2, and TMLI3 are shown, and VSA is also presented in the figure. As previously mentioned, five VSAs are used: VSA1, VSA2, VSA3, VSA4, and VSA5. Each VSA used to operate the TMLI and synchronize it by MC modes. VSA1 is synchronized with an odd number of MC modes: M1, M3, M5, M9, and M11. Where VSA2 and VSA3 are linked with even modes of MC, VSA2 is linked to MC mode; M4, M8, and M12, the VSA3 is linked to M2, M6, and M10, respectively. As a result, a three-phase 13L output signal of Load A, Load B, and Load C is generated. The output voltage of the triangular signal in 13L 3TMLIMC is found at the end of Fig. 7. This waveform of a triangular signal has high THD, although it has a high number of levels. So, in this paper, an improved output signal will be presented to generate more sinusoidal waveform signal with lower THD.

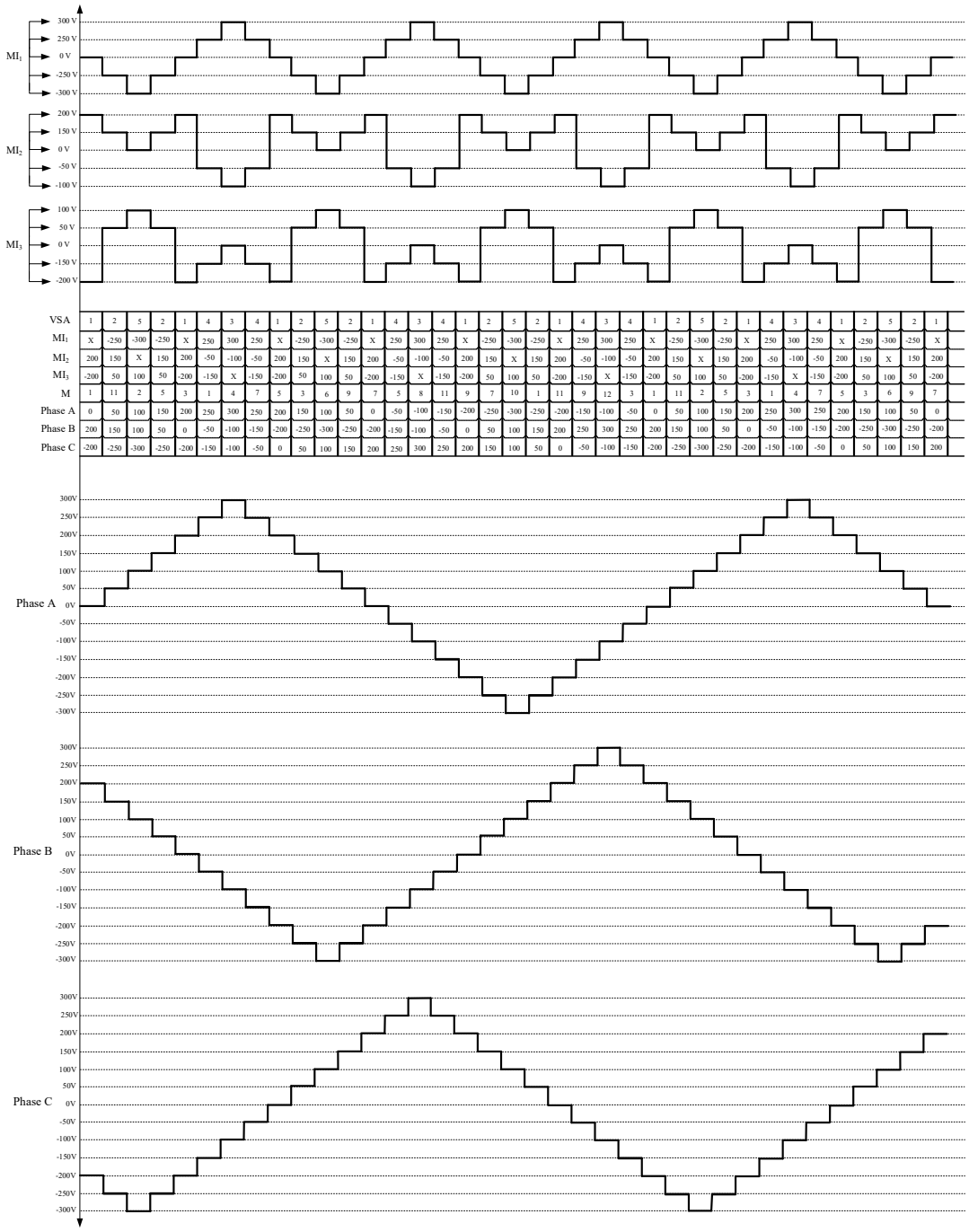


Fig. 6. The complete operation of 13L 3TMLIMC.

3. SIMULATION AND RESULTS

3.1. Results of 3TMLIMC at 7L and 13L

The validation and verification of the proposed design are illustrated in this section by presenting the output voltage waveforms of 7L and 13L. Figs. 8 and 9 present the output signal of 7L and 13L 3TMLIMC of phases A, B, and C respectively. The output voltage signals of the phases have ten periods and 50Hz frequency operation.

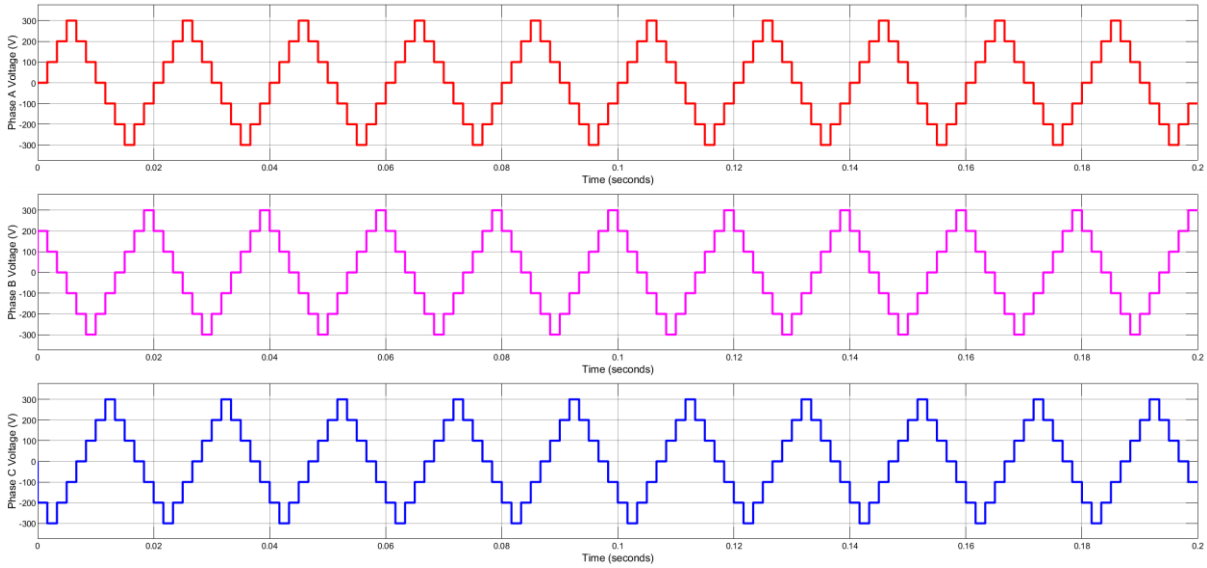


Fig. 7. Three-phase output voltage of 7L 3TMLIMC.

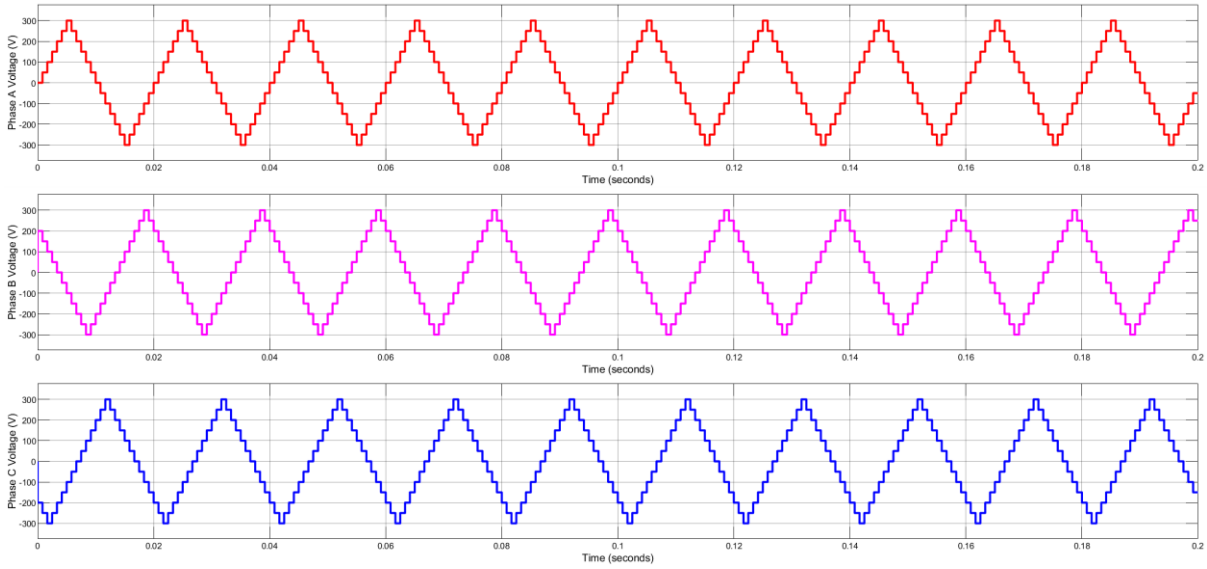


Fig. 8. Three-phase output voltage of 13L 3TMLIMC.

3.2. Modified voltage source in proposed design

The operation of the proposed 3TMLIMC is optimized to generate low THD using low switching frequency. The upgrade voltage values of 7L are found using Eq. (15), where the V_{max} is present the maximum peak value of voltage that required when the certain number of sine wave step (n_{step}) is applied. On the other hand, the voltage values of 13L are found using Eq. (16) [22, 23].

$$Vs_{@7L} = V_{max} * Sin\left(n_{step} * \frac{360}{12}\right) \quad (15)$$

$$Vs_{@13L} = V_{max} * Sin\left(n_{step} * \frac{360}{24}\right) \quad (16)$$

Table 4 presents the modified voltage source required to optimize the 7L 3MLIMC, 100V is replaced by 150V, and 200V is replaced by 259.8V. Both 0V and 300V are kept as it.

Table 4. New capacitor charge values for 7 output levels MLI.

Old Voltage	n_{step}	New Voltage
0	0	0
100	1	150
200	2	259.8076
300	3	300

Table 5 presents the modified voltage source required to optimize the 13L 3MLIMC, the 50V, 100V, 150V, 200V, and 250V are replaced by 77.64V, 150V, 212.13V, 259.8V, and 289.77V, respectively. Both 0V and 300V are kept as it. Based on the modified voltage source, the output results on MATLAB Simulink are illustrated in Figs. 10 and 11.

Table 5. New capacitor charge values for 13 output levels MLI.

Old Voltage	n_{step}	New Voltage
0	0	0
50	1	77.64571
100	2	150
150	3	212.132
200	4	259.8076
250	5	289.77
300	6	300

3.3. Proposed design THD results

The THD values of the proposed system are summarized in Table 6. At 7L, the proposed design THD has 16.94% before voltage source modification and 7.78% after voltage source modification. In 13L 3TMLIMC, the THD has 12.99% before voltage source modification and 3.8% after voltage source modification is applied. In addition, Fig. 12 presents the spectrum of 13L 3TMLIMC, which finds the lowest THD.

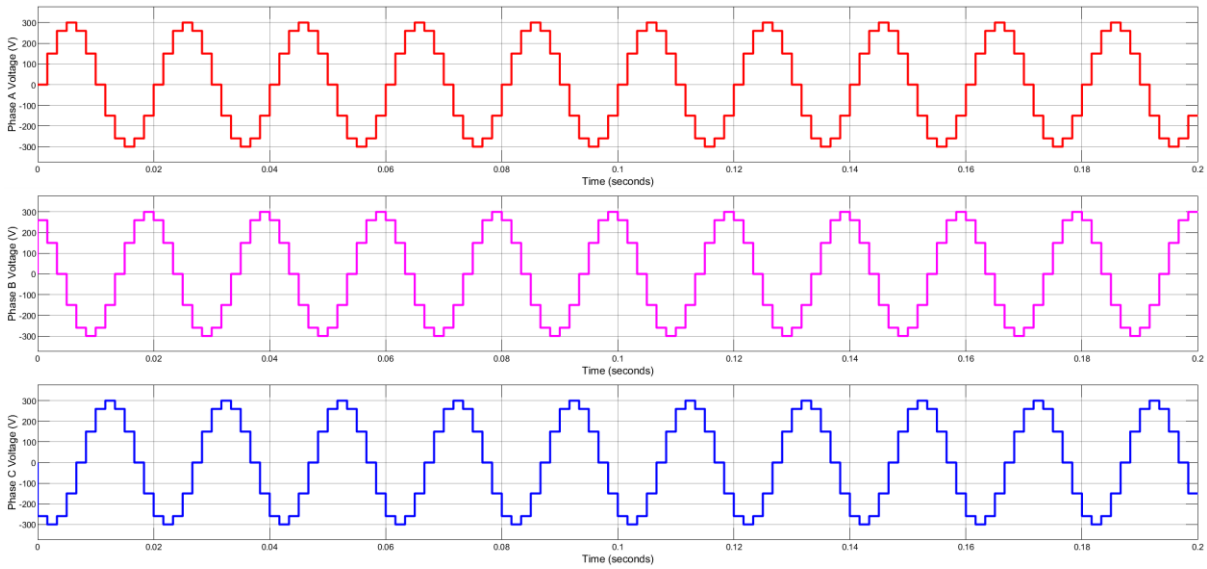


Fig. 9. Three-phase output of 7L TMLIMC after voltage source modification.

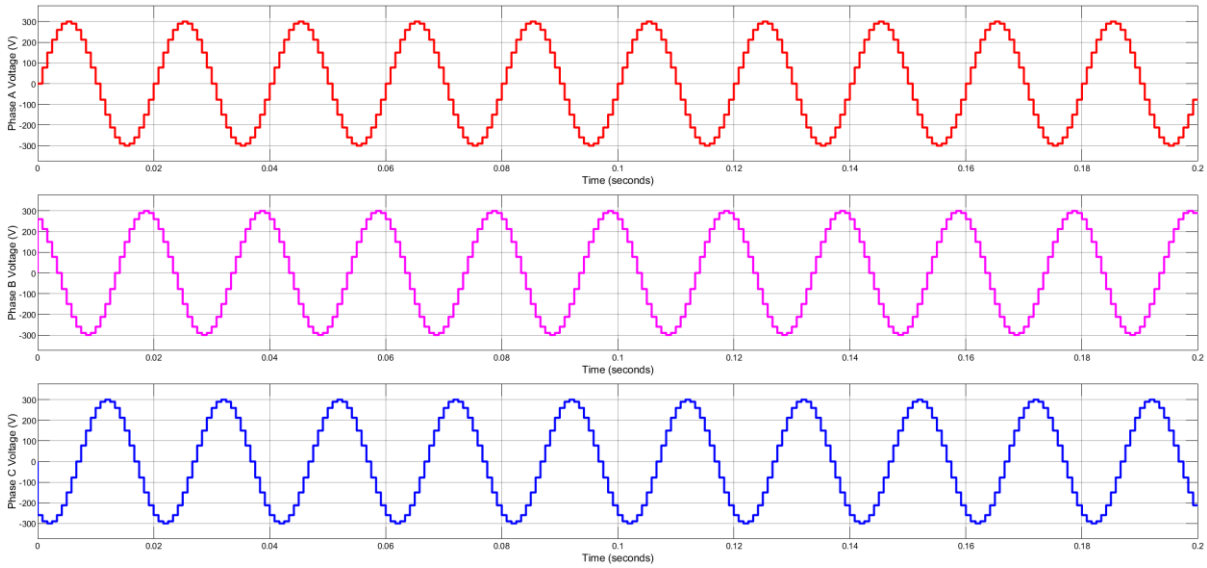


Fig. 10. Three-phase output of 13L TMLIMC after voltage source modification.

Table 6. THD of 3TMLIMC at 7L and 13L before and after voltage source modification.

Proposed design 3TMLIMC	THD (%)	
	Before voltage modification	After voltage modification
7L	16.94%	7.78%
13L	12.99%	3.80%

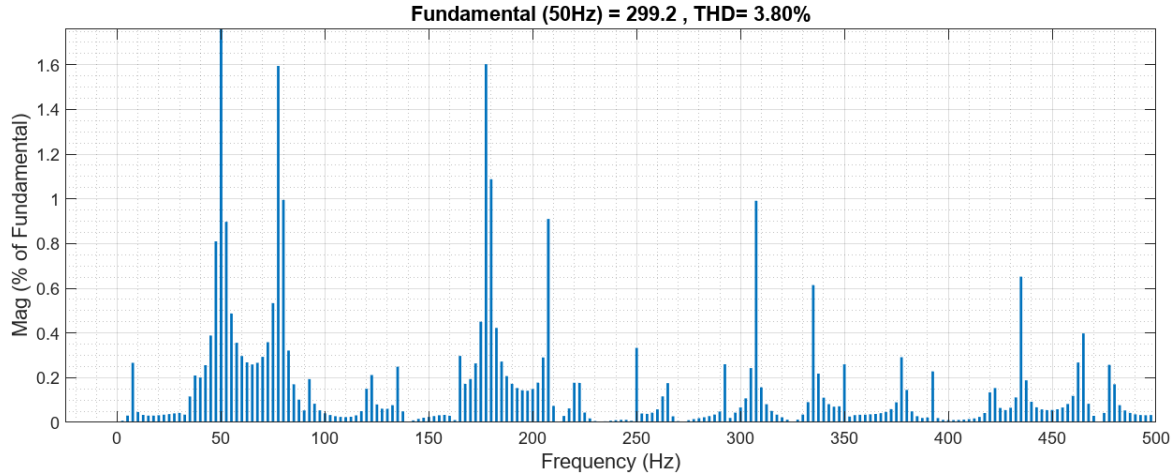


Fig. 11. Total Harmonic distortion analysis of 5L MLI after modification.

3.4. Results comparison

An expression for the anticipated CC for the proposed topology is presented. The CC for the three TMLI stages is $2(m-1)$, plus nine additional switches for the MC. The converter is then compared to the most commonly used topologies, such as the diode-clamped MLI (DCMLI), cascaded H-bridge MLI (CHMLI), flying-capacitor MLI (FCMLI), and standard TMLI, shown in Table 7. Also, some recent structures of multilevel inverters are examined for comparison, including the bidirectional switch multilevel inverter (BSMLI), multilevel modular multilevel inverter (MMMLI), transistor-clamped multilevel inverter (TCMLI), series-connected switched sources (SCSS), and developed H-bridge multilevel inverter (DHMLI).

Table 7. proposed design compared with the pervious study [24, 25].

MLI	Main Switch @ three-phase						DC sources	control	year	Ref
	Unidirectional switch			Bidirectional switch						
	Equation	@7L	@13L	Equation	@7L	@13L				
DCMLI	$6(m-1)$	36	72	0	0	0	$6(m-1)$	simple	1981	[3]
FCMLI	$6(m-1)$	36	72	0	0	0	$6(m-1)$	simple	1992	[4]
CHMLI	$6(m-1)$	36	72	0	0	0	$6(m-1)$	simple	2002	[5]
TMLI	12	30	48	$3(m-1)$	30	48	[6]	simple	2019	[6]
BSMLI	$6(m+1)$	48	84	0	0	0	[7]	average	2006	[7]
MMMLI	12	12	12	$\frac{3(m+1)}{2}$	12	21	[8]	average	2012	[8]
TCMLI	$4(m+1)$	32	56	0	0	0	[9]	average	2013	[9]
SCSS	$3(m+3)$	24	42	0	0	0	[10], [11]	average	2014	[10, 11]
SPSS	$\frac{3(3m-1)}{2}$	30	57	0	0	0	$\frac{3(7m-13)}{2}$	average	2010	[12]
CBSCMLI	0	0	0	$3(m+1)$	24	42	[13]	average	2008	[13]
RV	$3(m+3)$	30	48	0	0	0	$9(m-1)$	average	2008	[14]
Proposed Design	$2(m-1)$	12	24	9	9	9	$(m-1)$	hard	-	-

The suggested configuration accomplishes the lowest possible CC, needing 12 main power switches for a 7L structure and 24 for a 13L structure. The proposed approach, merging the TMLI and the MC, achieves a CC reduction of 53% for the 7L and 83% for the 13L in comparison to conventional designs. This emphasizes the growing positive impact in relative CC reduction, attributed to the increase in output voltage levels, thus showcasing the proposed architecture's structural efficiency and scalability. The focus of this comparison is on the number of DC sources and the complexity of control design, where the proposed design shows the least number of DC sources, but operational design is highly complex. In the proposed design, the series connection of both converters, TMLI and MC, increases the complexity of control.

4. CONCLUSIONS

The research presented in this paper has made a first theoretical and computational analysis of a novel architectural combination for three T-type multilevel inverter and matrix converters (3TMLIMC). The proposed topology derives a unique advantage of increasing the TMLI output voltage levels number while maintaining the same number of inverter components, through a mechanism of voltage sharing among the output TMLIs. A dedicated voltage selection algorithm (VSA) was designed and applied to both seven-level (7L) and thirteen-level (13L) configurations. The proposed topologies for both 7L and 13L 3TMLIMCs were verified by theoretical analysis and by simulations in MATLAB/Simulink. The simulation results were able to demonstrate the proposed topology's performance around multilevel voltage synthesis and voltage level equidistance, coupled with THD within the permissible range, with THD of 7.78% and 3.8% for the 7L and 13L configurations respectively. A unique and comprehensive analysis of both classical and contemporary MLI topologies established and confirmed the proposed design's structural advantages. Utilizing the CC based metric, the proposed converter reduced the number of main power switches by 54% for the 7L case and by 83% for the 13L case in comparison to the most contemporary design. Considering this fact, the

3TMLIMC can be classified as a compact, efficient and inexpensive design for any advanced multilevel power conversion applications.

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