JJEE

Volume 12 | Number 3 | September 2026 | Pages 535-544

Jordan Journal of Electrical Engineering

ISSN (print): 2409-9600, ISSN (online): 2409-9619

Homepage: jjee.ttu.edu.jo

A 10-bit Asynchronous SAR ADC with Dynamic Clock Phase Generation for Ultra-Low Power Mixed-Signal Applications in 45 nm CMOS

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Received: Aug 05, 2025 *Revised: Dec 09, 2025* *Accepted: Dec 23, 2025* *Available online: Aug 15, 2026*

***Abstract*—** The increasing demand for energy-efficient and high-performance analog-to-digital converters (ADCs) in modern wireless communication systems necessitates the development of architectures that balance speed, accuracy, and power consumption. This work addresses the challenge by designing and verifying a synchronous Successive Approximation Register (SAR) ADC optimized for low-power mixed-signal applications using 45nm CMOS technology. The proposed ADC adopts a fully dynamic architecture to eliminate static power dissipation, making it highly suitable for energy-constrained environments. Key architectural components include a precision clock phase generator for accurate timing control, a capacitive Digital-to-Analog Converter (CAPDAC) for power-efficient signal conversion, and a StrongArm dynamic comparator for fast and robust decision-making. The design achieves a resolution of 10 bits with a high Effective Number of Bits (ENOB) of 9.86 bits and SINAD of 61.12 dB at 100 MS/s sampling rate, while consuming only 2.63 µW. To ensure functional correctness and performance reliability, a modular "divide-and-conquer" verification strategy is implemented. Each subsystem, including the comparator, DAC, and clock generator, is analyzed independently to identify and quantify sources of noise and error. Advanced simulation tools such as Virtuoso ADE and Cadence Spectre APS are employed, complemented by pnoise and transient noise analysis techniques. Low Discrepancy Sampling (LDS)-based Monte Carlo simulations are conducted to evaluate design robustness across process-voltage-temperature (PVT) variations. The final outcome verifies the viability of the proposed design for integration into modern system-on-chip (SoC) platforms. The combination of a dynamic, low-power architecture and structured verification methodology contributes to the advancement of energy-efficient, high-precision SAR ADCs for embedded systems.

***Keywords*—** Analog-to-digital converters (ADC); Successive approximation register (SAR), Low power mixed signal design.

1. INTRODUCTION

Modern electronic systems increasingly demand analog-to-digital converters (ADCs) that simultaneously achieve high speed, medium resolution, and ultra-low power consumption. This convergence of requirements is particularly critical in emerging applications such as Internet of Things (IoT) devices, biomedical monitoring systems, and artificial intelligence edge computing, where battery life and thermal constraints impose stringent power budgets while maintaining adequate signal processing performance.

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DOI: https://doi.org/10.5455/jjee.204-1754118338

Among various ADC architectures, Successive Approximation Register (SAR) ADCs have emerged as the preferred solution for medium-resolution applications due to their inherent simplicity, scalability with CMOS technology scaling, and favorable power-speed trade-offs. However, conventional asynchronous SAR ADCs suffer from timing uncertainties and process variations that limit their performance in advanced CMOS nodes, while traditional synchronous implementations often exhibit excessive dynamic power consumption due to continuous clock distribution networks.

This work presents a synchronous SAR ADC architecture specifically optimized for low-power operation in 45 nm CMOS technology. The proposed design addresses the fundamental limitations of existing synchronous SAR implementations through several key innovations: (1) an intelligent clock phase generator that dynamically manages timing signals to minimize switching activity, (2) advanced circuit techniques including bootstrapped sampling switches and dynamic comparators optimized for low-voltage operation, and (3) a comprehensive power management strategy that reduces both static and dynamic power consumption without compromising conversion accuracy.

The primary objective is to achieve a 10-bit resolution ADC with superior power efficiency while maintaining competitive performance metrics, specifically targeting high Effective Number of Bits (ENOB) and optimized Signal-to-Noise and Distortion Ratio (SINAD). The synchronous architecture eliminates the timing uncertainties inherent in asynchronous designs while the proposed clock phase generation scheme significantly reduces the dynamic power overhead typically associated with synchronous operation.

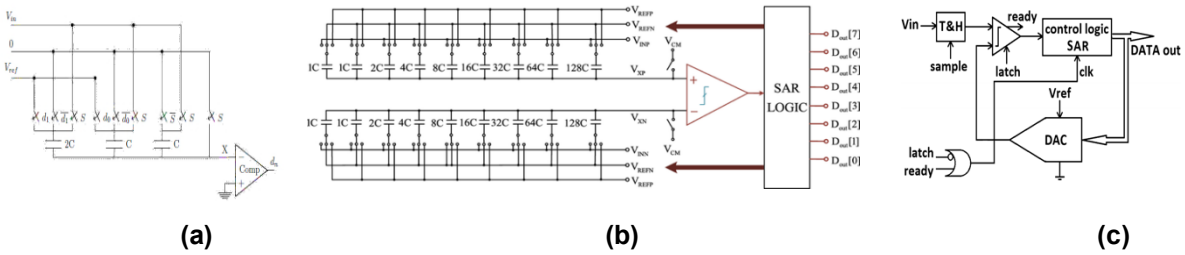
The design methodology incorporates dynamic circuit topologies, including StrongArm latch comparator architectures and capacitor DAC switching mechanisms, which demonstrate enhanced performance with regenerative gain to convert the differential voltage into digital levels compared to conventional implementations [1, 2]. These innovative approaches not only improve power efficiency but also enhance the overall robustness of the conversion process against process, voltage, and temperature variations.

This research contributes to the advancement of energy-efficient data conversion systems by demonstrating how synchronous SAR ADC architectures can be optimized to meet the demanding requirements of next-generation mixed-signal applications. The proposed design establishes new benchmarks for power-efficient ADC implementations in scaled CMOS technologies, providing a foundation for future developments in ultra-low-power analog-to-digital conversion systems.

2. SAR ADC ARCHITECTURE

By comparing the input sampled voltage, Vin, to a DAC output voltage, VDAC, SAR ADCs employ a binary search algorithm to progressively approximate the input voltage. Often, a capacitive charge redistribution technique is used to implement the DAC. Capacitive charge redistribution single-end and differential configuration of SAR ADC are shown in Fig. 1(a) and Fig. 1(b). However, because most of the components are doubled for the differential configuration, the layout area is larger. Synchronous SAR ADC uses the same consistent clock signal, as illustrated in Fig. 1(c), and generates a signal that instructs another block to alter its state, thus reducing the area and power consumption. Traditional ADCs often consume significant power, making them unsuitable for battery-operated or energy-harvesting systems. To address this challenge, researchers have focused on developing ADCs that operate at lower

supply voltages and sampling rates while maintaining acceptable performance metrics as shown in the summary of Table 1.



(a) (b) (c)

Fig. 1. ADC Architecture a) Single-ended 2-bit SAR ADC; b) Differential capacitive DAC of an 8-bit SAR ADC; c)Synchronous SAR ADC

Table 1. Evolutions of ADCs.

Ref.	Total Power Consumption	Effective Number of Bits (ENOB) / bits	Signal-to-Noise and Distortion Ratio (SINAD) / dB	Figure of Merit (FoM) / fJ/step	Limitation
[1]	49.124 µW	7.35	46	15	8-bit resolution insufficient for high-precision applications.
[3]	16nW	8.08	50.4	59.1	1 kS/s sampling rate inadequate for high-speed data processing.
[4]	35.724 µW	10.5	65	7.08	Intrinsic circuit noise affects ADC performance and accuracy.
[5]	45 µW	8.84	55.8	2.01	Sensitivity to 1/f and thermal noise degrades ENOB and performance.
[6]	2.50mW	7.75	48.52dB	163.6	Power consumption needs further optimization for ultra-low-power use.
[7]	4.45 µW	9.97	61.77	22.2	Noise susceptibility affects signal-to-noise ratio (SNR).
[8]	136µW	9.16	53.3	120	2 MS/s conversion speed too slow for high-frequency applications.
[9]	0.3561 µW	10.5	65	7.08	Excessive number of clocks need reduction.
[10]	0.257 mW	10.5	65	7.1	Spider-latch consumes significant power, requires optimization.
[11]	0.124 mW	9.765	60.547	-	Input voltage range (0.2V-0.8V) too restrictive for many applications.
[2]	129.3 µW	8.03	-	-	Sample rate constraints limit high-speed application use.
[12]	505.2 µW	10.45	65.35	41.84	CDAC array area grows exponentially with resolution, increasing chip size and power.
[13]	5.9 mW	6.49	40.83	168	7-bit resolution insufficient for high-precision signal processing.
[14]	407.36 µW	13.89	-	-	Insufficient detailed results provided.
[15]	45 µW	9.35	58.053	75.3	55nm CMOS process limits adoption in advanced technologies.

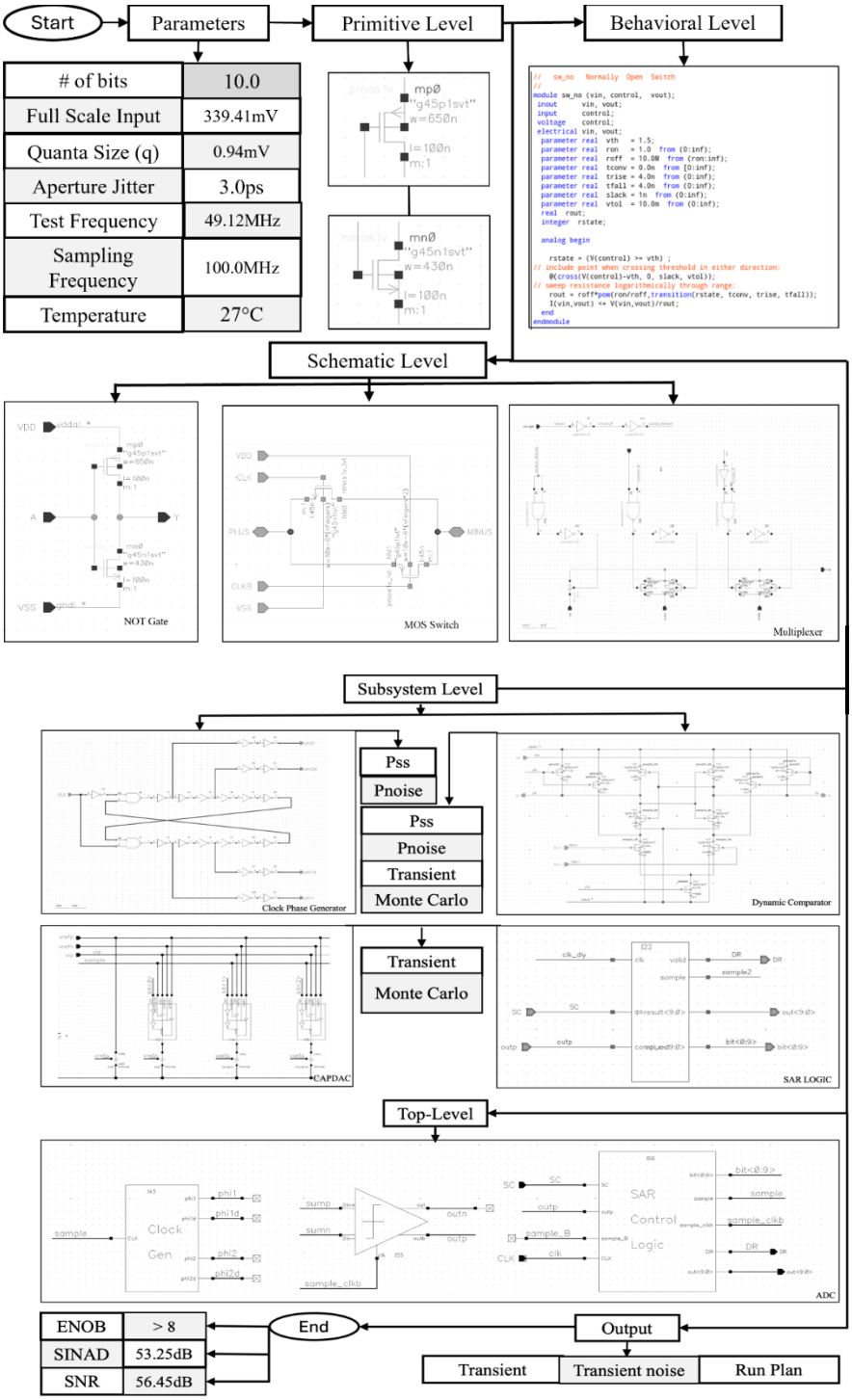


Fig. 2. Systematic design flow for the synchronous SAR ADC implementation.

3. DESIGN METHODOLOGY

Figure 2 illustrates the systematic design flow for the synchronous SAR ADC implementation using a hierarchical bottom-up methodology. The process begins with specification definition, establishing key parameters including 10-bit resolution, input voltage range, sampling frequency, and operating temperature.

At the primitive level, fundamental components (logic gates, multiplexers) are modeled using both structural netlists and behavioral scripts, capturing process variations and parasitic effects in 45 nm CMOS technology. The circuit level integrates these elements into functional

blocks, emphasizing critical timing components such as clock generators and latches, with transistor-level simulations validating timing relationships across process corners. Subsystem-level design implements key functional blocks including the clock phase generator, dynamic comparator, CDAC array, and SAR logic. Performance evaluation employs noise analysis and Monte Carlo simulations to assess PVT variations and yield characteristics.Top-level integration assembles validated subsystems into the complete ADC architecture with comprehensive testbench frameworks. The design flow concludes with performance metric extraction, including ENOB, SINAD, and SNR measurements, ensuring specification compliance and validating the design methodology effectiveness.

3.1. Top-Level SAR ADC Architecture

Figure 3 presents the complete SAR ADC system architecture, comprising four primary functional blocks: sample-and-hold circuit, dynamic comparator, capacitive DAC (CDAC) array, and SAR control logic. The CDAC array, occupying the right most section, interfaces directly with the analog input through binary-weighted capacitors. The centrally positioned comparator performs differential comparison between the CDAC output and sampled input voltage. The SAR logic orchestrates the successive approximation algorithm, controlling the bit-by-bit conversion sequence. Reference voltage distribution and control signal routing demonstrate the modular mixed-signal design approach essential for high-precision analog-to-digital conversion.

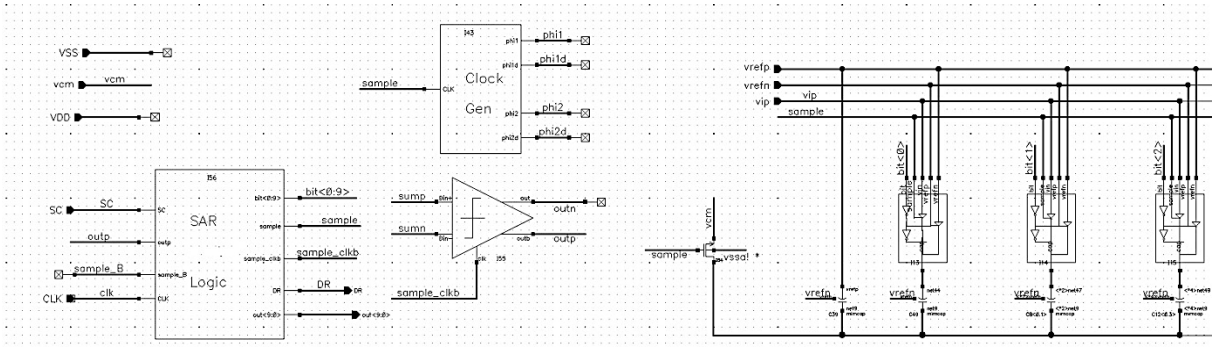


Fig. 3. Full schematic diagram of ADC.

3.2. Dynamic Comparator Design

The dynamic comparator circuit shown in Fig. 4 is optimized for high-speed SAR ADC applications. The design features differential inputs (Din+, Din−) with clock-controlled operation for precise timing synchronization. The core latch_buffer stage provides regenerative amplification during the active clock phase, rapidly resolving small input differentials to full-scale digital outputs. A subsequent SR latch (sr_latch_nand) maintains the comparison result until the next conversion cycle. This clocked architecture ensures low power consumption through reduced static current while delivering fast settling times critical for high-speed data conversion.

3.3. Capacitive DAC Implementation

Figure 5 illustrates the CDAC architecture, fundamental to SAR ADC operation. The design employs binary-weighted capacitor arrays with digitally controlled switches enabling selective connection to reference voltages or input signals. During successive approximation,

capacitors are sequentially switched according to the SAR algorithm, generating precise analog voltages corresponding to digital test codes. The charge redistribution mechanism ensures monotonic DAC characteristics essential for SAR ADC linearity. This capacitive approach provides good matching properties and scalability in advanced CMOS processes, enabling high-resolution conversion with minimal area overhead.

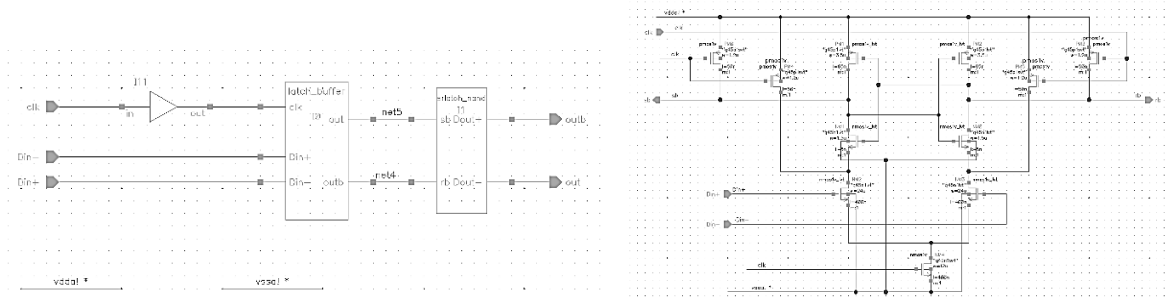


Fig. 4. Dynamic comparator schematic diagram a) top level; b) strong arm comparator.

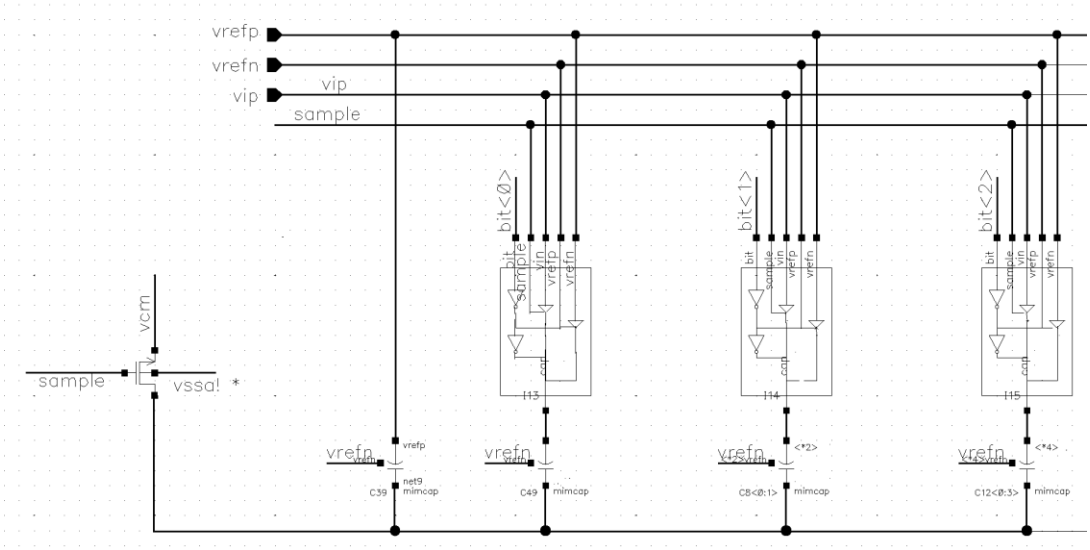


Fig. 5. CAPDAC schematic diagram.

3.4. Clock Phase Generator

Figure 6 presents the clock phase generator circuit that produces four phase-shifted outputs (ph1, ph2, ph3, ph4) from a single input clock (CLK). The design employs cascaded inverters, AND gates, and buffers to generate precisely timed non-overlapping clock phases through strategic signal delay and logical combination. This multi-phase clock generation is essential for synchronous SAR ADC operation, providing the temporal sequencing required for sample-and-hold operations, comparator timing, and CDAC switching control. The circuit ensures proper setup and hold times across all conversion phases while minimizing clock skew and power consumption.

3.5. SAR Control Logic

The SAR logic implementation shown in Fig. 7 coordinates the successive approximation algorithm through synchronized control signal generation. The design utilizes cascaded inverters for input clock conditioning and delay generation, producing the timing references

necessary for sequential bit resolution. Logic gates (AND, OR) process internal signals to generate critical control lines including sample and sample_clkb, ensuring precise timing coordination between sampling and conversion phases. The central SAR register processes comparator outputs sequentially, resolving individual bits of the digital conversion result. Signal conditioning circuitry guarantees accurate sampling signal timing for reliable analog input capture. This control architecture orchestrates the complete bit-by-bit conversion sequence, enabling high-speed and accurate analog-to-digital conversion.

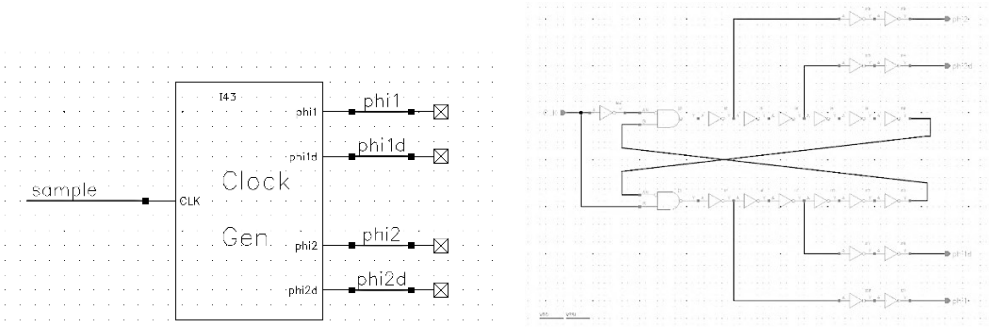


Fig. 6. Clock phase generator schematic diagram.

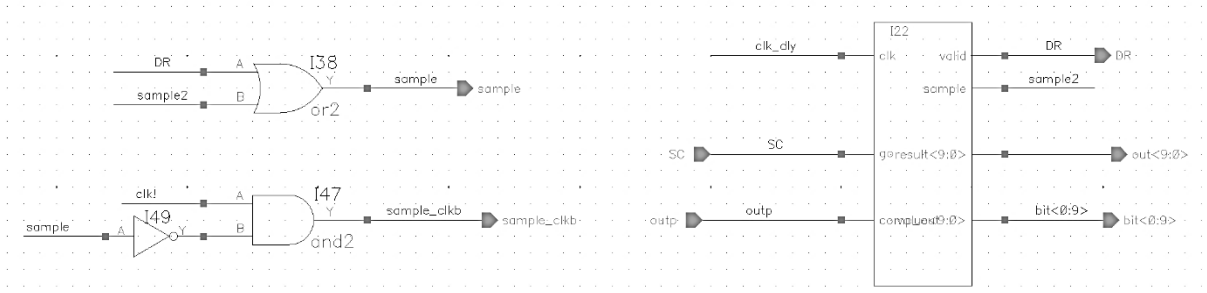


Fig. 7. Schematic diagram of SAR logic.

4. SIMULATION RESULTS AND ANALYSIS

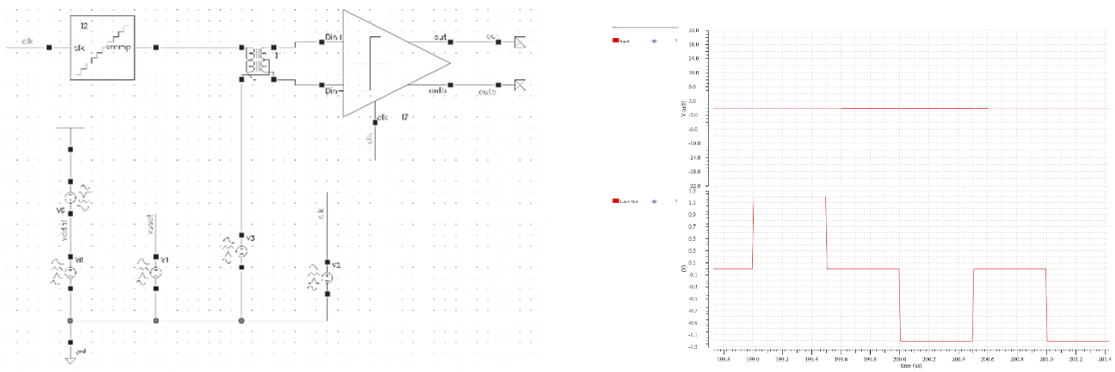
This section presents comprehensive performance characterization through noise analysis, mismatch evaluation, and key metrics including ENOB and SINAD, validating the proposed design methodology.

4.1. Latch Transient Response Analysis

Figure 8 demonstrates the dynamic comparator switching behavior, showing latch output and input signal waveforms during the critical transition from high to low logic states, confirming proper regenerative amplification and decision timing.

4.2. Clock Phase Generator Jitter Analysis

PSS and Pnoise simulations of the clock phase generator reveal excellent jitter performance with RMS jitter of 101 fs across 1 Hz to 50 MHz frequency range (Fig. 9). The consistent minimum and maximum jitter values indicate stable phase noise characteristics essential for maintaining sampling accuracy.



(a) (b)

Fig. 8. Dynamic comparator offset voltage characterization a) testbench; b) input and output of mixed-signal latch in transient analysis.

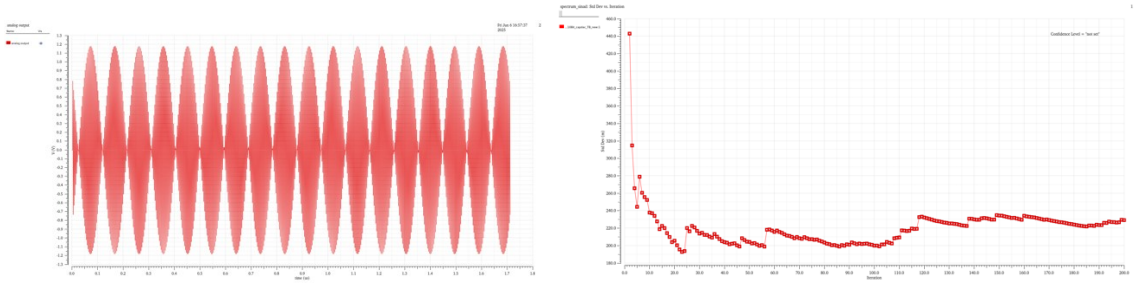
clockPhaseGenerator_TB_new | maestro

Name	Type	Details	Value
Jee[Second]:rms; pm0	expr	rf)itter(?result "pnoise_sample_pm0" ?unit "Second" ?from 1 ?to 50000000 ?signalLevel "rms")	101f
jitter[ps,rms]	expr	ymax(sqrt(iinteg((drpl)itter(?result "pnoise_sample_pm0" ?unit "Second" ?k 1 ?event 0)**2))))	101f
	expr	ymax(sqrt(iinteg((drpl)itter(?result "pnoise_sample_pm0" ?unit "Second" ?k 1 ?event 0)**2))))	101f

Fig. 9. Jitter noise of clock phase generator.

4.3. Capacitor Mismatch Monte Carlo Analysis

Monte Carlo analysis demonstrates SINAD standard deviation convergence after approximately 50 iterations (Fig. 10). The stabilization behavior confirms adequate statistical sampling for mismatch characterization, with the convergent trend validating the robustness of the CDAC array design against process variations.



(a) (b)

Fig. 10. CapDAC a) mismatch characterisation; b)sinad standard deviation versus iteration.

4.4. Performance Summary

Simulation results achieve ENOB of 9.86 bits and SINAD of 61.12 dB, approaching theoretical limits for 10-bit resolution. Monte Carlo analysis across 200 runs shows offset voltage variation < 2 mV and INL/DNL deviations < 0.5 LSB, meeting 10-bit ADC specifications with 2.6uW power consumption as shown in Fig. 11. Clock jitter remains < 0.5 ps RMS, ensuring minimal aperture uncertainty. Corner analysis validates robust performance across PVT variations, confirming design reliability for manufacturing implementation.

Table 2 compares the proposed ADC design with state-of-the-art implementations. Compared to [7], which operates at a lower sampling rate of 200 kHz, this work achieves higher speed with comparable power efficiency. While, authors in [6] shows a significantly higher power, making them less suitable for ultra-low-power applications. The proposed synchronous architecture with bootstrapped S/H and strong-arm comparator delivers an optimal balance

between speed, resolution, and power consumption, making it highly suitable for ultra-low-power mixed-signal applications in advanced 45nm CMOS technology.

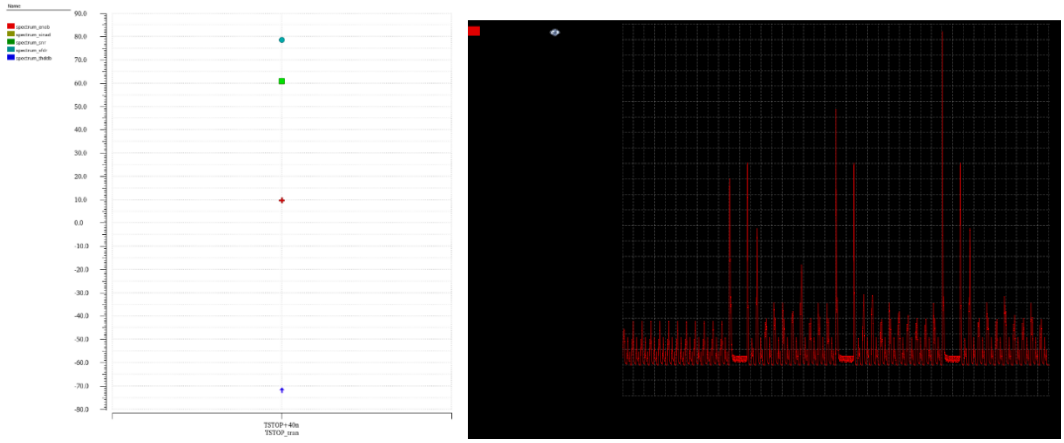


Fig. 11. Performance of the developed ADC.

Table 2. Comparison of proposed design with other designs.

Reference	CMOS Tech	VDD [V]	Sampling Rate [Hz]	Power [W]	ENOB [bits]	SINAD [dB]	Key Features
This work	45 nm	1.2	100 M	2.63 μ	9.86	61.12	Synchronous, bootstrapped S/H, strong-arm comparator
[7]	180 nm	1	200 k	4.45 μ	9.97	61.77	Energy-efficient CAP switching for wearable biosensors
[4]	90 nm	1.2	25 k	35.73 μ	8.84	65	Asynchronous SAR ADC for fast, low-power conversion
[6]	40 nm	0.9	70 M	2.50 m	7.75	48.52	Hybrid segmented DAC with reference buffer
[2]	180 nm	1.2	5 M	133 μ	8.08	50.4	Ultra-low power design for sensor applications

5. CONCLUSIONS

This work presents a 10-bit synchronous SAR ADC implemented in 45 nm CMOS technology, optimized for low-power mixed-signal applications. The architecture integrates a clock phase generator, bootstrapped switches, capacitive DAC, and StrongArm dynamic comparator to achieve high precision with minimal power consumption. The fully dynamic design eliminates static power dissipation, making it suitable for energy-constrained applications including IoT devices and biomedical systems. Comprehensive verification using Cadence Virtuoso tools, including transient analysis, Monte Carlo simulations, and noise characterization, successfully identified and quantified noise sources and mismatch effects. The achieved ENOB of 9.86 bits and SINAD of 61.12 dB at 100 MS/s sampling rate, while consuming only 2.63 µW at 1.2 V supply voltage demonstrate near-theoretical performance for 10-bit conversion, validating the design's linearity and signal integrity. The results confirm the viability of synchronous SAR ADCs for high-performance SoC integration, establishing a robust foundation for advanced low-power analog-to-digital conversion systems in next-generation mixed-signal applications.

Acknowledgement: The authors would like to thank their institution for the financial support of this article. the authors acknowledge the technical and financial support by the ministry of higher education, malaysia, under the research grant no. FRGS/1/2024/ICT02/UTEM/02/3 (FRGS/1/2024/FTKEK/F00566) and Universiti Teknikal Malaysia Melaka (UTeM).

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