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High-Efficiency Modified Soft Switching PFC Boost Converter and Interleaved Synchronous Rectifier for AC–DC Power Conversion

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***Abstract*—** This paper presents a novel low-ripple AC–DC conversion architecture for Electric Vehicle (EV) or industrial load applications, integrating a Modified Soft Switching Power Factor Correction (MSS-PFC) boost converter stage with high-frequency galvanic isolation and synchronous rectification. Front-end PFC circuit integrates a dual-loop control mechanism combining a hysteresis current control strategy with voltage and current PI controllers. This approach ensures accurate input current shaping, reduced Total Harmonic Distortion (THD), and near-unity power factors, while providing stable and ripple-free DC output ideal for load. The intermediate high-frequency inverter and isolation transformer enables compact design and safe voltage level adaptation, meeting safety and performance standards required in EV infrastructures. On the secondary side, an interleaved synchronous rectifier with closed-loop control minimizes switching losses and enhances energy transfer efficiency. The coordinated control structure ensures excellent dynamic response and robust output voltage regulation under varying input and load conditions, which are common in real-world EV charging scenarios. MATLAB simulation results validate that the proposed system achieves superior power quality, enhanced efficiency of 97.89%, and effective ripple suppression compared to conventional converter topologies.

***Keywords*—** AC–DC conversion architecture, MSS-PFC boost converter, Dual-loop control mechanism, EV charging.

1. INTRODUCTION

The use of electronic equipment in everyday life is rapidly expanding to meet both consumer and industrial demands. These devices rely on power supplies that draw energy from the utility grid. Typically, they incorporate one or more Switched-Mode Power Supplies (SMPS), which consume non-sinusoidal current [1]. This irregular current leads to distortions in both current and voltage, negatively impacting other devices connected to the same grid and reducing the overall efficiency of the power source [2]. To address these issues, new standards have been introduced to limit harmonic content of input currents. Manufacturers are now required to develop solutions that comply with these regulations. Most power supplies include AC/DC converter stages based on diode or thyristor rectifier circuits [2]. Traditionally, these stages feature a diode rectifier paired with an output capacitor, which significantly contributes to harmonic distortion in the mains supply. Diode rectifiers operating at line frequency convert AC to DC in an uncontrolled manner [3]. For low-power applications such as personal computers, televisions, and household appliances, single-phase diode rectifiers are preferred due to their simplicity and cost-effectiveness. In contrast, high-power systems like industrial machinery and motor drives utilize three-phase diode or thyristor

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rectifiers [4]. A standard offline SMPS typically includes a full-wave bridge rectifier with a large smoothing capacitor, an economical and straightforward solution for AC/DC conversion. However, this setup draws non-sinusoidal current from the grid [5].

In general practice, different load groups are distributed across various phases. When nonlinear loads are concentrated on one phase, it results in unbalanced currents flowing through the neutral line in a star configuration. These unbalanced currents lead to conductor heating, power losses, voltage distortion, and Electromagnetic Compatibility (EMC) issues [6]. Additionally, the harmonic content of these pulsating currents causes extra losses and dielectric stress in capacitors and cables, increases winding currents in motors and transformers, and generates noise in many devices. These effects lead to premature failure of fuses and other safety components and interfere with other equipment connected to the same grid [7].

To mitigate these harmonic disturbances, international standards such as IEC 61000-3-2 have been established. International Electro technical Commission (IEC) defines harmonic current limits for small single-phase and three-phase loads under 16 A per phase in its EMC guidelines. This standard outline circuit classifications and harmonic thresholds [8]. To meet these requirements, power supply manufacturers implement various strategies, collectively known as PFC techniques. The primary goal of PFC is to ensure that power supplies behave like resistive loads, thereby minimizing harmonic emissions. As energy consumption continues to rise, the demand for high-quality electrical energy supply has become increasingly stringent [9]. This necessitates the use of power electronic converters to transform input voltage into a precisely regulated DC voltage suitable for powering loads. Regulated DC power supplies are essential for the operation of most analog and digital electronic systems. Power supplies are typically designed to deliver regulated output, electrical isolation, and multiple output channels [10]. Most research in the area of PFC primarily targets the reduction of harmonic content in line currents. Passive PFC methods rely solely on passive components to reshape the input current waveform. However, a limitation of passive PFC is that it does not allow for control over the output voltage [11-12]. Various PFC based converter topologies are reviewed in Table 1.

The proposed high-efficiency modified soft switching PFC boost converter has various benefits over traditional low-voltage EV battery chargers.

- Enhanced efficiency through soft switching techniques
- Reduced thermal stress and conduction losses
- Simplified control architecture via DICM operation
- Lower component count and cost
- Improved power quality and compliance with PFC standards

These innovations position the modified boost converter as a promising solution for next-generation EV on-board charging systems.

The contributions of the proposed block diagram of a high-efficiency AC–DC power conversion system with soft switching and advanced control strategies.

- The AC source provides the main electrical energy input, starting the process of conversion with a sinusoidal voltage waveform.
- Source inductance conditions the input current and restricts inrush current, facilitating power factor correction and alleviating electromagnetic interference.

Table 1. Structured comparison of state-of-the-art PFC converter topologies.

Ref	Topology/ Application	Switching & Conduction mode	Key Advantages	Major Limitations	Gap related to proposed MSS-PFC
Hyeon-JoonKo*et al* (2023) [13]	Boost PFC,Model Predictive Current Control (MPCC) for EV chargers.	CCM, Hard switching, Variable frequency	Improved efficiency via reduced switching frequency near peak current.	No soft-switching (ZVS/ZCS absent), diode conduction losses remain high due to body diode operation.	MSS-PFC reduces both switching and conduction losses, lowers thermal stress without computationally intensive MPCC
Deliang Wu *et al* (2022) [14]	Isolated Bridgeless Active-Clamped SEPIC PFC	Bridge-less, CCM, ZVS for all HF MOSFETs, Soft diode turn-off	Eliminates diode bridge, reduced conduction loss, Active clamp enables ZVS, Inherent lossless snubbing for output diodes	Requires center-tapped transformer, Higher component count (transformer, clamp network).	MSS-PFC reduces control complexity, lowers cost.
Alzugure n et al. (2023) [15]	Floating Capacitor Integrated Dual Active Bridge (FCI-DAB) for single-phase, single-stage wireless EV battery charging	Resonant DAB, soft switching (ZVS over wide range), Duty-cycle-modulated PFC	Eliminates bulky electrolytic DC-bus capacitor. Active power decoupling at twice grid frequency.	Overall efficiency limited to ~93%. complex multi-bridge structure	MSS-PFC achieves higher efficiency (97.89%) with simpler boost-based structure.
Huang &Ruan, (2021) [16]	Two-stage single-phase PFC with SHCC (electrolytic-capacitor-less)	PFC stage as BVCC/BCCC with SHCC (BCCC)	Impedance-based stability analysis, removal of electrolytic capacitor using SHCC, virtual impedance stabilization	No soft-switching, Added control complexity	Proposed MSS-PFC achieves ZVS/ZCS with higher efficiency (97.89%), reduced switching stress.
Geethu Krishnan *et al* (2023) [17]	PFC-modified Zeta converter fed BLDC motor drive	DICM, hard switching, PWM-ON-PWM VSI control	Single voltage sensor, significant torque ripple reduction (34.2%), simple control	Hard-switched PFC stage, Limited to low–medium power BLDC applications	MSS-PFC targets front-end AC–DC efficiency enhancement.
Monireh Ghorbani an*et al* (2023) [18]	Bridgeless Buck-Boost PFC with ZVT auxiliary circuit	DCM, ZVS (main switches), ZCS (auxiliary & diodes)	Simple ZVT auxiliary circuit, Elimination of diode reverse recovery	Higher current stress, Limited power scalability.	Lower current stress due to boost operation, Simpler current shaping
Yu Qi *et al* (2021) [19]	Cascaded H-Bridge (CHB) Multilevel PFC with Mirror-Bridge Phase-Shift Modulation (MBPSM) for EV.	Multilevel CHB, phase-shift modulation, CCM	High power density, 40-dB CM noise reduction via modulation, EMI filter volume reduced >75%.	Multiple floating DC links, complex multilevel structure, increased boost inductor volume,	MSS-PFC achieves soft switching and near-unity PF using a single-stage boost topology with simpler control
Manish Kumar Dwivedi *et al* (2025) [20]	Dual-Switch Semi-Bridgeless SEPIC PFC (Battery charger)	DCM, inherent PFC	THD = 2.1–2.6%, reduced inductor size, no extra PFC control loop	Moderate efficiency (92.4%), hard switching, limited to low-power (100 W)	MSS-PFC achieves ZVS/ZCS, higher efficiency (97.89%), lower stress, scalable to higher power
Humam Al-Baidhani *et al* (2023) [21]	Bridgeless single-switch SEPIC PFC	DICM, hard switching, current-mode control.	PF≈0.99, <1% ripple, robust tracking, single switch, wide buck-boost operation	No soft switching, high peak current stress, switching loss not addressed, limited efficiency analysis	MSS-PFC introduces ZVS/ZCS soft switching, lower stress and higher efficiency (97.89%)

- Proposed soft switching PFC boost converter with modified topology effectively converts regulated DC from AC and achieves better efficiency by soft switching with a PF close to unity.
- High-frequency single-phase inverter transforms DC back into high-frequency AC, allowing for compact transformer design and efficient isolation.
- Sinusoidal Pulse Width Modulation (SPWM) regulates the inverter to produce a clean sinusoidal waveform with reduced harmonic distortion.
- Isolation transformer offers galvanic isolation and voltage transformation, which adds safety and compatibility with other load demands.
- Interleaved synchronous rectifier converts high-frequency AC back to DC with less conduction loss and ripple, which ensures high efficiency and stable output.

2. PROPOSED SYSTEM DESCRIPTION

The proposed high-efficiency modified soft switching PFC boost converter for AC–DC power conversion is displayed in Fig. 1, sums up an advanced power electronics system meant to maximize the conversion of AC to DC with zero energy loss and maximum control.

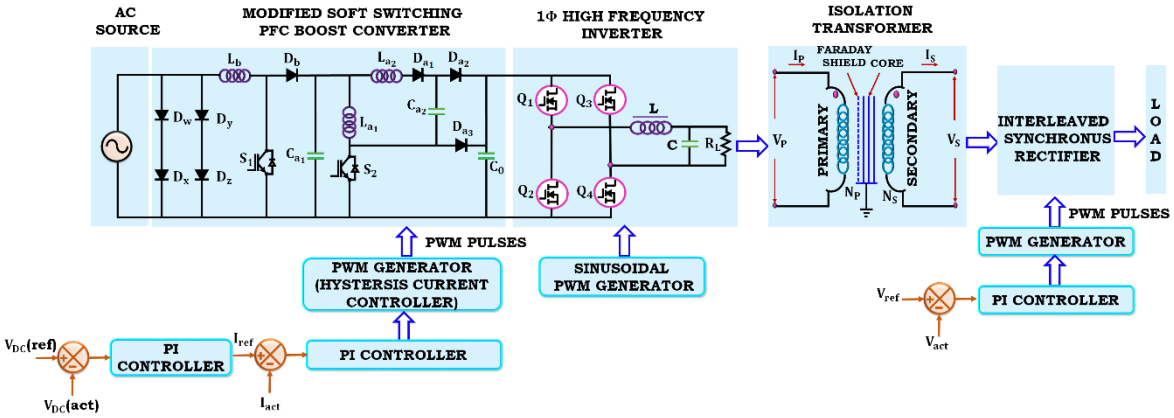

Fig. 1. Proposed high efficiency EV charging infrastructure.

AC source goes through a source inductance, a passive device that performs several functions. It restricts inrush current, removes high-frequency noise, and assists in shaping the input current waveform to enable PFC. After the source inductance, the AC signal flows into the core of the system, the modified soft switching PFC boost converter that effectively boosts input voltage to a higher DC level, and adjusts power factor so that AC source current drawn is in phase with the voltage, thus reducing reactive power and increasing system efficiency overall. Proposed boost converter control is taken care of by a PWM Generator using a Hysteresis Current Controller. The controller keeps the current inside a specified hysteresis band, responding quickly to load changes and providing accurate current regulation. A Proportional-Integral (PI) Controller sends this PWM Generator, comparing reference voltage $(V_{DC(ref)})$ with the actual DC voltage $(V_{DC(act)})$. PI Controller output is a reference current$(I_{DC(ref)})$, which directs the PWM Generator to control switching pulses in order to keep voltage level at its desired level. This closed-loop control keeps the DC output constant even with variations in input or load conditions. The converted DC, is supplied to single-phase high-frequency inverter, transforming DC to AC, driven by a SPWM generator, which controls the switching devices to yield a clean sinusoidal waveform. High-frequency AC output from

inverter is then directed through an isolation transformer, it offers galvanic isolation between input and output, and this improves safety and prevents sensitive loads from being damaged by electrical faults. The AC signal comes to the interleaved synchronous rectifier and gets converted back to DC, responsible for high efficiency in the output, is also driven by another PWM Generator to maintain accurate timing of the switching devices. The enhanced, power quality improved power is provided to load, offer a fast dynamic response, high accuracy, and disturbance resilience.

3. PROPOSED SYSTEM MODELLING

3.1. Modified Soft Switching PFC Boost Converter

From the AC source the input electrical energy is attained, which comprises of voltage fluctuations and harmonics, the source inductance is introduced that limits inrush current and suppress noises, plays a crucial role in energy conversion. Circuit configuration of proposed modified soft switching PFC boost converter is illustrated in Fig. 2. In this converter, V_s represents the AC supply voltage, and input rectification is performed using diodes D_w, D_x, D_y, D_z, forming a diode bridge rectifier. Rectified DC voltage is applied to converter stage, where $L_b$acts as the main boost inductor, and $D_b$serves as the boost diode. Switches S_1 and $S_2$are the active power IGBTs responsible for Pulse-Width Modulation (PWM) control and soft-switching operation. Capacitors C_{a_1} and C_{a_2}function as auxiliary snubber capacitors, while inductors L_{a_1} and L_{a_2}operate as auxiliary resonant inductors, providing soft-switching transitions for the main switches. Diodes D_{a_1}, D_{a_2} and D_{a_3}act as auxiliary resonant diodes that control energy transfer between the snubber network and the output.

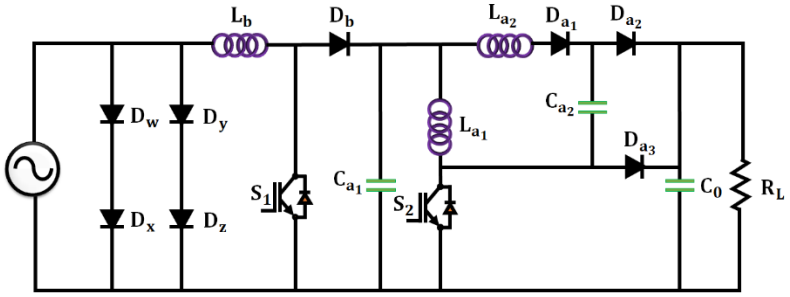

Fig. 2. Proposed MSS-PFC boost converter.

The output capacitor $C_0$is assumed to be sufficiently large to maintain a nearly constant output voltage V_0 across load resistor R_L, minimizing voltage ripple. Similarly, the boost inductor L_b is considered large enough to maintain nearly constant current during each switching cycle. During converter operation, soft-switching is achieved through the resonance among $L_{a_1}, L_{a_2}, C_{a_1}andC_{a_2}$. These resonant element soft switching Current Switching (ZCS) and Zero Voltage Switching (ZVS) conditions for S_1andS_2, respectively, effectively reducing switching losses and improving overall efficiency.

The converter operates in multiple modes, displayed in Fig. 3 throughout a switching cycle, determined by the conduction states of S_1andS_2, and the auxiliary diodes.

Mode 1 $(t_0 - t_2)$

At start of operation $(t = t_0)$, diode D_b conducts the input current from the boost inductorL_b. Both switchesS_1 and $S_2$are initially OFF.At$t = t_1$, switch S_2turns ON near Zero Current Switching (ZCS). The current $i_{L_{a2}}$in inductor increases due to resonance between

L_{a2}andC_{a2}, while the current through L_{a1} starts to increase linearly. The resonant capacitor C_{a1} charges during this interval.

The equations for this mode are written as follows:

$$L_{a1}\frac{di_{L_{a1}}}{dt} = V_0 \quad (1)$$

$$L_{a2}\frac{di_{L_{a2}}}{dt} = V_0 - v_{c_{a2}} \quad (2)$$

$$C_{a2}\frac{dv_{c_{a2}}}{dt} = I_i - i_{DB} - i_{L_{a1}} \quad (3)$$

Mode 2:

At $(t = t_2)$, diode D_b turns ON, initiating another resonant interval involving L_{a1}, L_{a2}andC_{a1}. The output capacitor $C_0$is large and therefore behaves as a constant voltage source, not participating in resonance. During this mode, C_{a2}begins to discharge, $i_{L_{a1}}$increases, $i_{L_{a1}}$decreases. Diode D_{a3}remains ON, transferring current from $L_{a2}$to the output stage through D_{a1}andD_{a2}.

$$L_{a2}\frac{di_{L_{a2}}}{dt} - L_{a1}\frac{di_{L_{a1}}}{dt} = -V_0 \quad (4)$$

$$I_i + C_{a1}\frac{dv_{c_{a1}}}{dt} = i_{L_{a1}} + i_{L_{a2}} \quad (5)$$

Mode 3:

At $(t = t_3)$, a new resonance occurs between L_{a1} and C_{a2} .The voltage across C_{a2} and current through L_{a1}remain to minimize and improve, respectively.

$$L_{a1}\frac{di_{L_{a1}}}{dt} = v_{c_{a1}} \quad (6)$$

$$C_{a1}\frac{dv_{c_{a1}}}{dt} = i_{L_{a1}} \quad (7)$$

Mode 4:

In this mode, stored energy in L_{a1} continues transferring to the output.

$$L_{a1}\frac{di_{L_{a1}}}{dt} = -V_0 \quad (8)$$

$$i_{S2} = I_i - i_{L_{a1}} \quad (9)$$

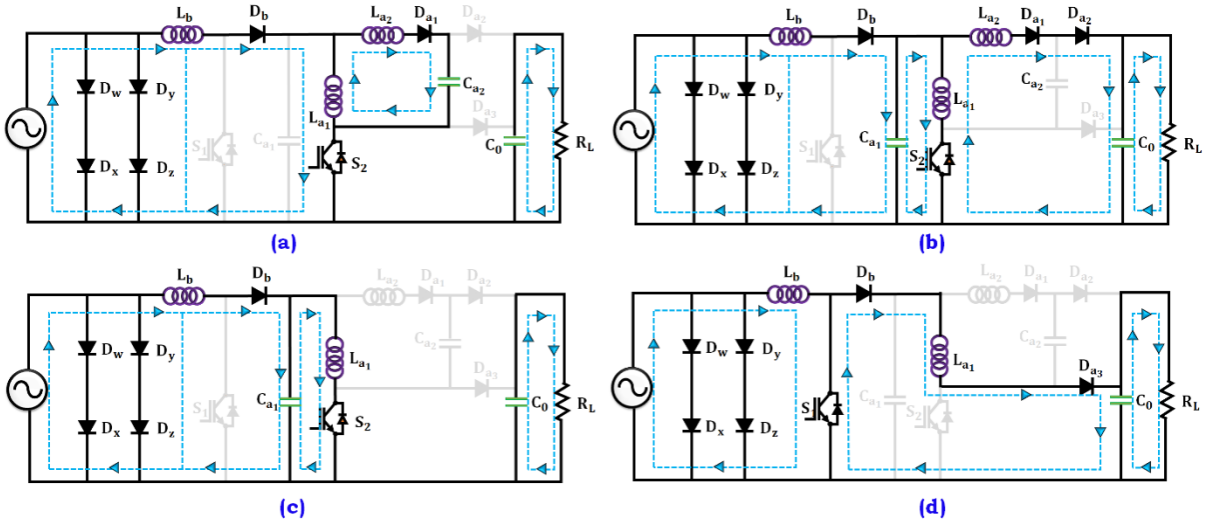

Fig. 3. Operating modes of MSS-PFC boost converter.

Conduction losses in rectifier diodes, conduction and core losses in boost inductor, conduction losses in boost IGBT and boost diode, make up total power losses in the proposed converter. Conduction loss in proposed PFC based boost inductor is given by:

$$P_{cond,L_b} = I^2_{LB\cdot RMS} \cdot R_{Lb} \quad (10)$$

Where, $I_{Lb\cdot RMS}$ is RMS current through inductor, R_{Lb} is internal resistance of boost inductor.

Turn-on switching loss is:

$$P_{Turn-onS} = \frac{V_0^2 t_{rTs} \cdot f_{sw}}{24 L_{a1}} \quad (11)$$

Turn-off switching loss is:

$$P_{Turn-offS} = \frac{I_0^2 t_{fTs} \cdot f_{sw}}{24 C_{a2}} \quad (12)$$

Figure 4 displays the switching waveform of the proposed MSS PFC boost converter, effectively shapes input current to follow sinusoidal voltage waveform, thereby achieving near-unity PF. The proposed configuration supports resonant transitions and energy recycling, enhancing efficiency across varying load conditions.

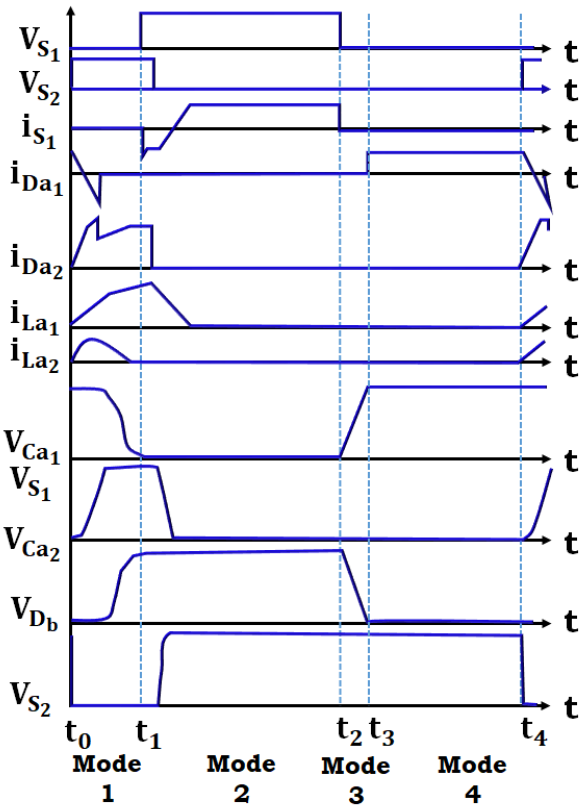

Fig. 4. Switching waveform.

3.2. Hysteresis Current Controller

MSS-PFC boost converter proposed here utilizes a dual-loop current-mode control architecture comprising an outer voltage control loop and an inner inductor current control loop. The choice of this design is aimed at meeting the three conditions concurrently i.e. tightly regulated output voltage, rapid dynamic response and almost unity PF even with wide variations in the input and load.

Outer Voltage Control Loop

The outer voltage loop is to control the DC- link output voltage at the desired reference level. The output voltage being fed back is scaled down by a feedback gain and then compared with the reference generating a voltage error:

$$e_0(t) = V_r - \beta v_o(t) \quad (13)$$

This error then gets processed by a PI controller, which is preferred because it performs:

This error signal is fed into a PI controller which is a good choice for the PI controller due to the following reasons:

- It eliminates steady-state voltage error by means of integral action.
- It increases transient response by proportional action.
- It keeps computational and implementation complexity at a low-level.

The PI controller's voltage output produces the inductor reference current $I_R$which is given by:

$$I_R(t) = K_P(V_r - \beta v_o(t)) + K_I \int (V_r - \beta v_o(t))dt \quad (14)$$

Here, proportional and integral gains are K_P and K_I respectively.

Design Justification:

The voltage loop is equipped with a small bandwidth, normally much less than the line frequency ($\sim 10 - 20\ Hz$), which ensures:

- The output voltage regulation does not cause the input current waveform to be distorted.
- The PFC function is mainly supported by the inner current loop.

The PI gains are first estimated using the Ziegler-Nichols method of tuning and then fine-tuned to give a good balance between fast voltage recovery and a small overshoot.

Inner Current Control Loop

The inner loop controls the boost inductor current directly, which is the main variable that accounts for power factor correction. In contrast to voltage-mode control, current-mode control offers:

- Faster dynamic response
- Improved input current shape
- A built-in over-current protection

The instantaneous boost inductor current $i_{L_b}$is detected and rectified to get its absolute value of$\left|i_{L_b}\right|$, thus the control action is the same for both AC half cycles. This signal is first scaled by a gain K and then compared to the reference current I_R.

The current-mode control law which results from this is:

$$u(t) = I_R(t) - K\left|i_{L_b}(t)\right| \quad (15)$$

Here, $u(t)$ is normalized duty control variable ($u(t) \in [0,1]$)

Design Justification:

Operating the converter through Discontinuous Inductor Current Mode (DICM) activity has these impacts:

1. The input current profile is naturally shaped in a manner proportional to the input voltage
2. Diode reverse-recovery losses are totally removed.
3. During turn-on events, ZCSis achieved

This method thus avoids right-half-plane zero commonly associated with CCM boost and SEPIC converters, which limits voltage-loop bandwidth and compromising transient response.

Hysteresis Current Controller (HCC) Implementation:

Continuous control signal $u(t)$ is being changed to switching pulses by the HCC and not by the regular fixed-frequency PWM modulator. The HCC looks at the actual inductor current and the reference current I_R within a given hysteresis band Δi.

Switching logic:

- Switch turns ON when $i_{L_b} < I_R - \Delta i$
- Switch turns OFF when $i_{L_b} > I_R + \Delta i$

Justification for HCC Selection:

- Offers great speed tracking of the load current and excellent dynamic performance.
- Provides natural handling of input voltage distortion and load transients.
- Gives precise current shaping without complicated compensators.
- Allow soft switching by controlling the current slope.

However, hysteresis control gives variable switching frequency, and this variation is tolerated in PFC front-end applications and negated by the proper design of resonant auxiliary parts.

Integration with Soft-Switching Network

The current-mode control method proposed in this paper interacts directly with the auxiliary resonant network(L_a, C_a)allows:

- Main switches get ZVS
- Auxiliary switches and diodes get Zero-Current Switching ZCS

The controller precisely regulates the inductor current pattern, thus ensuring that resonant transitions get anticipated, which results in lower switching losses and less electromagnetic stress.

The integrated PI-HCC control strategy is an ideal high efficiency PFC solution for EV and industrial applications, where power quality, efficiency and robustness become the critical factors.

3.3. Single Phase High Frequency Inverter

The enhanced DC power is applied to single phase high frequency inverter, Fig. 5, is an ideal sinusoidal RMS voltage source$V_{DC}$of controllable amplitude and phase, only constrained by its maximum output voltage $V_{max}$and currentI_{max}. That inverter is driving a load with complex impedance Z_L(which include both resistive and reactive components). In order to make analysis manageable consider the inverter supply any resistive/inductive load within voltage/current limits.

The Phasor relations are:

$$I_L = \frac{V_{DC}}{Z_L} \tag{16}$$

$$P_{out} = Re\{V_{DC} I_L^*\} \tag{17}$$

The inverter accepts the load's reactive component itself and its allowable range of operation at a specified power level is thus determined by:

- Voltage and current ratings of the inverter V_{max}, I_{max}
- Load impedance Z_L,
- Any further limits due to the switching topology (e.g., the need to ensure zero-voltage switching (ZVS) or other soft-switching requirements).

In practice, high-efficiency HF topologies are good at driving resistive or inductive loads but exhibit difficulties with capacitive loads. Single-inverter solution deal with capacitive or highly varying reactance's.

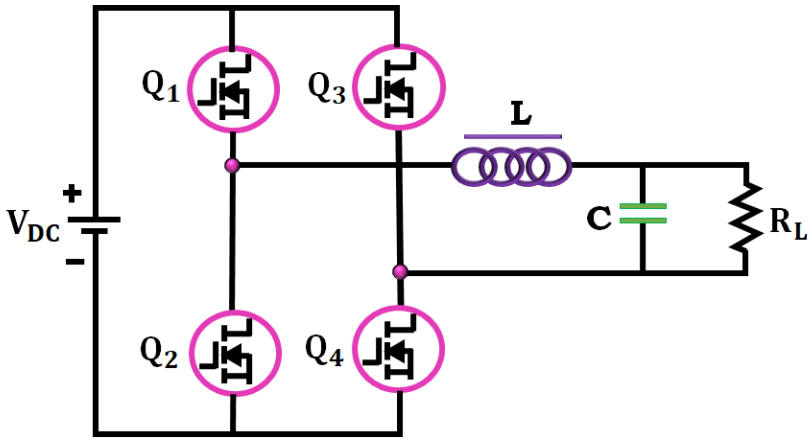

Fig. 5. Single-phase high frequency inverter.

3.4. SPWM

Pulse width modulation is a switching control method employed for modulation of the inverter output voltage and waveform profile. It works by producing constant-amplitude pulses whose width is varied in response to a control signal, thus modulating the duty cycle of the inverter switches. In an analog PWM control arrangement, a reference signal and a carrier signal are compared by a comparator. The logical output from the comparison decides the switching states of the inverter. The reference signal is the waveform that is wanted as the output. Carrier signal is typically high-frequency saw tooth or triangular waveform, at frequency much higher than reference.

The switching logic is such that:

If $V_{control} > V_{tri}$, T_{A^+} is ON, T_{A^-} is OFF

If $V_{control} < V_{tri}$, T_{A^-} is ON, T_{A^+} is OFF

This comparison means that the two switches are never ON together, and hence the output voltage is alternating between $+V_d/2$ and $-V_d/2$. Thus, the instantaneous output voltage at the inverter terminal is expressed as:

$$v_A = \begin{cases} +\frac{V_d}{2}, V_{control} > V_{tri} \\ -\frac{V_d}{2}, V_{control} < V_{tri} \end{cases} \quad (18)$$

The PWM technique to be employed is based on cost, noise performance, and efficiency of conversion. Of all the PWM strategies that exist, Sinusoidal Pulse Width Modulation (SPWM) is most commonly employed as it is simple to implement and produces high-quality AC waveforms.

SPWM

In the SPWM method, Fig. 6, more than one output pulse is produced in each half cycle, and the duration of each pulse changes proportionally with the instantaneous amplitude of a sinusoidal reference wave. Gating signals are derived by comparing a sinusoidal modulating signal against a high-frequency triangular carrier.

The RMS AC output voltage can be formulated in terms of the number of pulses (p)and the pulse width(δ).The resulting PWM waveform is very close to a sinusoidal voltage when it is transmitted through an LC filter, which attenuates higher-order harmonics.

SPWM generates much cleaner AC waveform in comparison to other PWM methods. Higher-order harmonics are still present, but the fundamental component is predominant, which makes SPWM extremely suitable for single-phase high-frequency inverters.

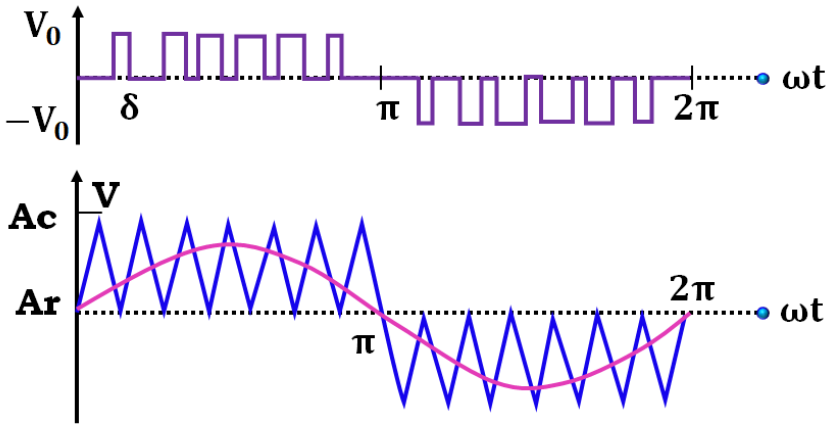

Fig. 6. Sinusoidal pulse width modulation.

Modulation Index and Over modulation:

Let the modulating signal be sinusoid of amplitude A_m, and the triangular carrier be of amplitude A_c. The Modulation Index (MI) is given by:

$$m = \frac{A_m}{A_c} \tag{19}$$

The modulation index itself controls directly amplitude of inverter output voltage. For (m< 1), the inverter is in the linear modulation region, whose output closely resembles the sinusoidal reference.

When (m>1), over modulation takes place, there are periods where the reference does not cut across the carrier waveform, leading to waveform distortion. Nevertheless, slight over modulation is occasionally accepted to rise the fundamental output voltage amplitude, though at the cost of higher harmonic content.

SPWM Harmonic Analysis and Elimination:

The SPWM waveform naturally has harmonics of different orders in its phase voltage. The most prominent harmonics are at orders of (n) and $n \pm 2$, with $n = \frac{f_c}{f_m}$ (carrier frequency divided by modulation frequency).

SPWM is the most efficient and reliable PWM control method for single-phase high-frequency inverters owing to the following benefits:

- Low power consumption and decreased switching stress
- High efficiency, generally up to 90% or greater
- Improved power handling capability
- Stable operation with little temperature drift or ageing effects
- Ease of implementation through digital controllers or microprocessors

Synchronization with Single-Phase High-Frequency Inverter Model

For single-phase HF inverter, the SPWM signal is used to switch the inverter bridge devices. The output from the comparator (reference and carrier signals) activates the inverter switches so that average value of output voltage waveform is equal to instantaneous amplitude of sinusoidal reference. On filtering, the output of the inverter produces a pure AC waveform ideal for use in high-frequency applications. Optimal selection of carrier frequency and modulation index provides a compromise between output quality, efficiency, and switching losses so that the inverter can run under its best performance under changing load conditions.

3.5. Interleaved Synchronous Rectifier

The interleaved synchronous rectifier employs several rectifier legs (phases) working in parallel with phase-shifted (interleaved) control, in order to minimize current ripple, share stress, and enhance thermal and efficiency performance. Each leg employs synchronous switches (not diodes) so the conduction losses are minimized and switching control is improved.

An isolation transformer (having primary and secondary windings), having a Faraday shield and core, Fig. 7. There are currents(I_S), voltages (V_S) on the secondary side, and on the primary side $(I_P), (V_P)$. This suggests the synchronous rectifier operates following a transformer stage in converting the high-frequency AC output to DC or another DC link.

Let the DC-link output voltage be V_{out}, each rectifier leg (k) (where $(k = 1 \dots N)$) produces a current$\left(i_{\{k\}(t)}\right)$. Since they are phase-shifted, the total current $I_{out}(t) = \sum_{k=1}^{N} i_k(t)$ has less ripple than a single leg. Average current per leg is considered as $\bar{I}_K = I_{out}/N$. Conduction loss per leg (approx.) $P_{cond,k} = R_{on,k} \cdot \bar{I}_k^2$ (in case of synchronism with on-resistance$R_{on,k}$. Switch timing is regulated in a way that each leg switches ON and OFF with a phase shift of (360°/N). The switching frequency (f_s) is the same across all legs, their gate signals are phase-shifted by (1/N) of the period. The interleaving enhances effective ripple frequency to $(N \cdot f_s)$ and minimizes ripple amplitude.

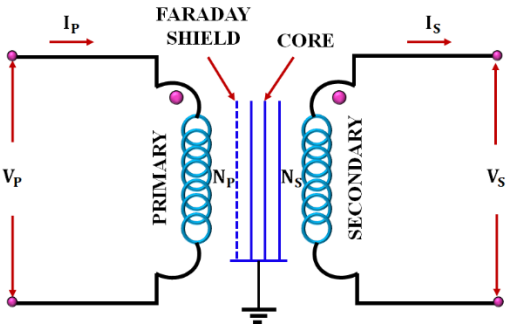

Fig. 7. Isolation transformer.

4. RESULT AND DISCUSSION

Proposed AC–DC conversion system is implemented in MATLAB/Simulink for attaining accurate modelling of control dynamics and power flow. The proposed structure performances verified with benchmark key parameters in comparison with some other works. Table. 2 summarizes the parameter specifications used in simulation and benchmarking.

Figure 8 presents input characteristics of a three-phase AC system. Plot (a) depicts the waveforms of a three-phase AC voltage, each sinusoidal with the amplitude is between $\pm 350V$, describes the symmetry of the waveform and the phase displacement of these waveforms, which further justify its balanced operation and sinusoidal integrity. Plot (b) is the three-phase AC waveforms, all sinusoidal and phase-shifted, with peak values at ±80 A, elaborates on the smoothness and alignment of current profiles, which essentially indicate effective load balancing and very minimal harmonic distortion, or power quality indicators. Plot (c) shows input AC voltage and current waveforms, both sinusoidal and in phase. Voltage ranges from $\pm 200V$, further support PFC successful implementation, ensuring that the front-end converter is able to shape the input current to a waveform similar to that of the voltage, thus ensuring minimal reactive power and greatly improving grid compliance.

Figure 9 represents the response of converter output voltage for a duration of 0.8 seconds. The voltage starts from 0 V and increases rapidly to reach approximately 310V, which ensures fast transient response and good voltage regulation of the converter. The waveform goes into a steady-state condition and maintains a constant output.

Table 2. Parameter specifications.

Parameter	Specifications
Three-phase AC source	
Source Voltage	$350V$
Source Current	$80A$
MSS PFC boost converter	
Inductor (L_{a_1}, L_{a_2}, L_b)	$4.7mH$
Capacitor (C_{a_1}, C_{a_2})	$22\mu F$
Capacitor (C_0)	$2200\mu F$
Switching Frequency	$10kHz$

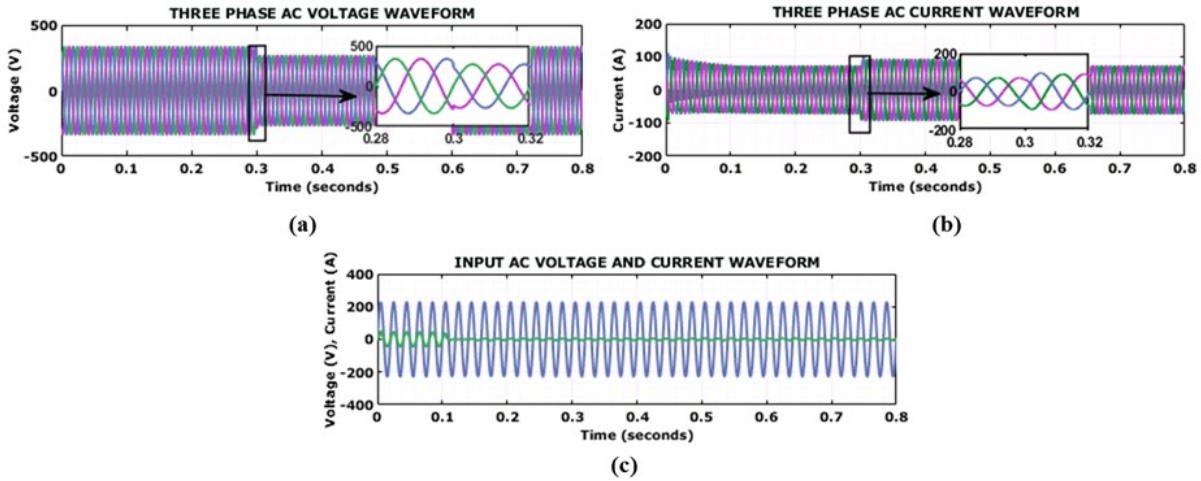

Fig. 8. Three-phase AC source.

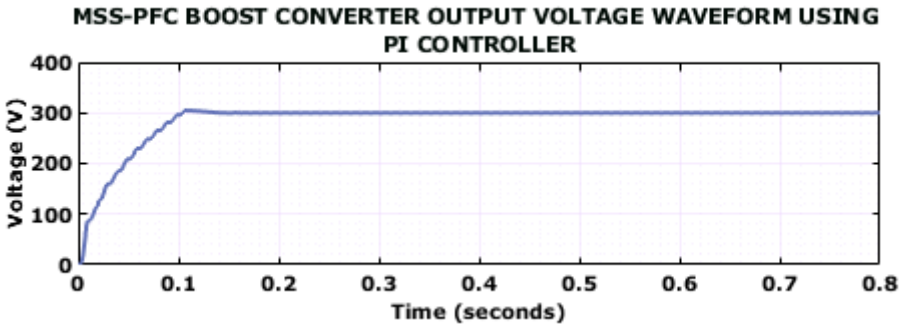

Fig. 9. Proposed MSS-PFC converter.

Figure 10 visualizes the transient and steady-state behaviour of real and reactive power in an AC–DC power conversion system. The waveform plot (a) is entitled real power waveform, has an initial sharp oscillation with a peak close to 4000 W within the first 0.1 sec, then quickly settles and stabilizes close to 500W. Plot (b), which is entitled reactive power waveform, shows a huge negative spike below –1000 VAR in the same initial period of time, followed by damped oscillations and then eventually stabilizing close to 0 VAR. Figure 11 displays the dynamic response of the power factor of the system during a period of 0.8

seconds. Initially, the power factor is about 1, then, at approximately 0.1 seconds, it suddenly drops, briefly around zero, this represents a transient disturbance, most likely due to sudden load change, or switching event. On the other hand, the waveform returns to unity power factor rapidly and then stabilizes, thereby assuring the effectiveness of control strategy regulated PFC boost converter of the restoration to and maintenance of ideal operating conditions. Figure 12 demonstrates waveform of output voltage for high-frequency inverter, it is settled to a steady-state high-frequency oscillation with amplitudes of ±350V. It confirms that the inverter passes its transient response and moves into steady-state operation, enabling it to provide symmetric AC output suitable for transformer coupling and isolation.

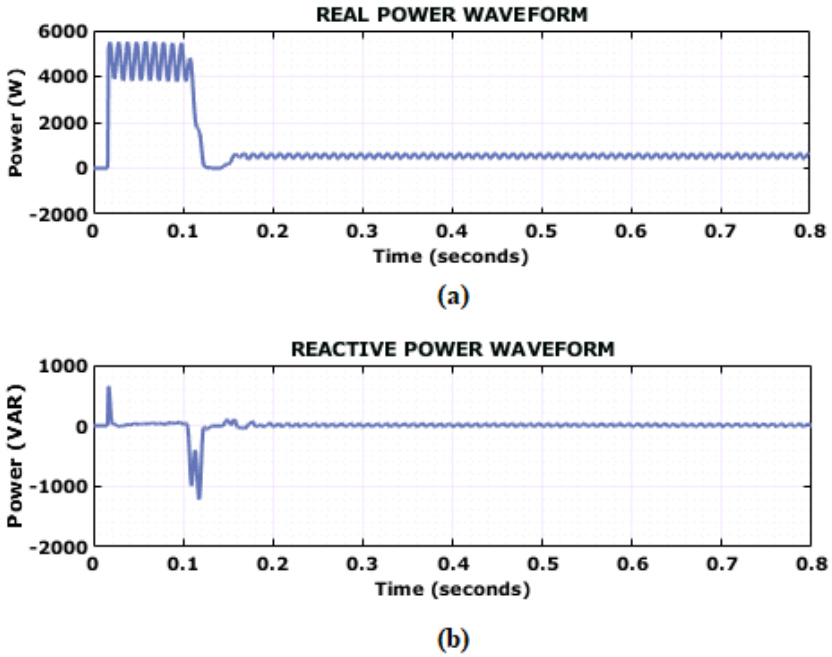

Fig. 10. Real and reactive power waveform.

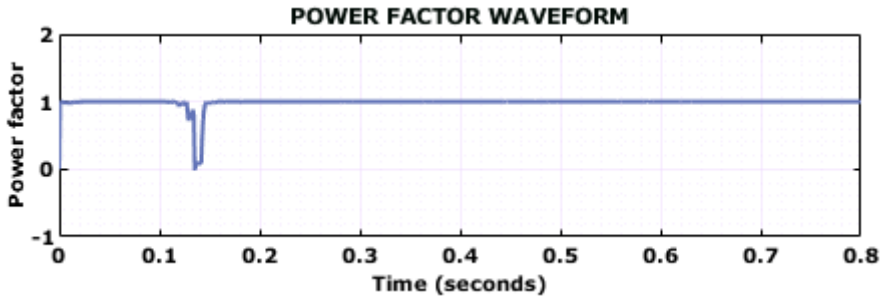

Fig. 11. PF waveform.

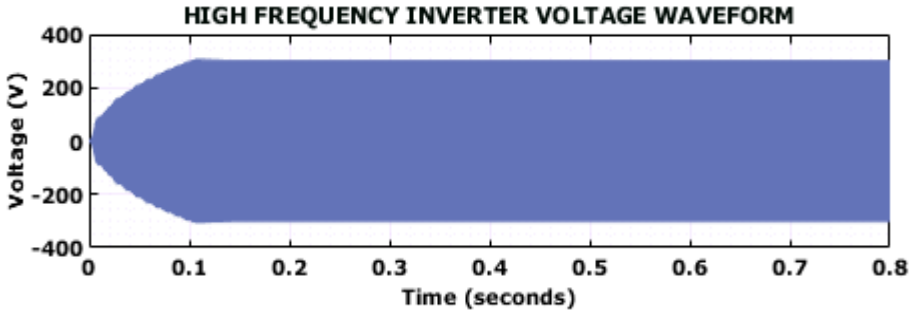

Fig. 12. High frequency inverter voltage waveform.

The high switching frequency increases the power density and decreases the filter size, which makes this inverter stage quite critical for any efficient DC–AC power conversion in an advanced power electronic system.

Figure 13 shows the output voltage waveform of the isolation transformer over a period of 0.8 seconds. From 0 to about 0.1 seconds, the waveform is sinusoidal, reflecting the high-frequency AC feeding into the transformer. The voltage in this condition remains within ±90 V, demonstrating effective isolation and voltage regulation.

Figure 14 gives dynamic output characteristics of interleaved synchronous rectifier system through four waveform plots. Plot (a) shows output voltage of Rectifier 1, which quickly ramps up to its steady-state value close to 80V, reflecting good voltage regulation without appreciable overshoot. Plot (b) gives the output current for Rectifier 1, and Plot (d) shows the output current for Rectifier 2 with a similar current ramp-up and steady-state value of about 2.5A, confirming proper current handling and load response. Plot (c) shows the output voltage of Rectifier 2, which similarly demonstrates a rapid rise and settles to the same steady-state value of approximately 80V as Rectifier 1, thus showing matched steady-state operation for the two interleaved phases.

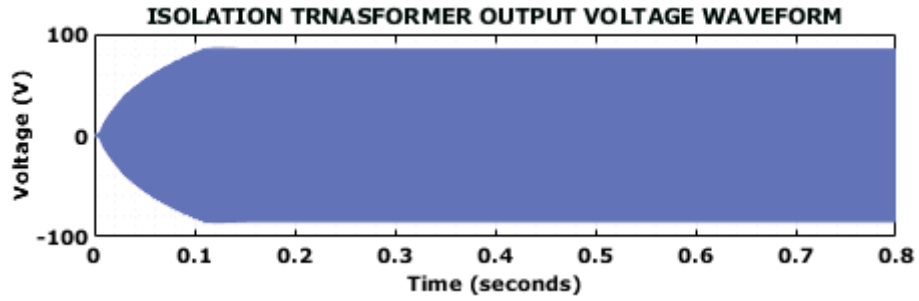

Fig. 13. Isolation transformer output voltage.

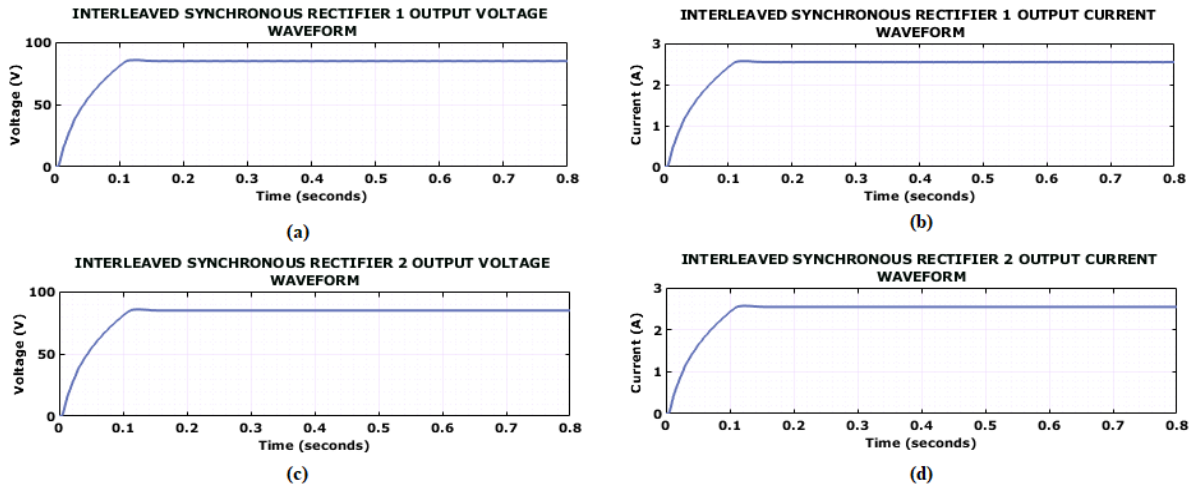

Fig. 14. Interleaved synchronous rectifier waveforms.

Figure 15 is DC output voltage of interleaved rectifier system, reaching around 180V and remaining stable, verifying effectiveness in boosting voltage and reducing ripple through interleaving. These waveforms confirm the capability of the system to provide high-efficiency, low-ripple DC output by synchronized multi-phase rectification. Figure 16 shows three bar graphs illustrating the harmonic spectrum and THD levels for electrical signals at a fundamental frequency of 50 Hz. The fundamental component in plot (a) has a magnitude of

72.86, with a THD of 1.16% at a moderate level. In plot (b), the signal is better, with a higher magnitude of the fundamental of 91.87 and a THD of 1.00%, which evidences better waveform purity. In plot (c), this is the clearest signal among the three, with a fundamental magnitude of 92.07 and the lowest THD of 0.97% maintain high power quality and follow harmonic standards for grid-connected applications.

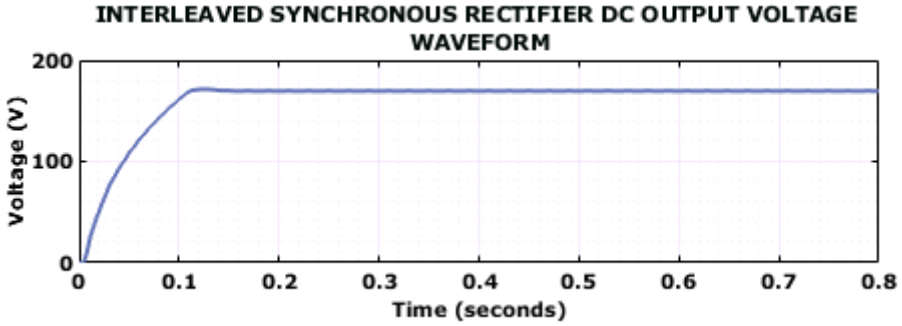

Fig. 15. Interleaved synchronous rectifier DC output voltage.

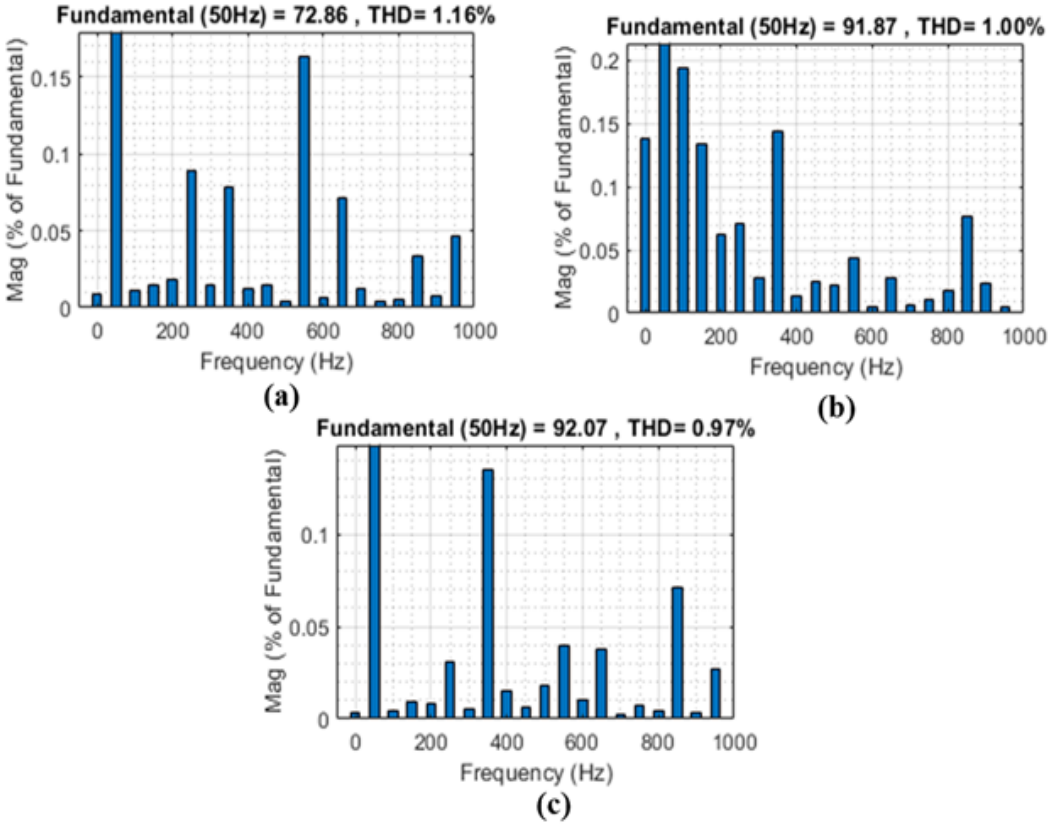

Fig. 16. THD waveforms.

Table 3 along with Fig. 17 reveal the performance of the proposed MSS-PFC boost converter under different load levels. When the load is increased from 20% to 100%, the total losses increase slightly as a result of both higher conduction and switching activity. However, the converter operates at a high efficiency level, reaching a maximum of 97.89% at about 40% load and staying almost unchanged afterwards. The main losses such as switch conduction, diode and inductor losses follow a normal pattern while auxiliary circuit losses are negligible. Hence, the converter is capable of delivering highly efficient, low, distortion power over a broad range of operating conditions.

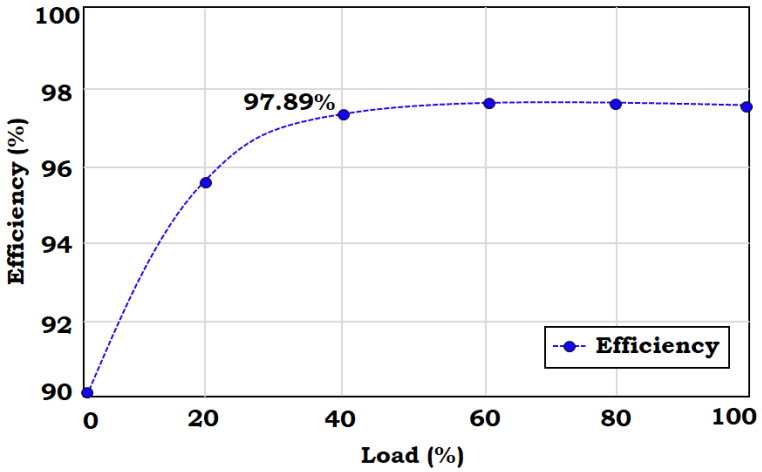

Fig. 17. Efficiency versus load characteristics.

Table. 3. Simulated loss breakdown of the proposed MSS-PFC boost converter.

Load Level (% Rated Power)	Output Power [W]	Switch Conduction Loss [W]	Switching Loss [W]	Diode Loss [W]	Inductor Copper & Core Loss [W]	Auxiliary Circuit Loss [W]	Total Loss [W]
20%	100	2.8	0.6	1.2	1.5	0.2	6.3
40%	200	4.9	0.9	2.1	2.6	0.3	10.8
60%	300	6.8	1.1	2.9	3.5	0.4	14.7
80%	400	8.7	1.4	3.6	4.4	0.5	18.6
100%	500	10.5	1.6	4.2	5.1	0.6	22.0

Figure 18 demonstrates the efficiency comparison graph, traditional PFC approaches demonstrate considerably lower efficiency, mostly at higher power levels, indicating their limited scalability and increased thermal stress. Proposed converter attained highest efficiency of 97.89% among the topologies discussed, strongly minimizing switching losses and conduction losses under different load conditions. Thus, the consistent efficiency gain throughout the operating range validates effectiveness of proposed soft-switching mechanism and the optimized control strategy, making it a potential solution for high-performance power factor correction in energy-sensitive applications.

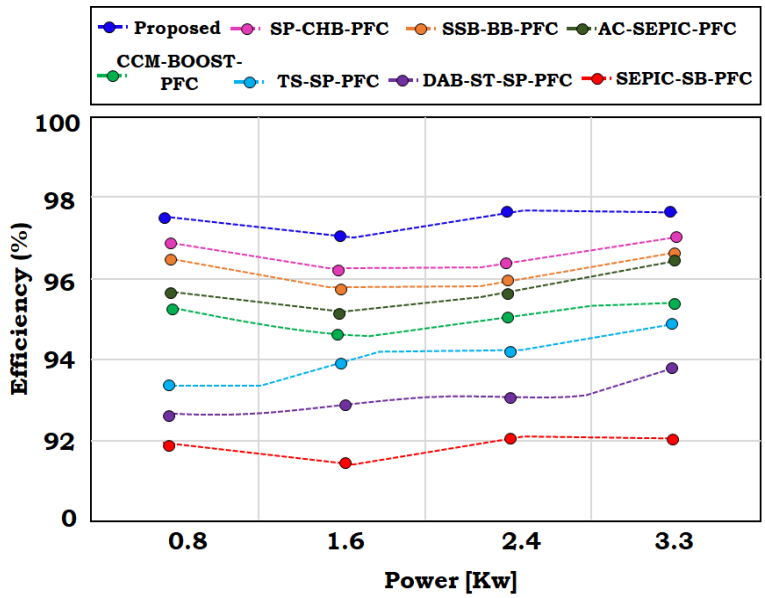

Fig. 18. Comparison of PFC converter efficiency.

Figure 19 illustrates the harmonic performance obtained for different PFC techniques such as Boost-PFC, AC-SEPIC-PFC, SSB-BB-PFC, SEPIC-SB-PFC, CCM-Boost PFChave higher THD, while the proposed approach yields the lowest THD throughout the operating range and maintains distortion at 0.97%. It shows better input current shaping, providing better grid compatibility, which considerably helps reduce electromagnetic interference and improves power quality.

Figure 20 shows the comparison graph of performance of the different PFC converter topologies at various loads from 0% to 100%. The proposed MSS-PFC boost converter maintains a PF close to unity throughout the load variations, reaching a peak value of unity PF at full load. This reflects that input current is almost in-phase with input voltage at this condition, minimizing reactive power and maximizing real power transfer.

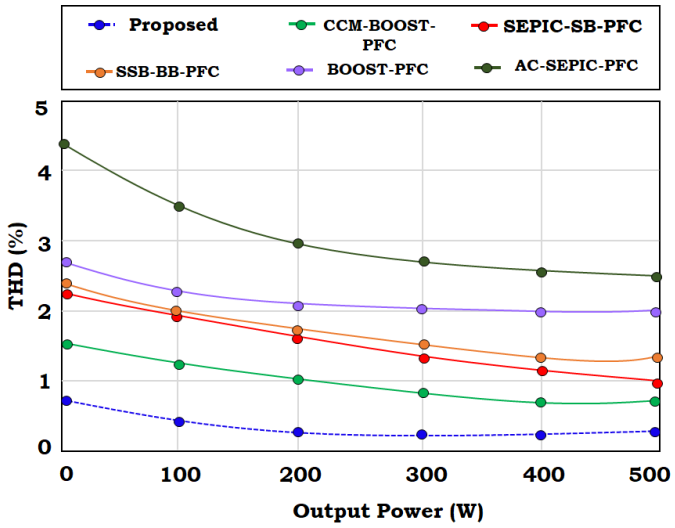

Fig. 19. THD comparison.

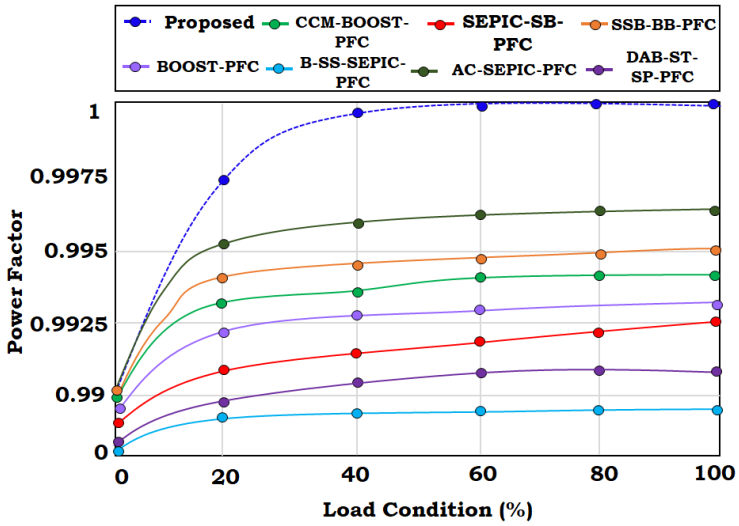

Fig. 20. PF comparative analysis.

5. CONCLUSIONS

The proposed AC–DC power conversion system, integrating a modified soft switching PFC boost converter and interleaved synchronous rectification, demonstrates robust

performance across all operational stages. The control architecture, enhanced by HCC-controlled approach, achieves unity power factor, ensuring ideal alignment between input voltage and current. The system delivers a conversion efficiency of 97.89%, reflecting minimal energy loss and high operational effectiveness. Harmonic analysis confirms a THD of 0.97%, validating excellent power quality and compliance with grid standards. Furthermore, the entire system is modelled and implemented in MATLAB/Simulink, enabling precise simulation of dynamic behaviour, control loops, and waveform fidelity. These results affirm the system's suitability for high-efficiency, low-distortion applications in smart grid and industrial energy systems. Even though this research only verifies the concept through simulations, the future research focuses on hardware prototype at a lower and scalable power level to experimentally implement the proposed MSS-PFC boost converter. It will cover Hardware-In-the-Loop (HIL) testing and laboratory measurements of efficiency, PF, THD, switching waveforms and thermal performance under real operating conditions. Experimental verification will be taken a step further to assess the feasibility of the proposed soft-switching mechanism, control robustness and EMI behavior, thus, making a bridge between the simulation and the real practice and thereby strengthening the application of the proposed technology for EV charging and industrial power conversion.

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