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Harmonics Mitigation and Reactive Power Compensation of Variable Speed Drive Using a Multi-Function Converter System with PI Controller Tuned by Horse Herd Optimization Technique

Omar H. Abdalla[1], Mohamed I. El Korfolly[2], Said Elmasry[3], Ibrahim Htita[4*]

[1, 2, 3, 4] Department of Electrical Power and Machines Engineering, Faculty of Engineering, Helwan University, Cairo, Egypt

E-mail: ibrahimhtita@h-eng.helwan.edu.eg

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***Abstract*—** This paper presents a proposed Horse Herd Optimization (HHO) technique for tuning a PI controller of a Multi-Function Converter (MFC) system. The MFC system consists of the converter and its associated controls. It is used to mitigate harmonic distortion caused by a Variable Speed Drive (VSD) operated in a modified Cigre benchmark 14-bus distribution network. Moreover, the MFC system is used to provide reactive power compensation for achieving unity power factor at the Point of Common Coupling (PCC). First, voltage and current harmonics at all buses are calculated in accordance with the IEEE Std. 519-2022 requirements. Five cases are considered for studying the harmonic distortion mitigation, using the MFC system: (i) no MFC system; (ii) installing an MFC system controlled by a hysteresis controller; (iii) installing an MFC system controlled by a fuzzy logic controller; (iv) installing an MFC system controlled by a PI controller tuned by Particle Swarm Optimization (PSO) method; and (v) installing an MFC system controlled by a PI controller tuned by the HHO method. Second, the reactive power compensation using the MFC system is investigated when switching an RL load at the VSD busbar for achieving unity power factor. Simulation studies are performed based on the MATLAB/Simulink software. The results have shown that the MFC system with the proposed HHO-tuned PI controller provides the most reduction in currents and voltages harmonic distortions compared to the other controllers. The Total Demand Distortion (TDD) of the current is reduced from 25% to 2.7% after installing the MFC system, which indicates a significant reduction of harmonics. Moreover, the MFC system proved to capable for providing the required reactive power to maintain unity power factor at the PCC, even if an additional RL load is added at the same bus.

***Keywords*—** Fuzzy logic control; Horse herd optimization; Hysteresis control; Multi-function converter system; PI controller; Reactive power compensation; Variable speed drive.

1. INTRODUCTION

Multi-Function Converter (MFC) systems can perform different functions according to its application, and each application requires definite structure. The purpose of the MFC system in [1] is for compensating harmonics and reactive powers. In this case, two converters are used for working as a shunt active filter or as AC-DC-AC converter. A three leg four wire converter is used with multi-functional namely power transfer to the grid and active power filter for nonlinear loads [2]. This MFC system is controlled by an adaptive hysteresis current controller. MFC systems in microgrids are not used only for interfacing the renewable energy sources into the grid, but also for compensating harmonics and reactive currents in the micro-grids [3]. Three legs converter is used in this case with L coupler for the interface with the microgrid. The

* Corresponding author
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voltage source converter connected in shunt with the AC system via a coupling transformer provides multi-functional topology including reactive power compensation, power factor correction, and currents harmonics mitigation [4]. A battery integrated modular MFC system for grid energy storage is presented in [5]. The modular MFC system consists of several modules in series and parallel for providing zero voltage switching, soft DC link voltage, and mitigating the three phase currents harmonics. A dual mode control of an MFC system is presented [6] in solar Photo Voltaic (PV) system for small off-grid applications. This MFC system is used in two modes, i.e., hybrid power flow, and the inverter mode for feeding the AC loads. A single stage multi-level MFC system for grid interactive PV system using cascaded two-level inverter [7]. This proposed MFC system tracks the maximum power produced by the PV array, compensates the reactive power, and mitigates the harmonics of nonlinear loads. A multi-functional parallel three-level four-leg converter system is proposed for harmonic current compensation, and circulating current mitigation [8]. A space vector modulation based on the non-axial redundant vectors is proposed for this MFC system.

Hysteresis controllers provide simple and robust control of the SAF. A hysteresis controller is used with four-leg Shunt Active Filter (SAF) photovoltaic grid connected system to improve for mitigating harmonics with the usage of Synchronous Reference Frame (SRF) theory [9]. A novel adaptive hysteresis controller is suggested in [10] for improving the performance of a shunt active filter in mitigating currents harmonics. Fuzzy logic control is considered as a popular control method used with the SAF. It provides efficient performance in harmonics mitigation without the need of knowing system parameters. It also provides robust control of the SAF, can handle system nonlinearities, and does not depend on mathematical models [11]. The Proportional Integral (PI) controller is widely used in the SAF. It is a simple, and robust controller when tuned properly. The power quality of a distribution system is improved by a SAF controlled by a robust backstepping controller with nonlinear observer [12].

A hybrid optimization algorithm based on a PSO, and a grey wolf optimization is suggested in [13] for tuning a fractional order PI controller for controlling the operation of a hybrid SAF. This PI controller shows good performance in terms of harmonics mitigation and reactive power compensation for balanced and unbalanced loading conditions. An adaptive PI controller is suggested in [14] based on an Ant Colony Optimization (ACO) algorithm for SAF control. The ACO shows better performance than genetic algorithm and eagle perching optimization techniques. A Cuckoo controller is suggested in [15], and its performance is compared with a PI controller and a fuzzy logic controller. The Cuckoo controller gives better performance than the conventional PI controller and the fuzzy logic controller. A SAF controlled by a sliding mode controller is used to mitigate harmonics [16], the sliding mode controller is tuned by an improved reptile search algorithm.

The previous research works have proposed applications of MFC systems and its structures. The functions of each application are discussed. Moreover, different controller types of MFC systems are introduced. Although hysteresis controller is simple, the efficient operation of this controller requires small hysteresis bands, high switching frequencies which increase the switching losses. The fuzzy logic controller provides robust control and does not need detailed mathematical model, but building rule tables is a complex process that depending on human expertise. Despite the above studies, more efficient tuning methods of the PI controller of MFC

systems are still needed for providing better system performance by mitigating harmonics due to the increasing usage of Variable Speed Drives (VSDs).

This paper presents an innovative tuning method of the PI controller based on a Horse Herd Optimization (HHO) technique for mitigating harmonics generated by VSDs, and compensating the reactive power at bus 4 for achieving unity power factor. Beside the Total Demand Distortion (TDD) of currents, the Total Harmonic Distortion (THD) of voltages are studied with the proposed tuning method. The performance of the MFC system with the proposed tuning method is compared with hysteresis, fuzzy, and PSO-tuned PI controllers. Harmonics analyses of voltages and currents are performed according to the IEEE Std. 519-2022 [17] in the cases employing the MFC system and in the case of no MFC system.

The rest of the paper is organized as follows. Section 2 presents the simulation model of the Cigre benchmark distribution network, the VSD, and the applied MFC system. Section 3 explains the HHO technique. Section 4 presents the different applied controllers considered in this paper. Section 5 presents the simulation results in case of a hysteresis controller, a fuzzy logic controller, a PSO-tuned PI controller, and an HHO-tuned PI controller for mitigating the currents harmonics, and compensating the reactive power at bus 4. Section 6 summarizes the main conclusions.

2. SYSTEM DESCRIPTION

2.1. Cigre Benchmark Distribution Network

The studied system is a modified 14-buses Cigre benchmark distribution system [18]. It is modified by connecting a VSD at bus 4. The other buses of the benchmark supply linear loads. Fig. 1 shows the studied distribution system [19]. Fig. 2 illustrates the block diagram of the VSD system [19]. The VSD consists of power electronic devices and a speed controller adjusting the motor speed at the desired reference value.

The VSD is considered as a highly distorting nonlinear load. It comprises a diode bridge and an inverter which contains semiconductor switches causing distortions in the supply current. The inverter gate signals are obtained from the space vector modulator controlled by a speed controller. The nominal power of the motor studied here is 1400 kW, and its nominal speed is 1480 rpm.

2.2. MFC System

Fig. 3 shows the MFC system structure. The objectives of the MFC system are mitigating current harmonics generated by the VSD connected at bus 4, and compensating the reactive power at bus 4 for obtaining a unity power factor. The MFC system injects harmonic currents in opposite direction to the nonlinear load harmonic currents for obtaining a pure sinusoidal current drawn from the supply and unity power factor. The MFC system includes the converter, and its associated control systems. The control systems include the control system for extracting the required reference current (SRF), and the current control system. The control systems details are presented in section 4.2. The MFC system controller generates the converter gate signals for achieving harmonics mitigation, and compensating the reactive power at bus 4. The DC link storage capacitor of the MFC system smooths the DC link voltage. The MFC system is connected to the Point of Common Coupling (PCC) through an inductor. This

inductor is used to mitigate harmonics generated due to the switching action of the converter, and smooths the MFC system currents.

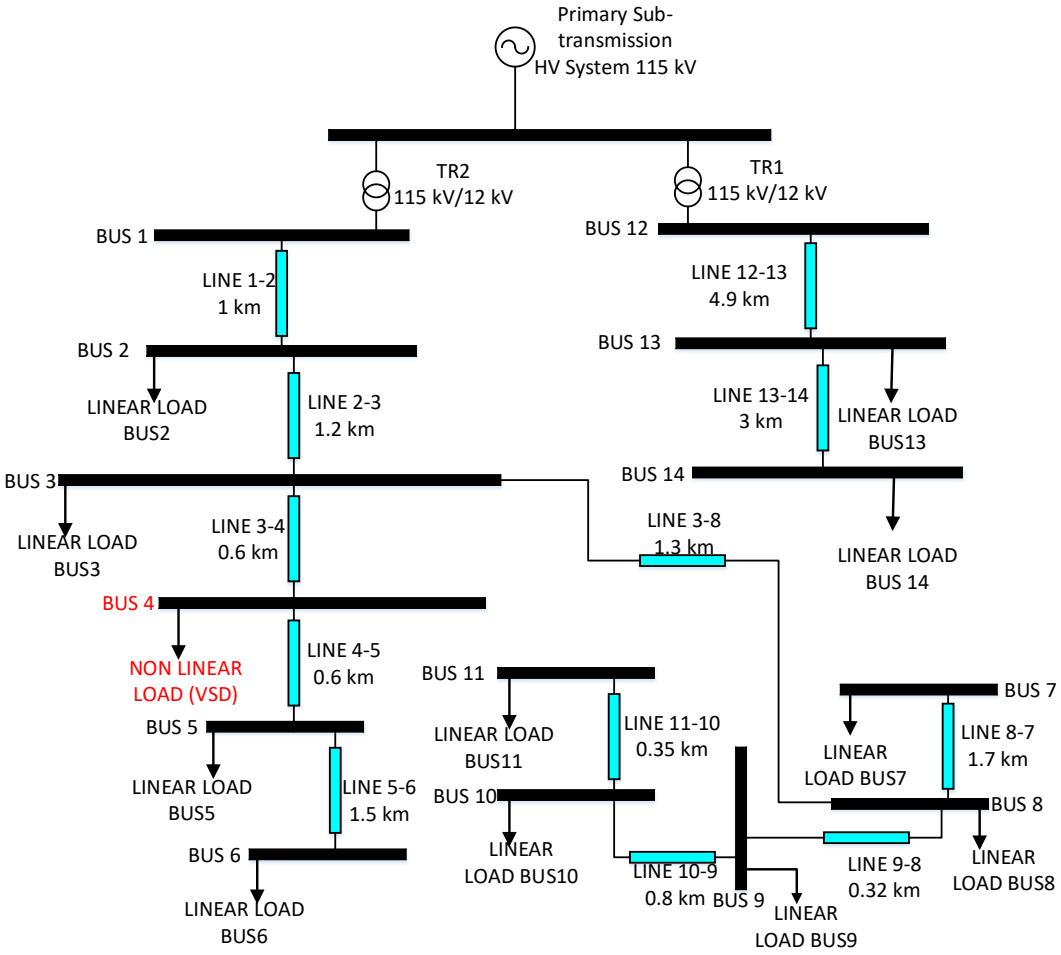

Fig. 1. 14-bus modified Cigre benchmark with VSD at bus 4.

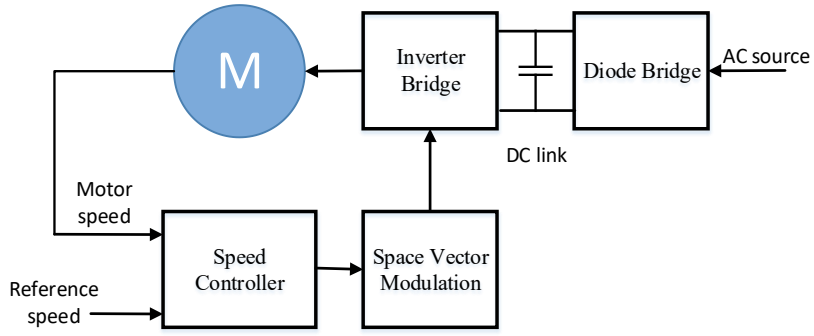

Fig. 2. Block diagram of VSD system.

The required DC link voltage is calculated as follows [19]:

$$V_{DC} = \frac{2\sqrt{2}\,V_{LL}}{\sqrt{3}\,m} \quad (1)$$

where V_{LL} is the line-to-line voltage, and m is the modulation depth and is taken to be 1. For V_{LL}equals 11.5 kV at bus 4 and m equals 1, the value of V_{DC} is,

$$V_{DC} = \frac{2\sqrt{2} \times 11500}{\sqrt{3} \times 1} = 18.77\ kV$$

The DC link capacitance value is expressed as follows [20]:

$$C_{DC} = \frac{3 \times K \times a \times V_{ph} \times I_{sh} \times t}{0.5 \times \left({V_{DC}}^2 - {V_{DC1}}^2\right)} \quad (2)$$

where K is a factor considering the energy variation during dynamics, V_{ph} is the phase voltage, I_{sh} is the phase current of the MFC system, a is an overloading factor, t is the minimum time required for reaching a steady-state value after a disturbance, V_{DC1} is the lowest required value of the DC bus voltage. For K = 0.1, a = 1.2, I_{sh} = 100 A, V_{ph} = 6.64 kV (11.5/$\sqrt{3}$), t = 20 ms, V_{DC} = 18.77 kV, and V_{DC1} = 18 kV. The value of C_{DC} is calculated as:

$$C_{DC} = \frac{3 \times 0.1 \times 1.2 \times 6640 \times 100 \times 0.02}{0.5 \times (18770^2 - 18000^2)} = 0.337\ mF$$

The interfacing inductance is calculated as follows [20]:

$$L = \frac{\sqrt{3} \times m \times V_{DC}}{12 \times a \times f_{sh} \times I_{r,pp}} \quad (3)$$

where f_{sh} is the switching frequency (20 kHz), and $I_{r,pp}$ is the peak-to-peak value of the ripple current which is taken 10% of the shunt compensator phase current (10 A).

then, $L = \frac{\sqrt{3} \times 1 \times 18770}{12 \times 1.2 \times 20000 \times 10} = 11.28\ mH.$

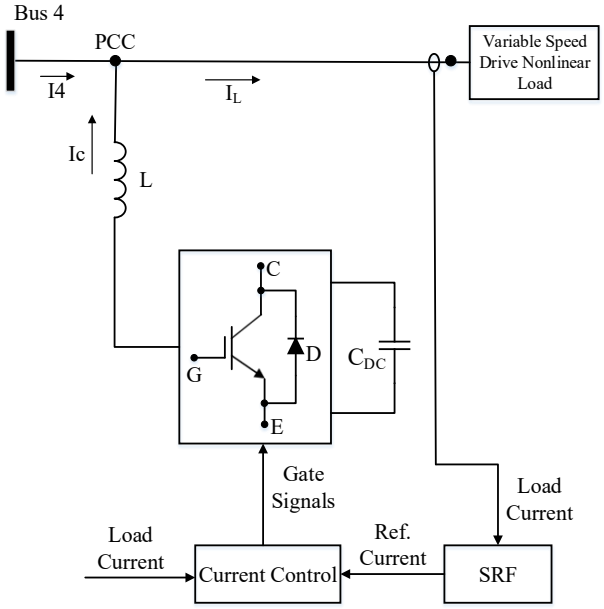

Fig. 3. MFC system structure.

3. HHO METHOD

The HHO is one of the most accurate and simple optimization algorithms, and it has several advantages include [21]:

- It is easy to use.
- Few parameters' settings are needed.
- No requirement for derivative information in the initial search.
- It is a flexible optimization method.
- It is a very fast optimization method.

This optimization method is inspired by the natural habitat of horses. This optimization method is based on 6 characteristics of the horse at different ages [22] include Grazing (G), Hierarchy (H), Socialization (S), Imitating (I), Defensing (D), and Roaming (R). At each iteration, the horses move according to the following equation [22]:

$$X_m^{Iter,AGE} = \vec{V}_m^{Iter,AGE} + X_m^{(Iter-1),AGE} \quad (4)$$

where, $AGE = \alpha, \beta, \gamma, \delta$, $X_m^{Iter,AGE}$ refers to the position of m^{th} horse, AGE indicates the horse's age range.

$Iter$ is the present iteration number.
$\vec{V}_m^{\,Iter,AGE}$ is the velocity vector of the horse.

As the lifespan of horses is approximately from 25 years to 30 years, δ represents the horses of age from 0 to 5 years, γ represents the horses of age from 5 to 10 years. β represents the horses of age from 10 to 15 years, and α represents the horses of age more than 15 years old. Fig. 4 shows the flow chart of the HHO algorithm [23]. At each iteration, the motion vectors of each horse at the different age levels are expressed as follows [22]:

$$V_m^{\,Iter,\alpha} = \vec{G}_m^{\,Iter,\alpha} + D_m^{\,Iter,\alpha} \quad (5)$$

$$V_m^{\,Iter,\beta} = \vec{G}_m^{\,Iter,\beta} + H_m^{\,Iter,\beta} + S_m^{\,Iter,\beta} + D_m^{\,Iter,\beta} \quad (6)$$

$$V_m^{\,Iter,\gamma} = \vec{G}_m^{\,Iter,\gamma} + H_m^{\,Iter,\gamma} + S_m^{\,Iter,\gamma} + I_m^{\,Iter,\gamma} + D_m^{\,Iter,\gamma} + R_m^{\,Iter,\gamma} \quad (7)$$

$$V_m^{\,Iter,\delta} = \vec{G}_m^{\,Iter,\delta} + I_m^{\,Iter,\delta} + R_m^{\,Iter,\delta} \quad (8)$$

Additional details are given in the Appendix.

4. MFC CONTROL SYSTEM

The MFC control system consists of two main stages, the first stage is the generation of the reference current for the current controller, while the second stage is the generation of the required gate signals based on the obtained reference current. After obtaining the reference current, the inner loop controller produces gate signals. The PI controller is first studied and tuned by the HHO method. To verify the improved performance of the proposed HHO-tuned PI controller, it is compared with the following controllers: a PSO-tuned PI controller, a hysteresis controller, and a fuzzy-logic controller.

4.1. Reference Current Generation

The generation of reference current is performed by the SRF theory. Fig. 5 shows the block diagram of this technique. The reference voltage of the DC link is compared with the actual voltage, and the PI controller is used for maintaining the DC link voltage value at its reference value. The required current for maintaining the DC voltage at its reference value is called the compensation current (Icomp). The actual load current in the abc sequence is converted to the d-q components and the d-component passes through a low pass filter for mitigating current harmonics. The compensation current is added to the filtered d-component current for obtaining the required reference current.

4.2. PI-HHO Tuning Method

The HHO method is applied for tuning the PI controller, which controls the operation of the MFC system. Fig. 6 shows the block diagram of the PI controller. Two PI controllers are employed for generating the reference voltage required for the PWM modulator in the d-axis and q-axis. The reference voltage is generated by comparing the reference current with the actual current and the output error is processed by the PI controller for generating the reference voltages in the d-axis and q-axis. The reference voltage in the dq frame is converted to the abc sequence by knowing θ which is obtained from the PLL block. In the HHO method, a horse herd consists of 25 horses in the age range β is selected. The optimization technique changes the controller gains for minimizing the objective function, which is the error between the

reference current and the actual current. The acceptable tolerance between two consecutive iterations is assumed to be 0.001 and the optimization process is stopped when reaching this tolerance. In this case, the value of *Kp* in the d-direction is 1812 and the value of *Ki* is 2245. The value of *Kp* in the q-direction is 831.5 and the value of *Ki* is 533.6. The value of the scaling factor in d-direction is 82, while the value of the scaling factor in q-direction is 21.

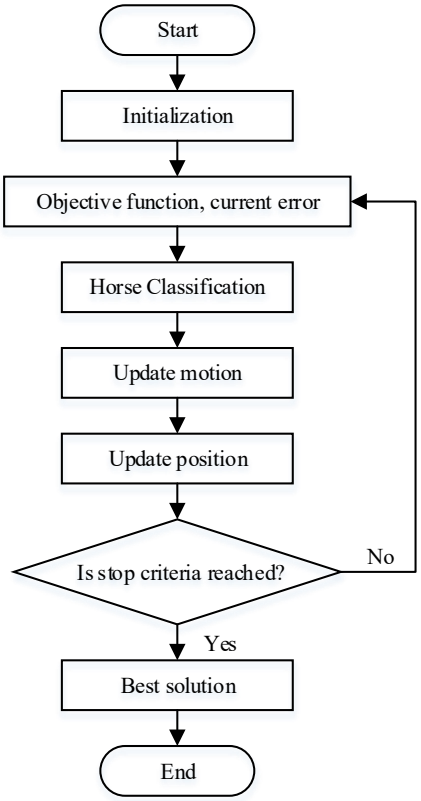

Fig. 4. HHO method flowchart.

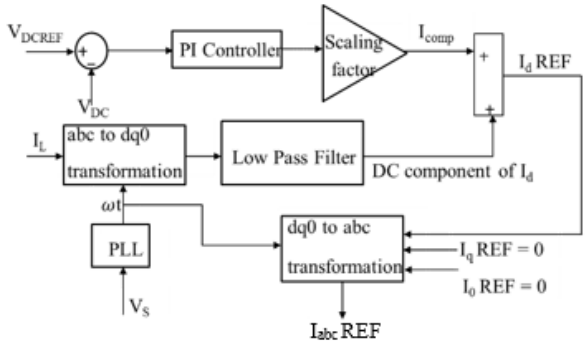

Fig. 5. SRF algorithm for extracting reference current.

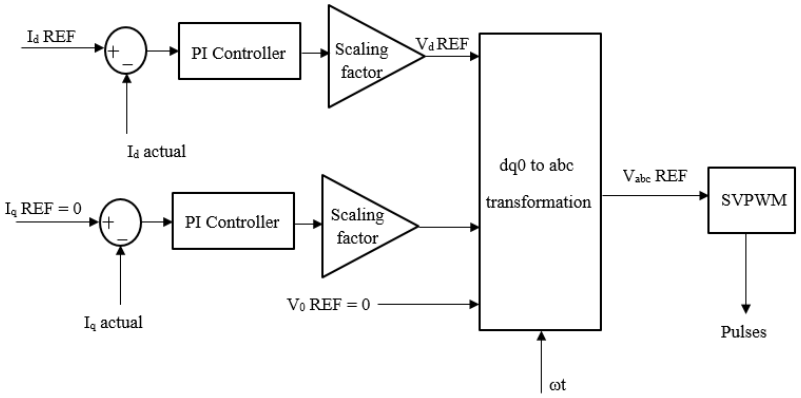

Fig. 6. PI current control block diagram.

4.3. PSO Method

The gains of the PI controller can be obtained by using the PSO technique. The cost function of the optimization technique is the error between the reference and actual currents in dq frame. The swarm size is 25 and the optimization technique changes the controller gains for minimizing the cost function for reaching the allowed tolerance of 0.001. The value of *Kp* in d-direction is 1809 and the value of *Ki* is 2243. The value of *Kp* in q-direction is 828 and the value of *Ki* is 532. The value of the scaling factor in d-direction is 82, while the value of the scaling factor in q-direction is 21.

4.4. Hysteresis Controller

The main concept of the hysteresis controller is to compare the reference current obtained by the SRF theory with the actual current drawn from the supply. The switching process occurs within upper and lower bands to avoid the continuous switching. When the actual current exceeds the reference current by a value greater than the upper band, the switch changes its state from off state to on state and the output voltage changes from $-0.5\,V_{DC}$ to $0.5\,V_{DC}$. Fig. 7 shows the concept of operation of the hysteresis controller. The error signal of the hysteresis controller is the difference between the actual current and the reference current.

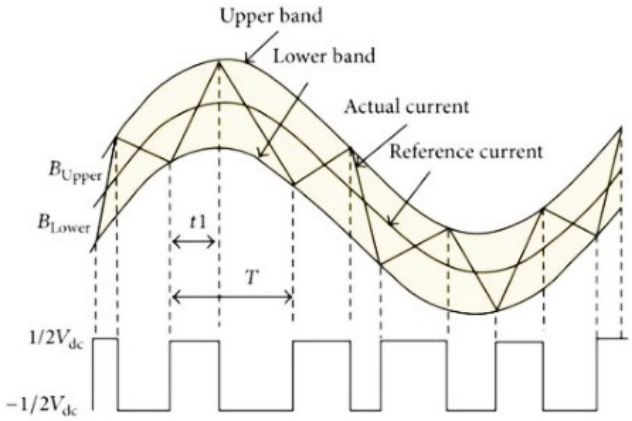

Fig. 7. Hysteresis current control principle.

4.5. Fuzzy Logic Controller

Fig. 8 shows the block diagram of the fuzzy logic system. The inputs of the fuzzy logic controller are the current error (e) and the change of error (de/dt) and expressed as fuzzy logic control variables by a fuzzifier. The inputs and outputs are expressed by membership functions of a triangular, a bell, or a Gaussian form.

The rules express the relationship between the inputs and the output and feed a fuzzy logic inference system. The output of the fuzzy logic controller is defuzzified by a suitable scaling factor for expressing the fuzzy logic controller output. Fig. 9 shows the block diagram of the fuzzy logic current controller designed for the MFC system.

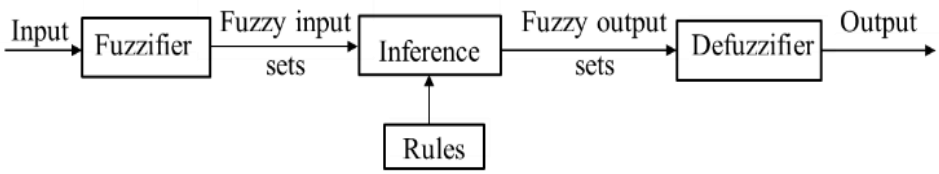

Fig. 8. Fuzzy logic system.

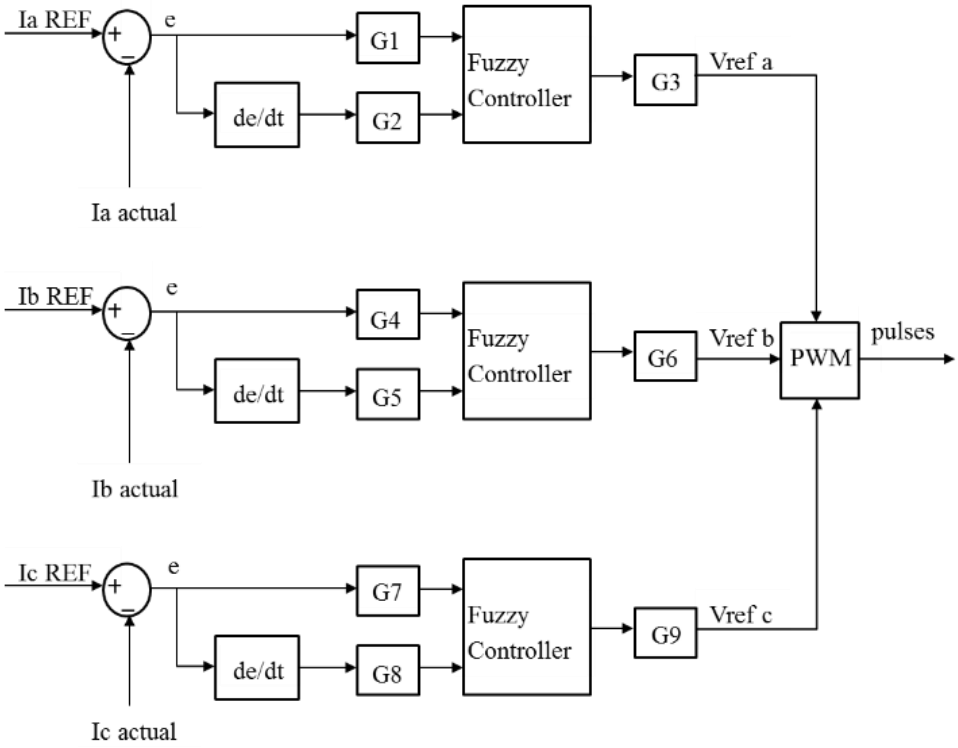

Fig. 9. Fuzzy logic current controller block diagram.

5. SIMULATION RESULTS

The studies are executed using the MATLAB/Simulink simulation platform with a step size of 2×10^{-6} s. The results of harmonics mitigation, and reactive power compensation at bus 4 for obtaining a unity power factor are presented.

5.1. Harmonics Mitigation by the MFC System

The Fast Fourier Transform (FFT) is applied for performing voltages and currents harmonic analyses at bus 4 according to the IEEE Std. 519-2022 [17]. Very short duration study is performed in a time interval of 3 s. This time interval is divided into 15 windows; each window duration is 0.2 s (10 cycles in 50 Hz system) [24]. At each window, harmonics are analyzed till order 50. With voltage level of 12 kV, the THD limit for voltages is 5% and the TDD limit for currents is 5%. For the very short duration study, the THD limit is multiplied by 1.5 and becomes 7.5%, and the TDD limit is multiplied by 2 and becomes 10%. Harmonic analyses are performed first when no MFC system is connected. The THD values of the three phase voltages and the TDD values of the three phase currents for 15 windows are calculated. The average THD value of bus 4 voltage windows are found to be 5.1% which is lower than the required limit. However, the average TDD value of current windows is 26.5% which is significantly larger than the required limit. This requires the installation of an MFC system for mitigating the excessive current harmonics.

An MFC system with an HHO-tuned PI controller is then designed and installed at bus 4. Harmonics analyses of bus 4 voltages and currents are performed. Fig. 10 shows the harmonic spectrum of window 10 of phase A voltage on bus 4. Table 1 summarizes the THD values of all windows of the three phase voltages at bus 4, when the MFC system is controlled by the HHO-tuned PI controller. Fig. 11 shows the harmonic spectrum of window 10 at bus 4 phase A

current, when the MFC system is controlled by the HHO-tuned PI controller. Fig. 12 shows the three-phase voltages of window 10, while Fig. 13 shows the three-phase currents of window 10.

Table 1. THD values of all windows of the three-phase voltages at bus 4 when the MFC system is controlled by the HHO-tuned PI controller.

Time interval	THD-VA	THD-VB	THD-VC
7.0-7.2	4.89	4.88	4.93
7.2-7.4	4.89	4.88	4.93
7.4-7.6	4.89	4.88	4.93
7.6-7.8	4.89	4.88	4.93
7.8-8.0	4.89	4.89	4.93
8.0-8.2	4.89	4.89	4.93
8.2-8.4	4.89	4.89	4.93
8.4-8.6	4.89	4.89	4.93
8.6-8.8	4.89	4.90	4.93
8.8-9.0	4.89	4.90	4.93
9.0-9.2	4.89	4.90	4.94
9.2-9.4	4.89	4.90	4.94
9.4-9.6	4.90	4.90	4.94
9.6-9.8	4.90	4.90	4.94
9.8-10.0	4.90	4.90	4.94
RMS of THD%	4.89	4.90	4.93

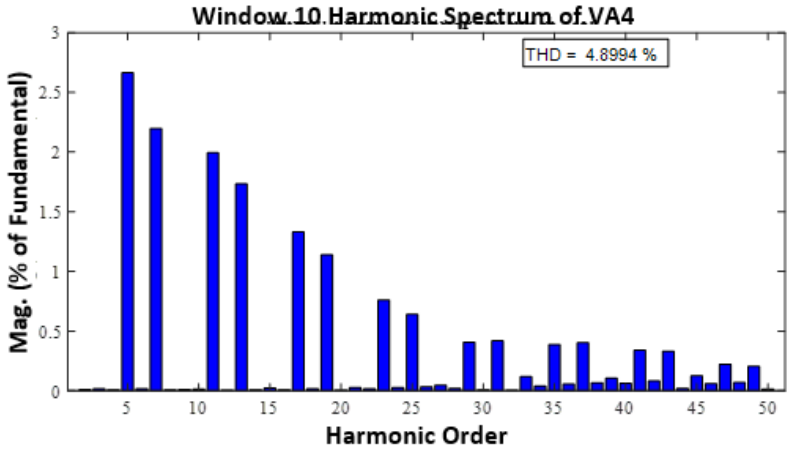

Fig. 10. Harmonic spectrum of window 10 of bus 4 phase A voltage when the MFC system is controlled by the HHO-tuned PI controller.

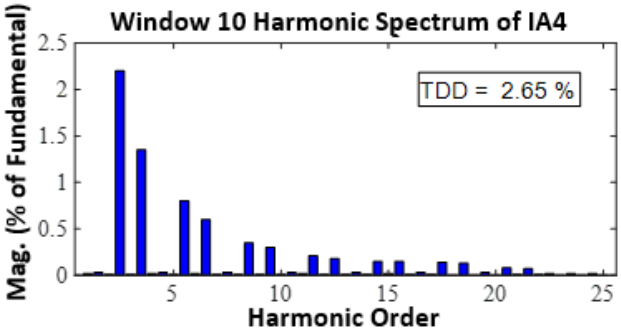

Fig. 11. Harmonic spectrum of window 10 of bus 4 phase A current when the MFC system is controlled by the HHO-tuned PI controller.

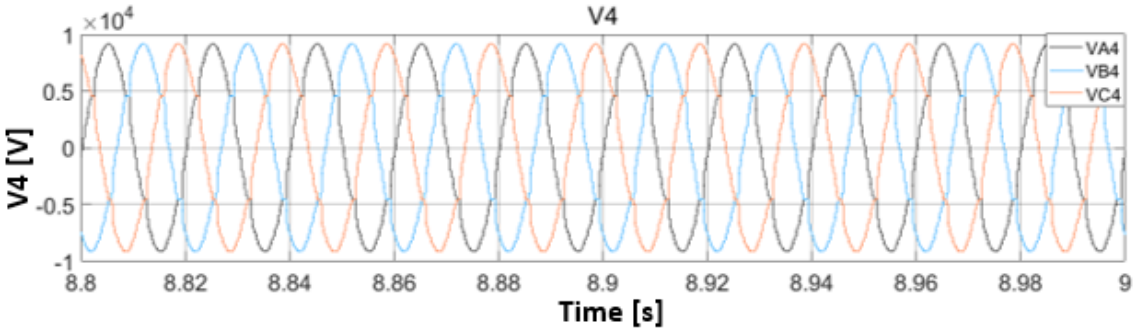

Fig. 12. Window 10 three-phase voltages.

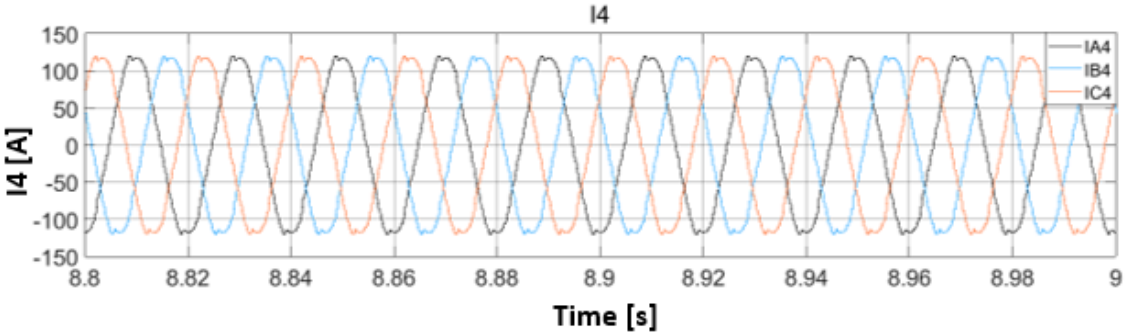

Fig. 13. Window 10 three-phase currents.

Table 2 summarizes the individual harmonics of window 10 at bus 4 phase A voltage when the MFC system is controlled by the HHO-tuned PI controller. According to the IEEE Std. 519-2022 and with very short duration (3 s) and an operating voltage of 12 kV, the limit for any individual voltage harmonic component is 4.5%. Table 2 shows that all individual voltage harmonic components are less than the limit.

Table 2. Individual harmonic components percentages of window 10 at bus 4 phase A voltage when the MFC system is controlled by the HHO-tuned PI controller.

Order	%	Order	%	Order	%	Order	%
2	0.01	15	0.03	28	0.03	41	0.35
3	0.02	16	0.01	29	0.39	42	0.10
4	0.01	17	1.35	30	0.01	43	0.34
5	2.70	18	0.02	31	0.40	44	0.03
6	0.02	19	1.18	32	0.01	45	0.21
7	2.20	20	0.01	33	0.15	46	0.07
8	0.01	21	0.04	34	0.05	47	0.32
9	0.02	22	0.02	35	0.38	48	0.08
10	0.02	23	0.77	36	0.07	49	0.31
11	1.97	24	0.03	37	0.39	50	0.01
12	0.01	25	0.65	38	0.08		
13	1.72	26	0.04	39	0.12		
14	0.01	27	0.05	40	0.08		

Table 3 summarizes the TDD values of all windows of the three phase input currents at bus 4, when the MFC system is controlled by the HHO-tuned PI controller.

Table 4 summarizes the individual harmonics of window 10 of phase A current when the MFC system is connected and controlled by the HHO-tuned PI controller. The dominant current harmonics are the fifth and the seventh harmonic components, which agreed with the

results obtained in [25]. According to the IEEE Std. 519-2022 requirements, all individual current harmonics are less than the limit of individual components.

Table 3. TDD values of all windows of the three phase input currents at bus 4 when the MFC system is controlled by the HHO-tuned PI controller.

Time interval	TDD-IA	TDD-IB	TDD-IC
7.0-7.2	2.64	2.64	2.66
7.2-7.4	2.64	2.64	2.66
7.4-7.6	2.64	2.64	2.66
7.6-7.8	2.64	2.64	2.66
7.8-8.0	2.64	2.64	2.66
8.0-8.2	2.64	2.64	2.66
8.2-8.4	2.64	2.66	2.66
8.4-8.6	2.64	2.66	2.76
8.6-8.8	2.64	2.66	2.76
8.8-9.0	2.64	2.66	2.76
9.0-9.2	2.64	2.66	2.76
9.2-9.4	2.64	2.66	2.76
9.4-9.6	2.66	2.66	2.76
9.6-9.8	2.66	2.66	2.76
9.8-10.0	2.66	2.66	2.76
RMS of TDD%	2.64	2.66	2.76

Table 4. Individual harmonic components percentages of window 10 at bus 4 phase A current when the MFC system is controlled by the HHO-tuned PI controller.

Order	%	Order	%	Order	%	Order	%
2	0.02	15	0.03	28	0.01	41	0.08
3	0.03	16	0.01	29	0.15	42	0.01
4	0.01	17	0.35	30	0.02	43	0.07
5	2.20	18	0.01	31	0.15	44	0.01
6	0.01	19	0.30	32	0.01	45	0.02
7	1.35	20	0.01	33	0.03	46	0.00
8	0.02	21	0.03	34	0.01	47	0.02
9	0.03	22	0.02	35	0.14	48	0.00
10	0.01	23	0.21	36	0.00	49	0.02
11	0.80	24	0.01	37	0.13	50	0.00
12	0.02	25	0.18	38	0.00		
13	0.60	26	0.01	39	0.03		
14	0.01	27	0.03	40	0.00		

Table 5 summarizes the Root Mean Square (RMS) value of the THD values of bus 4 three phase voltages and the RMS value of the TDD values of bus 4 three phase input currents for different cases as follow:

(i) No MFC system is connected (NC).
(ii) MFC system is connected and controlled by the Hysteresis Controller (HC).
(iii) MFC system is connected and controlled by the Fuzzy Logic Controller (FLC).
(iv) MFC system is connected and controlled by the PSO-tuned PI controller (PI-PSO).
(v) MFC system is connected and controlled by the HHO-tuned PI controller (PI-HHO).

Table 5. Summary of THD and TDD RMS values of bus 4 with different controllers.

Control	THD-VA	THD-VB	THD-VC	TDD-IA	TDD-IB	TDD-IC
NC	5.18	5.06	5.08	25.14	24.99	25.25
HC	6.12	6.31	6.19	3.30	3.33	3.29
FLC	5.52	5.33	5.56	3.34	3.33	3.36
PI-PSO	5.55	5.44	5.62	3.41	3.40	3.42
PI-HHO	4.89	4.90	4.93	2.64	2.66	2.76

Table 6 shows a comparison between the average TDD values of the different buses of the modified Cigre benchmark network when no MFC system is connected and when the MFC system is connected to bus 4. In Table 6, the connected MFC system is controlled by the HHO-tuned PI controller. It is noticed that with no MFC system, the TDD value of the current input at bus 4 is the largest, because the VSD is connected at this bus. The input current at bus 3 is equal to the input current at bus 4 plus the current of the linear load connected to bus 3, so the TDD value of the input current at bus 3 is less than the TDD value of the input current at bus 4. The TDD value of the input current at bus 2 is less than the TDD value of the input current at bus 4 for the same reason. The TDD values of the other buses are relatively very small. The connection of the MFC system at bus 4 significantly reduces the TDD values of the input currents at buses 2, 3, and 4 as shown in the table.

Table 6. Comparison of TDD at all buses when there is no MFC system and when the MFC system at bus 4, controlled by the HHO-tuned PI controller.

Bus	Without MFC system	With MFC system	Bus	Without MFC system	With MFC system
1	18.29	1.35	8	0.06	0.04
2	18.29	1.35	9	0.06	0.05
3	21.74	2.00	10	0.07	0.06
4	25.12	2.68	11	0.08	0.06
5	0.08	0.06	12	0.06	0.05
6	0.08	0.06	13	0.06	0.05
7	0.08	0.06	14	0.07	0.06

Table 7 shows a comparison between the average THD values at the different buses of the Cigre benchmark network, when no MFC system is connected and when the MFC system is connected to bus 4. The connected MFC system is controlled by the HHO-tuned PI controller. With no MFC system, the THD value at bus 4 is the largest, because the VSD is connected to this bus. The THD values of the buses near bus 4 are high, while the THD values of the far buses are small. The THD values on buses 12, 13, and 14 are very small, because they are connected to a separate branch in the Cigre benchmark network. When the MFC system is connected to bus 4 and controlled by the HHO-tuned PI controller, further reductions in the THD values at the different buses are achieved. The simulation results show that the HHO-tuned PI controller provides the best performance in terms of current harmonics mitigation and THD values reduction.

5.2. Reactive power compensation by the MFC system

To investigate the reactive power compensation capability of the MFC system, an RL load will be connected at bus 4, where the VSD is installed, through a circuit breaker. The power

factor of the RL load is 0.8 and its reactive power is 200 kVAr. The circuit breaker is closed at $t = 16\ s$.

Table 7. Comparison of THD values at all buses when no MFC system and when the MFC system at bus 4, controlled by the HHO-tuned PI controller.

Bus	Without MFC System	With MFC system	Bus	Without MFC system	With MFC system
1	1.72	1.54	8	0.55	0.33
2	3.46	3.22	9	0.48	0.31
3	4.33	4.12	10	0.41	0.29
4	5.06	4.90	11	0.38	0.28
5	3.92	3.80	12	0.06	0.03
6	2.37	2.18	13	0.06	0.03
7	0.35	0.27	14	0.04	0.02

Fig. 14 shows the VSD reactive power with a steady state value of 830 kVAr before connecting the RL load, then some damped transients occur in the time interval from $t = 16\ s$ to $t = 16.8\ s$ due to the variations of bus 4 currents and voltages during the transient interval. The VSD reactive power returns to its steady state value of 830 kVAr, after the transient interval is ended. Fig. 15 shows the reactive power of the RL load. At $t = 16\ s$, the reactive power starts with zero value, then increases in the transient interval gradually due to the circuit time constant and then reaches a steady state value of 200 kVAr.

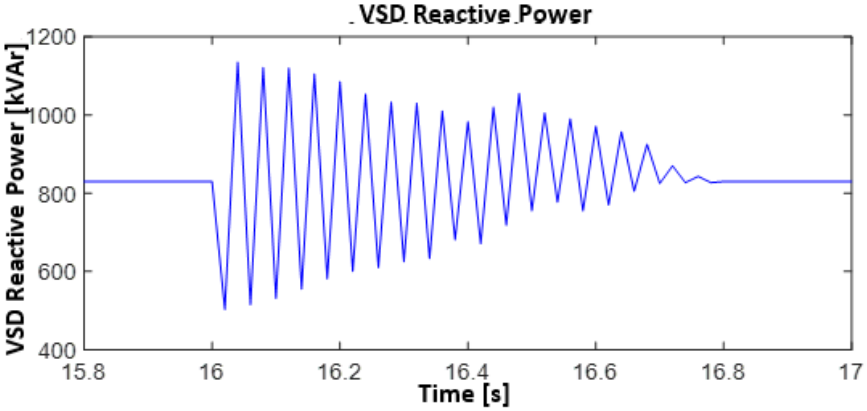

Fig. 14. Reactive power of the VSD.

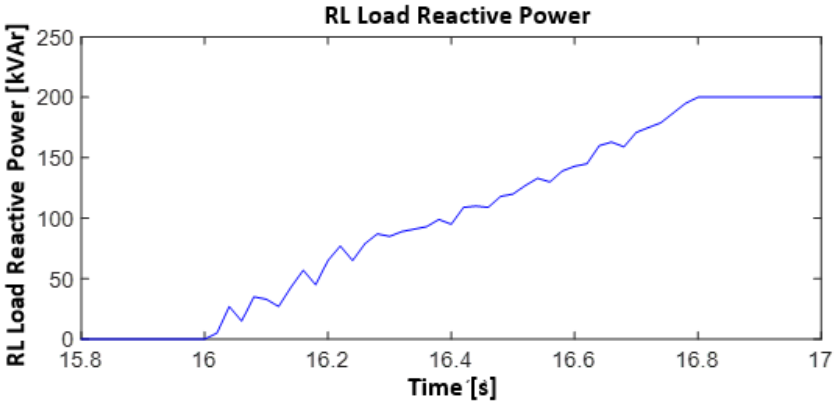

Fig. 15. RL loads reactive power.

Fig. 16 shows the MFC system reactive power. The MFC system reactive power is negative (capacitive) for compensating the positive (inductive) VSD reactive power. The MFC system reactive power starts at a steady state value of −830 kVAr, which equals the VSD

reactive power, followed by a transient interval of 0.8 s with decrease in the MFC system injected reactive power, then reaches a steady state value of −1030 kVAr. The steady state injected reactive power by the MFC system is increased due to the connection of the RL load of 200 kVAr reactive power.

Fig. 17 shows bus 4 reactive power change with time. Before the RL load is switched, the reactive power measured at bus 4 is zero, because it is compensated by the MFC system. When the RL load is switched on, a transient period occurs with changes of the reactive power. After the switching, bus 4 reactive power increased for compensating the RL load reactive power, then it gradually decreased to zero value, because the MFC system control system started to compensate the RL load reactive power. Finally, the RL load reactive power is compensated completely by the MFC system, and then the reactive power of bus 4 becomes zero.

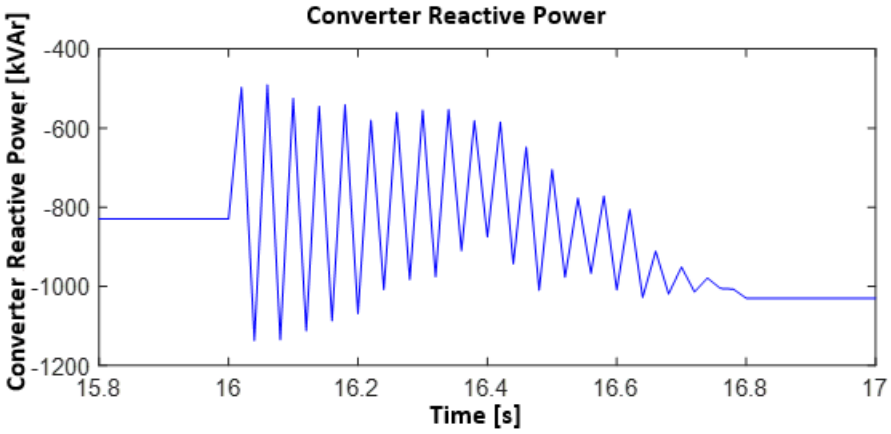

Fig. 16. MFC system reactive power.

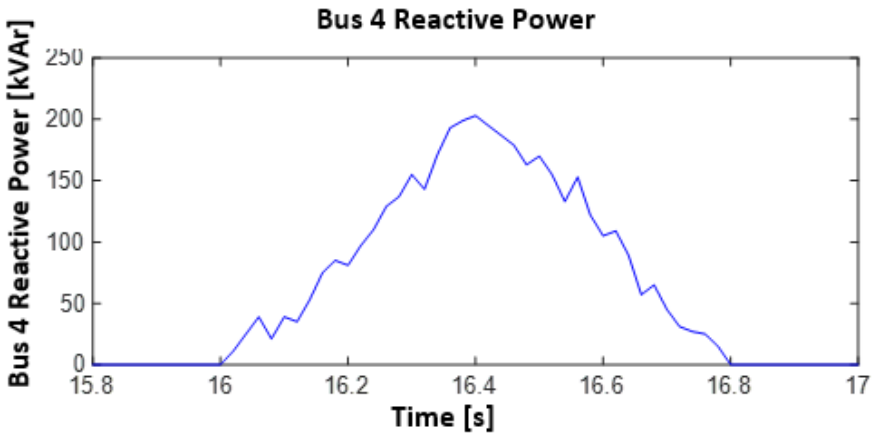

Fig. 17. Bus 4 reactive power.

Fig. 18 shows the voltages and current waveforms from $t = 15.8\,s$ to $t = 17\,s$ for showing the change from steady state condition to the transient condition, then the steady state condition. Fig. 19 shows bus 4 voltages and currents from $t = 15\,s$ to $t = 15.1\,s$. In this interval, bus 4 reactive power is compensated by the MFC system for obtaining a unity power factor at bus 4. In this case, bus 4 currents are in phase with bus 4 corresponding voltages. Fig. 20 shows 4 voltages and currents during a part of the transient interval from $t = 16\,s$ to $t = 16.04\,s$. During this interval, bus 4 currents lag bus 4 voltages due to the connection of the RL load. Bus 4 currents lag bus 4 voltages by a small angle, because the connected RL load reactive power is small compared with the VSD active power. Fig. 21 shows bus 4 voltages and currents from $t = 17.9\,s$ to $t = 18\,s$. In this interval, bus 4 reactive power is compensated by the MFC system

for achieving zero reactive power of bus 4, and a unity power factor occurs. In this case, bus 4 currents are in phase with bus 4 corresponding voltages, and the steady state currents at bus 4 are increased due to the added active power of the RL load.

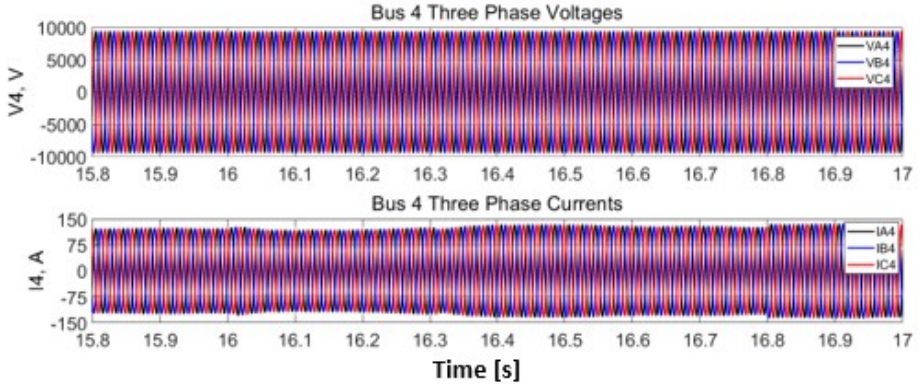

Fig. 18. Bus 4 voltage and current waveforms in the interval from $t = 15.8\ s$ to $t = 17\ s$.

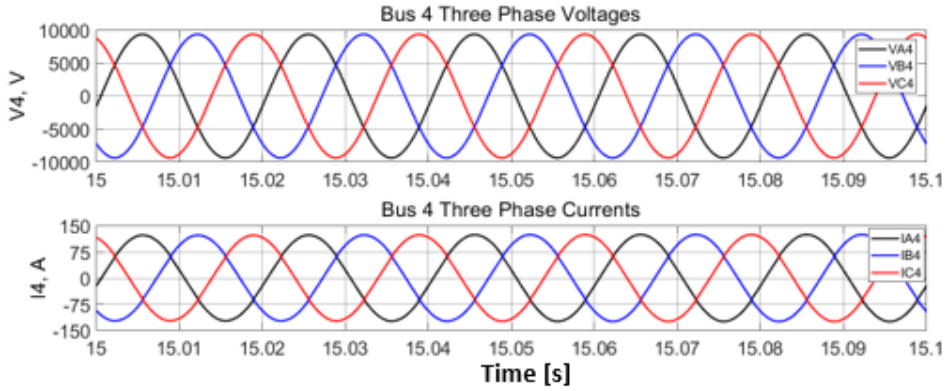

Fig. 19. Bus 4 steady state voltage and current waveforms before adding the RL load.

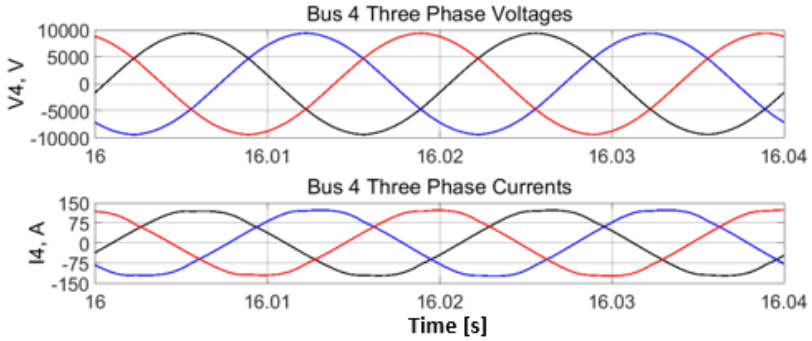

Fig. 20. Bus 4 voltage and current waveforms in a part of the transient interval from $t = 16\ s$ to $t = 16.04\ s$.

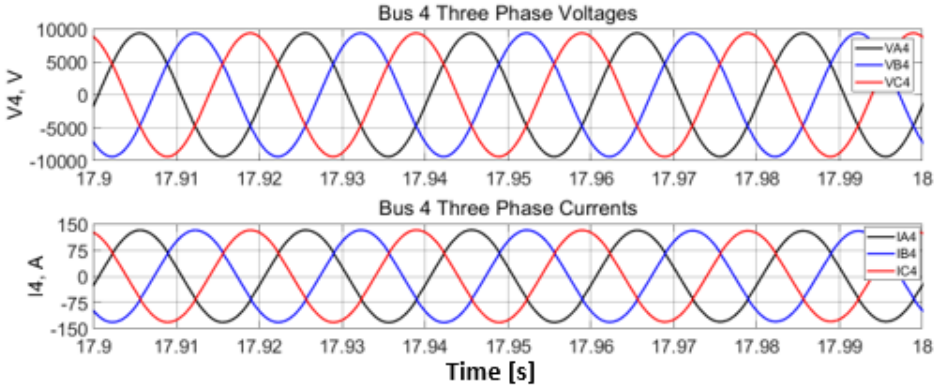

Fig. 21. Bus 4 steady state voltage and current waveforms after adding the RL load.

The MFC system is connected at bus 4, where the VSD is connected. From ABB catalog for the high voltage motor take the motor model (NMK 500L4A) as the case study for the induction motor and this motor has the following specifications from ABB catalog:

P_o = 1400 kW, n_s = 1500 r/min (4 poles), 50 Hz, n_r = 1486 r/min, efficiency at full load (η_{fl}) = 94.9%, power factor at full load (PF_{fl}) = 0.88, T_n = 8996 N.m., T_{max} = 20690.8 N.m., no load current (I_0) = 25 A, rotor inertia (J) = 76.6 kg.m^2.

An RL load is connected in parallel with the VSD at bus 4 through a circuit breaker. The reactive power of the RL load is 200 kVAr, the power factor is 0.8. The circuit breaker is closed at $t = 16\ s$. Fig. 22 shows phase A stator current of the motor, which is deformed due to the associated harmonics resulted from the power electronics components including the rectifier and the inverter of the VSD. The TDD of the stator current is 22%, which is high due to the existence of power electronics components in the VSD including the rectifier and the inverter. The stator current deformations cause electric torque and speed ripples. The deformation of the current due to the existence of power electronics components of the VSD including the rectifier and the inverter contributes to occurring the speed and torque ripples.

Fig. 23 shows bus 4 phase A voltage. After the switching occurrence, the voltage RMS value decreased from 6649 V to 6634.8 V (0.214%) due to the connection of the RL load. The change of voltage contributes to the occurring speed and torque ripples.

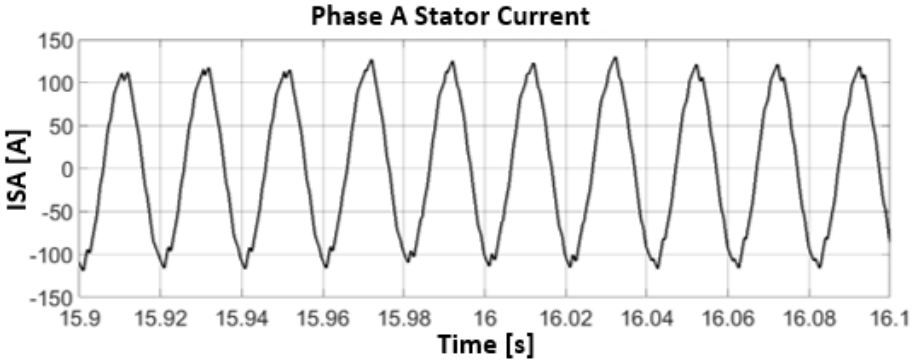

Fig. 22. Phase A stator current of the motor.

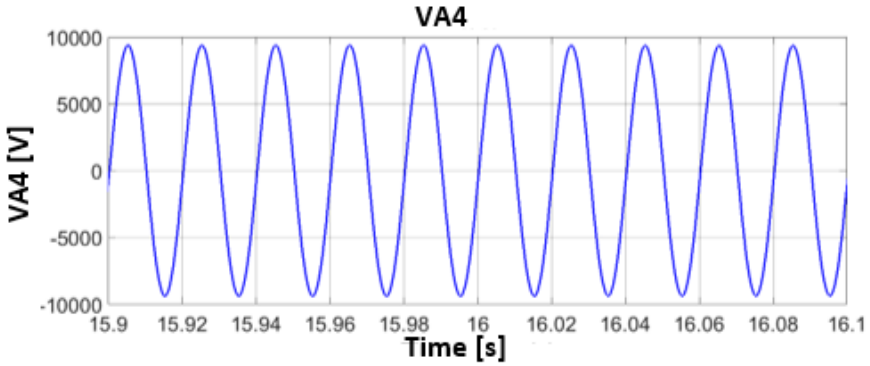

Fig. 23. Bus 4 phase A voltage.

Fig. 24 shows the electrical torque of the motor in the interval from $t = 10\ s$ to $t = 30\ s$. To evaluate the torque ripples, an arbitrary interval of 0.5 s is examined. Before connecting the RL load and during the interval from $t = 15\ s$ to $t = 15.5\ s$, the torque varies between T_{max} = 8870 N.m. and T_{min} 9165 N.m. The ratio of electric torque ripples is found to be 3.28%. After the connection of the RL load and during the interval from $t = 29.5\ s$ to $t = 30\ s$, the ripples ratio

is 3.73%. Fig. 25 shows the motor speed. Similarly, the ratios of speed ripples before and after connecting the RL load are found to be 0.54% and 0.81% respectively. These are acceptable ripples for the VSD.

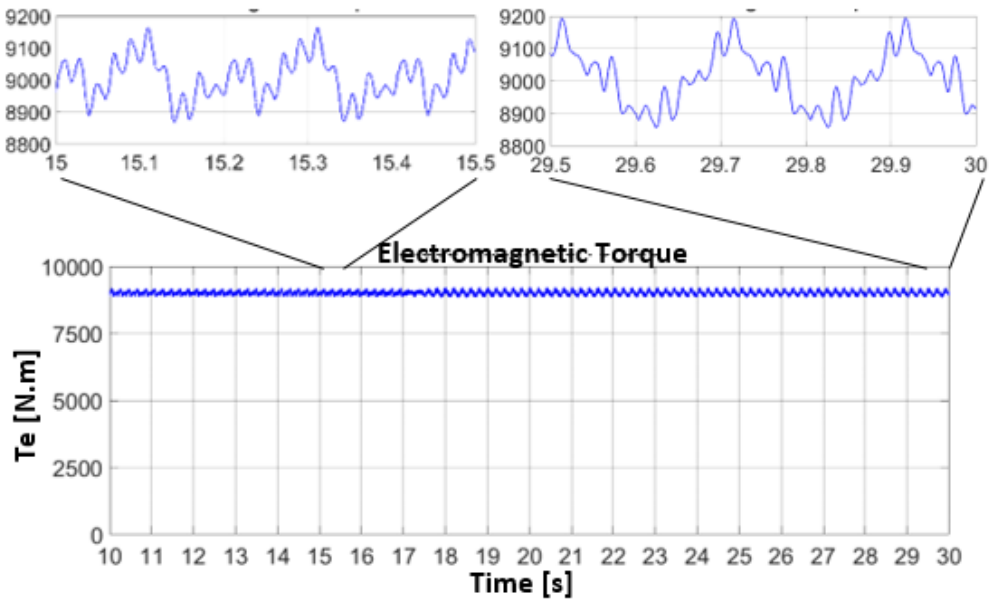

Fig. 24. Motor electrical torque.

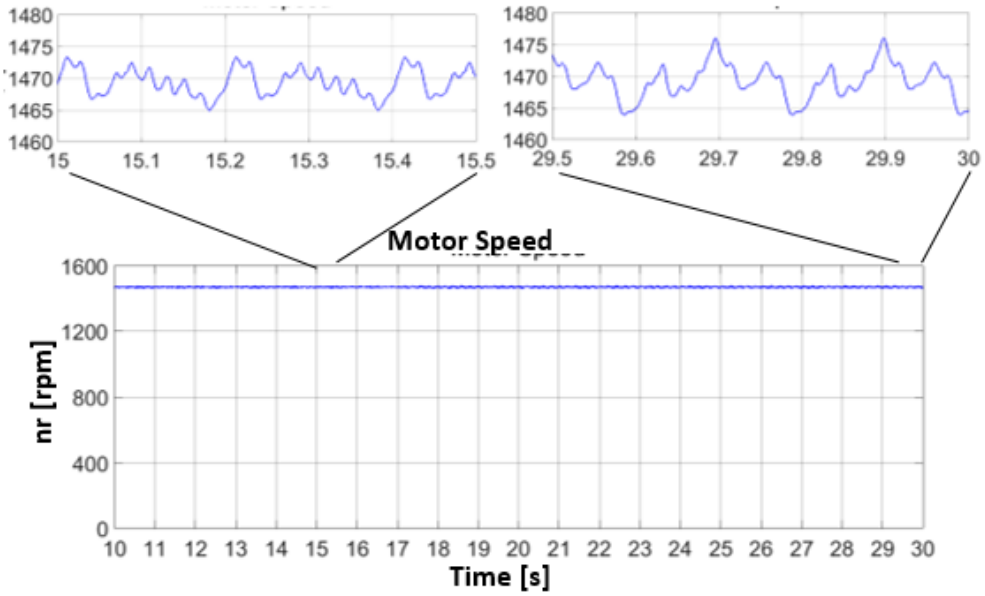

Fig. 25. Motor speed.

After the connection of the RL load and during the interval from $t = 29.5\ s$ to $t = 30\ s$, the motor speed changes from 1464 rpm to 1476 rpm, and the speed ripples percentage is 0.81%. This is accepted speed ripple percentage for the VSD. As concluded, the speed ripples are small and increased by a small value due to the connection of the RL load, which makes some small changes in the PCC voltages and currents.

6. CONCLUSIONS

Harmonic analyses of the VSD are performed according to the requirements of the IEEE Std. 519-2022 and using the FFT. Five cases are studied using the MATLAB/Simulink

software: (i) no MFC system; (ii) installing an MFC system controlled by a hysteresis controller; (iii) installing an MFC system controlled by a fuzzy logic controller; (iv) installing an MFC system controlled by a PSO-tuned PI controller; and (v) installing an MFC system controlled by an HHO-tuned PI controller. Moreover, the reactive power compensation at bus 4 for obtaining a unity power factor is performed.

The results show that with no MFC system, the TDD values exceed the limit (10%). When the MFC system is connected to bus 4 and controlled by the HHO-tuned PI controller, significant reduction in the TDD and THD values at the different buses of the Cigre benchmark network occurs. Although the hysteresis controller, the fuzzy controller, and the PSO-tuned PI controller reduce the TDD and THD values to be less than the limits, the performance with the HHO-tuned PI controller is the best. Controlling the MFC system by the HHO-tuned PI controller provides the best performance in terms of currents and voltages harmonics mitigation compared with the other controllers. Moreover, the proposed MFC system compensates bus 4 reactive power for achieving a unity power factor.

Appendix

Horse Characteristics [21-23]

Grazing

Horse grazes for 16 to 20 hours per day. Horses grazes at all stages of their life span. The grazing is expressed mathematically as follows:

$$G_m{}^{Iter,AGE} = \mathrm{g}_{Iter}(u + pl)\left[\vec{X}_m{}^{(Iter-1)}\right], AGE = \alpha, \beta, \gamma, \delta \quad \text{(A-1)}$$

$$g_m{}^{Iter,AGE} = g_m{}^{(Iter-1),AGE} \times \omega_g \quad \text{(A-2)}$$

where,

$G_m{}^{Iter,AGE}$ is the motion factor i^{th} horse. This factor decreases linearity of ω_g value in an iteration.

$l\ and\ u$ are the high and low limits of the grazing region.

p is a random number changes between 0 and 1.

ω_g is decrease parameter in each iteration.

Hierarchy

For horses between ages 5 and 15, the hierarchy is expressed as follows:

$$H_m{}^{Iter,AGE} = h_m{}^{Iter,AGE}\left[\vec{X}_*{}^{(Iter-1)} - \vec{X}_m{}^{(Iter-1)}\right], AGE = \beta, \gamma \quad \text{(A-3)}$$

$$h_m{}^{Iter,AGE} = h_m{}^{(Iter-1),AGE} \times \omega_h \quad \text{(A-4)}$$

where,

$H_m{}^{Iter,AGE}$ shows the effect of the better position of horses on the velocity vector.

$\vec{X}_*{}^{(Iter-1)}$ is the position of the better horse.

ω_h is decrease parameter in each iteration.

Sociability

The horses are active in the herd between ages 5 and 15, the sociability is expressed as follows:

$$S_m{}^{Iter,AGE} = s_m{}^{Iter,AGE}\left[\left(\frac{1}{N}\sum_{j=1}^{N}\vec{X}_j{}^{(Iter-1)}\right) - \vec{X}_m{}^{(Iter-1)}\right], AGE = \beta, \gamma \quad \text{(A-5)}$$

$$s_m{}^{Iter,AGE} = s_m{}^{(Iter-1),AGE} \times \omega_s \quad \text{(A-6)}$$

where,

$S_m{}^{Iter,AGE}$ is the social move vector of i^{th} horse.

N is the total number of horses.

ω_s is decrease parameter in each iteration.

Imitating

The horses are active in the herd between ages 5 and 15, the sociability is expressed as follows:

$$I_m{}^{Iter,AGE} = i_m{}^{Iter,AGE}\left[\left(\frac{1}{pN}\sum_{j=1}^{pN}\vec{X}_j{}^{(Iter-1)}\right) - \vec{X}_m{}^{(Iter-1)}\right], AGE = \gamma, \delta \quad \text{(A-7)}$$

$$i_m{}^{Iter,AGE} = i_m{}^{(Iter-1),AGE} \times \omega_i \quad \text{(A-8)}$$

where,

$I_m{}^{Iter,AGE}$ is the social move vector of i^{th} horse.

pN is the total number of horses in the better location, p represents 10 percent of the total number of horses.

ω_i is decrease parameter in each iteration.

Defencing

Defencing is required for keeping horses away from any undesired position, the defencing is expressed as follows:

$$D_m{}^{Iter,AGE} = -d_m{}^{Iter,AGE}\left[\left(\frac{1}{qN}\sum_{j=1}^{qN}\vec{X}_j{}^{(Iter-1)}\right) - \vec{X}_m{}^{(Iter-1)}\right], AGE = \alpha, \beta, \gamma \quad \text{(A-9)}$$

$$d_m{}^{Iter,AGE} = d_m{}^{(Iter-1),AGE} \times \omega_d \quad \text{(A-10)}$$

where,

$D_m{}^{Iter,AGE}$ is the escape parameter of i^{th} horse from average value of few horses in undesired places.

qN is the total number of horses in undesired places, q represents 20 percent of the total number of horses.

ω_d is decrease parameter in each iteration.

Roaming

Roaming of the horses is often noticed when they are young and gradually fades when they are mature, the roaming is expressed as follows:

$$R_m{}^{Iter,AGE} = r_m{}^{Iter,AGE}\, p\, \vec{X}_r{}^{(Iter-1)}, AGE = \gamma, \delta \quad \text{(A-11)}$$

$$r_m{}^{Iter,AGE} = r_m{}^{(Iter-1),AGE} \times \omega_r \quad \text{(A-12)}$$

where,

$R_m{}^{Iter,AGE}$ is the random selected velocity of i^{th} horse for the local searching and the escape from local minimum. ω_r is decrease parameter in each iteration.

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