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Design of GaN-Based Phase-Locked Dielectric Resonator Oscillator for Strategic Applications

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***Abstract*—** Electronic warfare systems have stringent requirements of ultra-low phase noise and substantial high-power oscillators, thus demanding an additional amplifier to drive subsequent stages. Most of the oscillator designs - realized using GaAs/SiGe technology - have the advantage of low phase noise profile, but offer low output power. GaN-based Dielectric Resonator Oscillators (DRO) could be one of the solutions due to their high power, quality factor, and compact size. Their phase noise profile can be further improved by Phase Locking loops (PLL). In this work, a hybrid phase-locking technique that amalgamates the salient features of the two most common techniques available in the literature, namely Analog PLL and Digital PLL, is presented. The designed GaN-based PL-DRO presents a substantial output power of 24 dBm at 12 GHz with excellent phase noise of -119 dBc/Hz at 100 kHz offset frequency. Performance evaluation of the proposed design compared with the state-of-the-art similar designs reported in literature has been carried out. It reveals that the proposed design is the most compact, low-cost, and efficient. Therefore, the suggested phase-locking approach can be used to design ultra-low phase noise DROs for strategic electronics communication systems.

***Keywords*—** Frequency synthesizer; Gallium Nitride (GaN) devices; Step recovery diode; Phase locked dielectric resonator oscillators.

1. INTRODUCTION

Microwave communication systems such as satellite base stations, electronic warfare, phased array systems, etc. often require high-capacity data transmission [1, 2]. They need RF / Microwave signal sources with high stability, low phase noise, and excellent spectral purity for security, anti-jamming, etc. applications. Such systems employ frequency synthesizers as a tunable local oscillator (LO) for up / down-conversion of RF signals. Frequency synthesizers especially in Radars often have more stringent noise and spurious signal requirements, primarily because they are used as the timing reference between the transmitted and received signals of the radar. Frequency synthesizers can be realized essentially using two approaches: Direct Digital Synthesizers (DDS) and indirect synthesizers. However, for radiofrequency operations, DDS needs additional components such as prescaler, mixer, amplifier, etc., which makes the system complex and costly. Instead, an indirect frequency synthesizer that integrates the voltage-controlled oscillator and Phase Locked Loop (PLL) is preferably used.

The PLL can be used as the basis for a frequency synthesizer that can produce a sequence of frequencies that are derived from a stable reference oscillator. A higher LO phase noise limits the dynamic range of the receiver. So, it is essential that the reference

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signals in the frequency synthesizer have low-phase noise so that noise degradation after frequency translation is within acceptable limits. Microwave oscillators use LC resonators, cavity resonators, Surface Acoustic Wave (SAW) resonators, coaxial resonators, and Dielectric resonators etc. as the frequency-determining elements.

Dielectric resonator has an advantage due to its low cost and very high Q-factor, typically 10,000 for 4 GHz, which translates to low-phase noise of -110 to -120 dBc /Hz at 100 kHz offset. The practical frequency range for dielectric resonators is up to 40 GHz, and the Q-factor reduces linearly with frequency. However, the further improvement of frequency stability and aging can be achieved by phase locking the Dielectric Resonator Oscillator (DRO) to a low-frequency crystal oscillator [3, 4]. The harmonics and spurious outputs of the Phase locked DRO (PL-DRO) also have to be low so that frequency selectivity can be improved. These parameters also depend on the phase-locking scheme used to design the PL-DRO. The most common schemes used to lock a DRO are an analog PLL (Sampling Phase Detector (SPD) based PLL) or a digital PLL [5].

The literature reveals that analog PLL (SPD-PLL) using Step Recovery Diode (SRD) has several advantages such as low phase noise, lower cost, etc. Although the SRD provides high-frequency multiplication, its output voltage is lower than that of traditional phase detectors with charge pumps. This necessitates additional circuitry, increasing system complexity [6, 7]. Further, it has a high lock-in time due to limitations on the loop filter bandwidth. On the other hand, digital PLL requires an extra frequency divider. The divider factor is quite high for a higher frequency of operation, which results in phase noise degradation [8-10]. Hence, to improve the phase noise, it is required to increase the phase-detection frequency and reduce the frequency division ratio. Conversely, the high-frequency reference with ultra-low phase noise is hard to achieve and expensive. This encourages the need to generate increasingly higher frequencies and high output power while maintaining the minimum phase noise.

The majority of oscillator in PL-DRO developed so far has been using SiGe, SiC, and GaAs technology due to their low phase noise characteristics. However, they often have a relatively low output power level. Hence such oscillators require separate power amplifiers [11] especially for strategic applications. This leads to increased system complexity, size, weight, and cost.

In contrast, GaN transistors are an excellent choice for applications requiring a high output power level and power added efficiency due to their high breakdown voltage, high power capability, and good efficiency. Most of the work [12-14] focuses on exploring the capabilities of GaN devices for developing high power amplifiers, with limited work being published on GaN-based oscillators [15-16].

In this paper, the authors propose a hybrid phase-locking scheme that alleviates the problems of analog and digital PLL and the use of a GaN device for the design of the negative resistance oscillator. To the best of authors' knowledge, this work is one of its kinds to report the phase locking scheme for a high-power GaN-based DRO at high frequency applications.

The paper is organised as follows: Section 2 briefly discusses the design and simulation of individual components such as dielectric resonator, negative resistance DRO, Frequency multiplier, loop filter. Section 3 presents the results of integrated PLDRO system, while section 4 concludes the paper.

2. DESIGN OF SRD BASED PL-DRO

To overcome the limitations of analog and digital PLL and considering the high operating frequency of the proposed PL-DRO, a hybrid approach of PLL is proposed in this work. The focus of work being high-frequency, noise-sensitive, high-power applications, the PLL is designed using solid-state technology rather than CMOS [17]. In the proposed scheme, it is intended to implement a frequency multiplier between a reference frequency and input of Phase-Frequency Detector (PFD) to cater to the requirement of ultra-low phase noise. This lowers the required input reference frequency and the frequency divider count. The complete loop thus comprises of frequency multiplier, PFD, loop filter, DRO, and frequency divider as shown in Fig. 1. The preliminary design considerations of such a system demand an apt selection of PLL topology, device technology, DRO design, PFD [18] etc. A SRD was chosen as the basis for multiplier design due to its nonlinear properties, ability to attain good higher-order frequency multiplication, and fast pulse generation. This would lower the required input reference frequency and the frequency divider count.

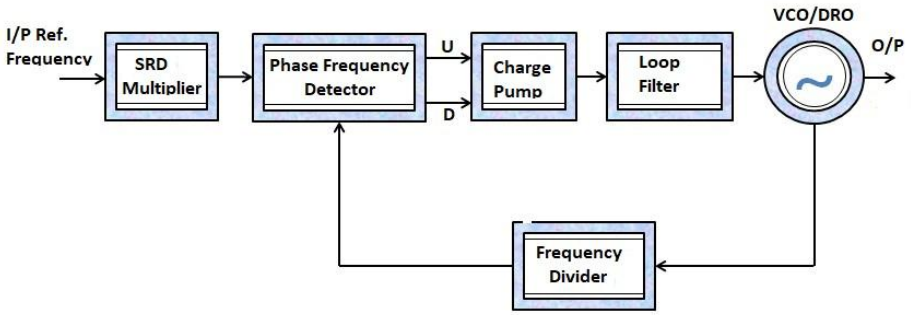


Fig. 1. Block diagram of SRD- phase-locked dielectric resonator oscillator.

2.1. Dielectric Resonator Oscillator

The Dielectric Resonator (DR) puck DRT0510224V series is used in this work, generally shielded by a metal casing to prevent excessive noise and enhance DRO performance. The dimensions (height) of the metal cavity have been such that the cavity resonates at a frequency much higher than the resonant frequency of the DR puck. The DR puck, when simulated using 3D-Analyst of Cadence Microwave Office, resonated approximately at 11.996 GHz with a return loss of -25.95 dB and an insertion loss of -0.43 dB, as shown in Fig. 2.

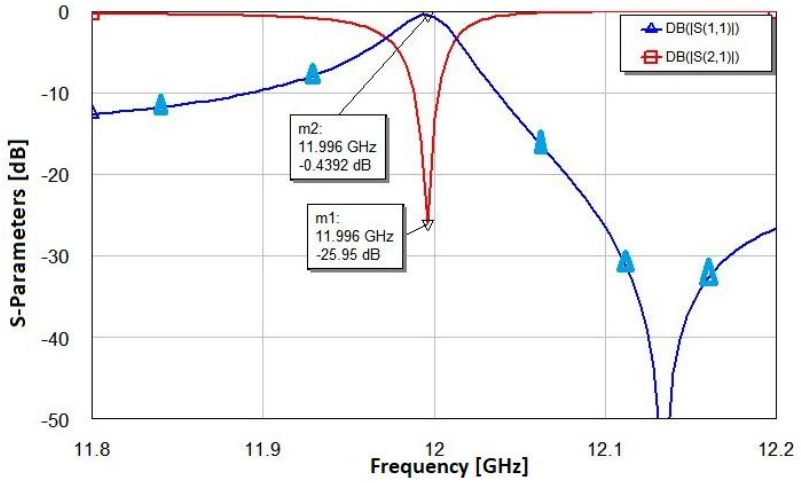


Fig. 2. Simulated transmission and reflection coefficients of DR puck coupled to microstrip line.

Even a slight variation (± 0.1%) in the enclosure dimensions, fabrication tolerances (± 0.5%) or temperature changes (± 1°) may lead to a deviation in frequency from the desired value. Hence, a metal tuning screw in the form of a rotor of length 8.2 mm was inserted into the enclosure from the top of DR as shown in Fig. 3a. As the tuning gap decreases, the magnetic energy changes, thereby increasing the frequency of oscillation. The minimum spacing between the tuning screw and DR puck is kept at least half the DR puck height so that the Q value of the DR puck is not degraded. The design can be tuned over a maximum frequency band of 180 MHz (11.94 GHz–12.12 GHz), as depicted in Fig. 3b.

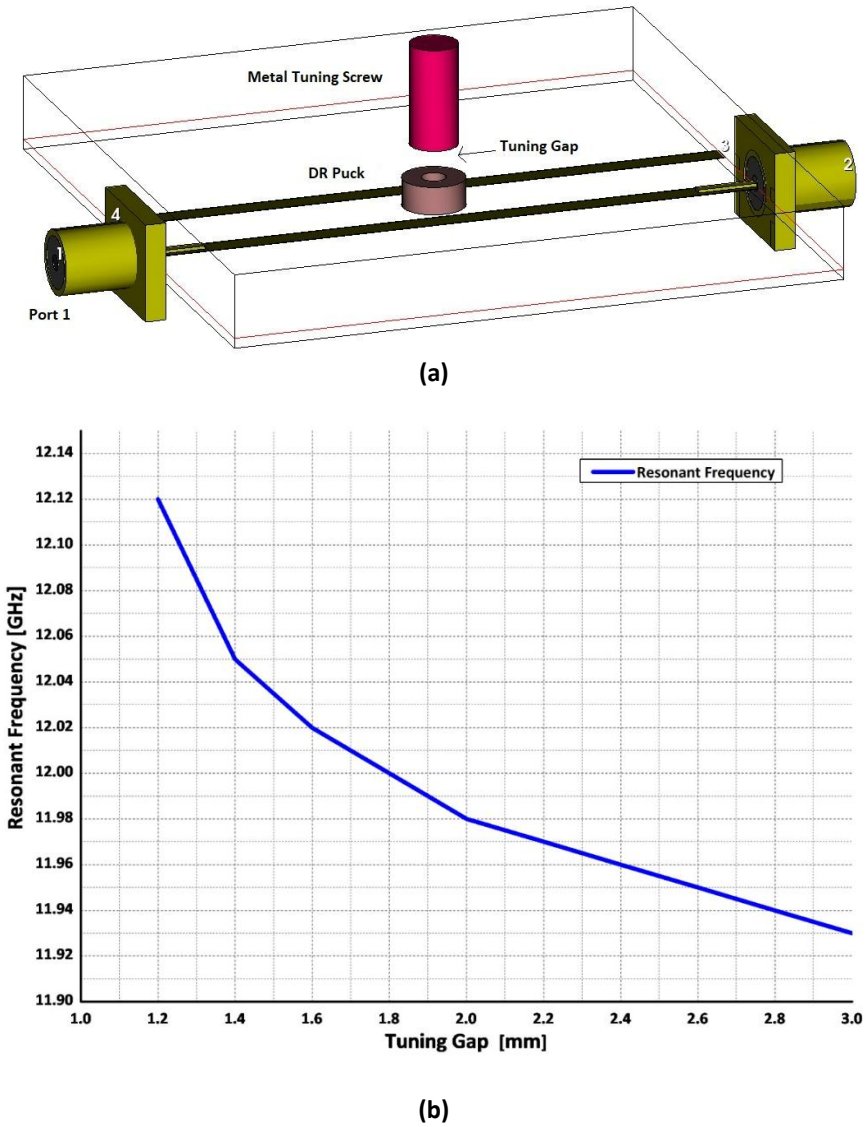


Fig. 3. DR puck: a) with mechanical tuning; b) resonant frequency vs tuning gap.

The tuning range is further improved using a varactor diode (Fig. 4) whose capacitance changes with a change in the applied bias voltage. This circuit setup is then incorporated with an active device to work as a voltage tuned DRO in a PLL. There are several other ways to increase DRO tuning range, such as using multiple resonators, MEMS technology, temperature correction, and hybrid designs. Advanced materials, accurate tuning mechanisms, and hybrid topologies allow DROs to attain substantially larger tuning ranges, increasing their suitability for a variety of RF systems, including radar, sensing, and communications. Taking into account the trade-offs, a successful integration of these

methods will guarantee a wider operating frequency range while preserving the high performance needed for practical applications.

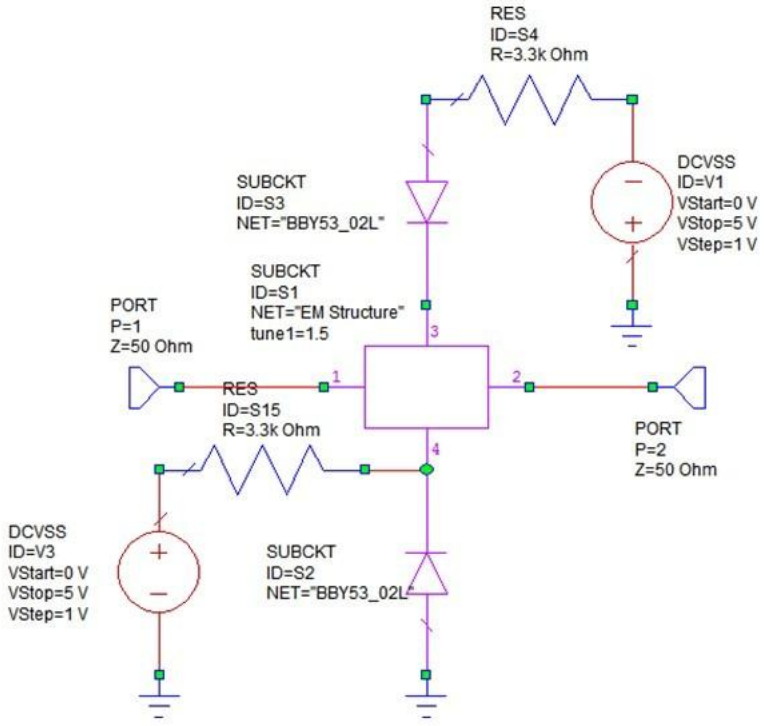


Fig. 4. DR Puck with electrical tuning.

The proposed design (Fig. 5) relies on the fundamental concept of negative resistance DRO using the tuning circuit, which consists of a DR puck and an amplifying device. On account of the low noise figure (1.2 dB), high 3-dB output power (33 dBm), and high 3-dB gain (20 dB), the TGF2942 GaN device is selected as an active device with a DR puck in series feedback topology.

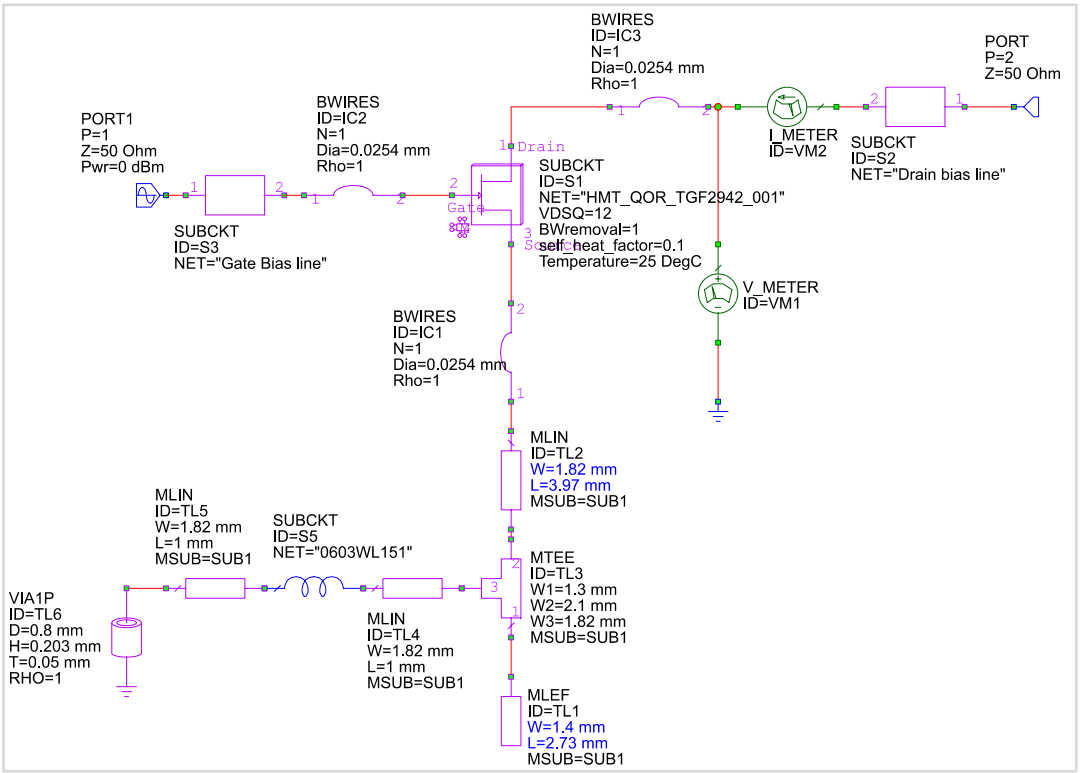


Fig. 5. Negative resistance oscillator.

The use of series feedback instead of parallel reveals the advantage of better load pulling, thereby achieving an optimum trade-off between the output power and phase noise. The loss in the resonator circuit is compensated proportionately by adjusting the negative resistance and the coupling coefficient between the resonator and negative resistance. The length of the stub at the source of the active device is tuned such that it maximizes the negative resistance and makes the reflection coefficient greater than 1. The biasing circuit for the drain and gate comprises of a RF choke, a radial stub, and a bank of capacitors for terminating undesirable frequencies. The RF choke is used to ensure that the correct DC operating voltage is supplied to an active device without allowing the DC supply circuitry to present an improper high-frequency termination to the device. In this design, a Rogers 4003C™ substrate with a dielectric constant of 3.5, a thickness of 0.8 mm, and loss tangent of 0.0035 is used. For an operation to be unstable, the output impedance R_{out} is tuned to be negative at the desired resonant frequency. Eqs. (1-7) represent the conditions to achieve the steady state oscillations.

$$\Gamma r\, \Gamma o \tag{1}$$

$$\frac{(Z_r - Z_0)}{(Z_r + Z_0)} \frac{(Z_{in} - Z_0)}{(Z_{in} + Z_0)} = 1 \tag{2}$$

$$Z_r = R_r + JX_r \tag{3}$$

where Z_r and Z_o are resonator and characteristics impedance respectively.

Above Eq. (3) reduces to:

$$Z_r Z_{in} - Z_{in} Z_0 - Z_0 Z_r + {Z_0}^2 = Z_r Z_{in} + Z_{in} Z_0 + Z_0 Z_r + {Z_0}^2 \tag{4}$$

$$Z_r + Z_{in} = 0 \tag{5}$$

Eq. (5) can be further reduced to Eqs. (6-7) which would decide the matching circuit design (Fig. 6).

$$R_{in} + R_r = 0 \tag{6}$$

$$X_{in} + X_r = 0 \tag{7}$$

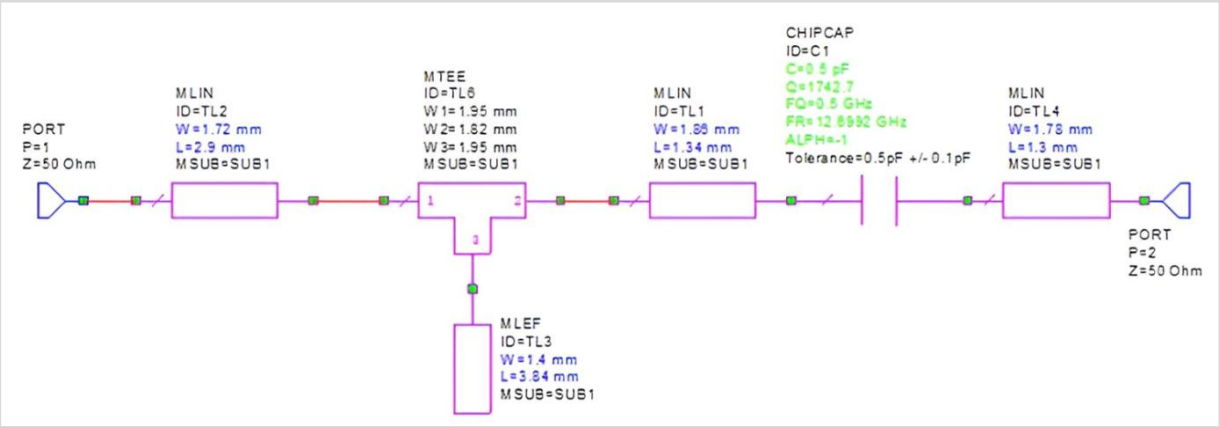


Fig. 6. DRO matching circuit.

The oscillator to converge properly demands that the real part of the input impedance be negative and the imaginary part have sharp variation at the desired operating frequency. The generated layout of DRO incorporates practical considerations such as jumpers, pads, vias, tees, etc. EM simulation was carried out in AXIEM EM simulator of Microwave office, to account for coupling among various microstrip lines. The circuit is further optimized for

several iterations to compensate for the coupling effect and losses. The prototype layout of DRO arrived after carrying out nonlinear EM analysis as shown in Fig. 7.

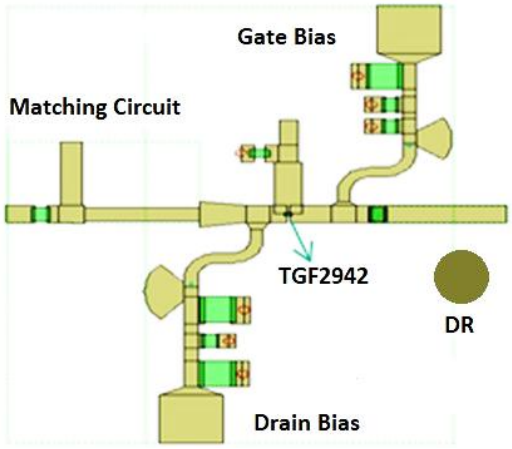


Fig. 7. DRO layout.

The simulation results (Fig. 8) show a phase noise of -116 dBc /Hz at 100 kHz away from the carrier for open-loop operation, while Fig. 9 shows the output power spectrum.

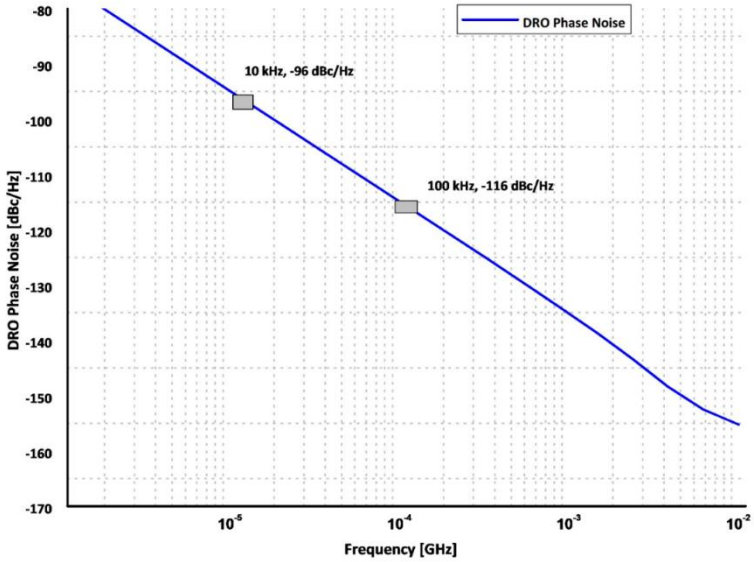


Fig. 8. DRO phase noise.

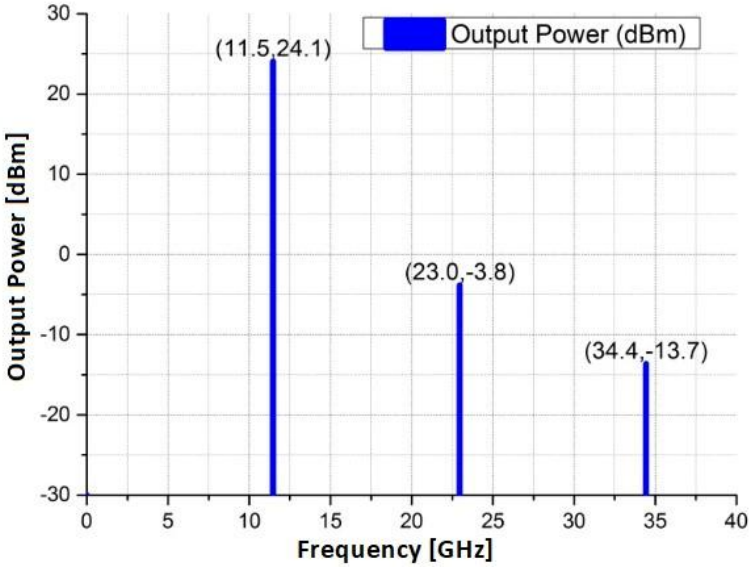


Fig. 9. DRO output power.

The fundamental output power of 24 dBm (220 mW) was obtained at 11.5 GHz. The device was initially tuned to a lower frequency than desirable, as the actual frequency would change due to the metal enclosure and tuning screw. The harmonics were observed to be more than 27 dBc below the fundamental frequency.

Choosing the dimensions of packaging is very important in order to avoid unwanted modes. The non-ideal characteristics of DRO such as thermal noise, flicker noise, and manufacturing variances may contribute to measured phase noise after fabrication.

2.2. SRD Multiplier

The sampling pulses are obtained using SRD in Sampling Phase Detectors (SPD). A frequency multiplier (x10) is used to allow the frequency of 1 GHz at the input of SPD. This reduces the required divider count, thus improving the overall phase noise. Although the SRD preferred in PLL oscillators for harmonic generation and frequency multiplication, there are several limitations, including switching speed, temperature sensitivity, non-linearity, aging effects, power consumption, and circuit complexity. The SRD (MSPD 1012x) was selected owing to its excellent characteristics of low reverse bias capacitance and a very fast voltage reversal (snap-off) at the end of the storage period. The multiplier design is realized using a matching circuit, drive network (impulse generator), and biasing circuit. Decoupling capacitors isolates the SRD from any frequency resonance lower than the input frequency, as shown in Fig. 10.

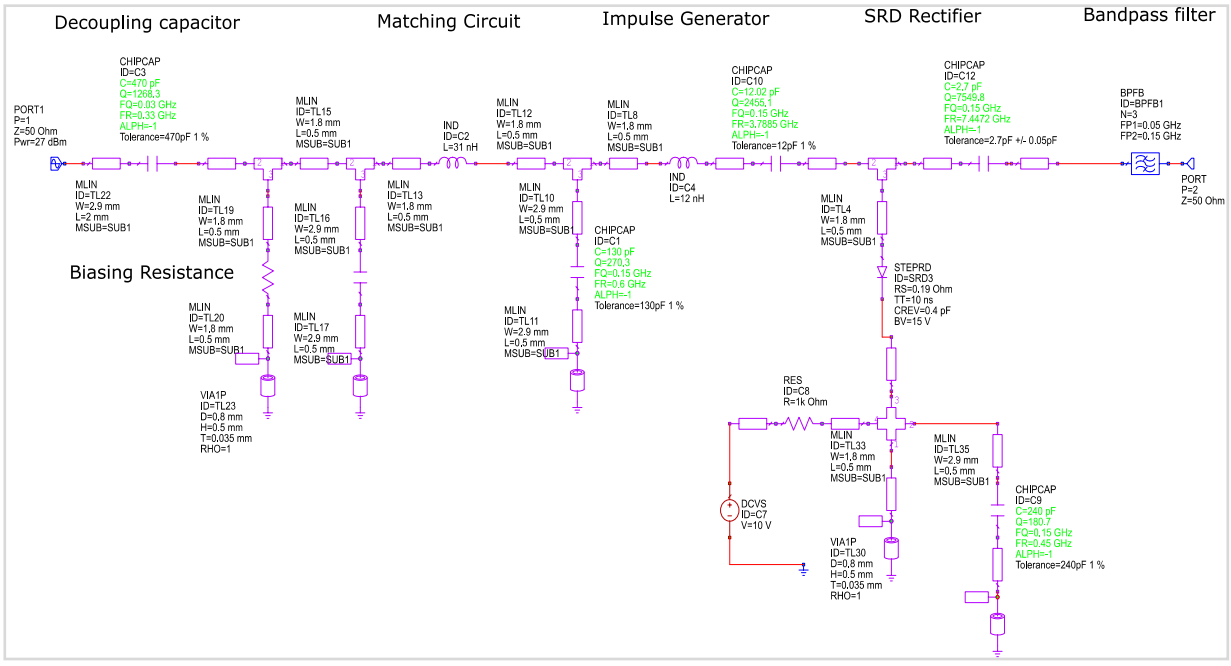


Fig. 10. Circuit of SRD multiplier using realistic components.

Accordingly, the high cut-off frequency of the filter has been chosen at 20 % below the input frequency. In the presence of an RF signal, the SRD rectifies it, thereby generating a bias voltage. The bias resistance was optimized to avoid undesired oscillations and maintain the minimum required power to drive the output. A matching network matches the impedance of SRD to 50 Ω at the desired 10th harmonic frequency (viz., 1 GHz). The RF input forward biases the diode, thereby allowing the conduction of current. During the snap-off time, due to the low reverse capacitance of SRD, the energy stored in the inductor produces a

short-width impulse with a very fast rise time. Such pulses are rich in harmonic content. The circuit was further tuned and optimized such that all harmonic signals up to the 10th harmonic are strong.

The output of the multiplier, terminated with a band-pass filter, suppresses the undesired harmonics. The frequency-domain simulated results shown in Fig. 11 revealed an output power of 8 dBm at the 10th harmonic of the fundamental frequency (1 GHz).

The loop filter reduces higher-order frequencies and harmonics caused by the SRD's nonlinearity. The selection of loop bandwidth and gain has a significant impact on phase noise, spurs, and switching speed of the PLL. In simulations, initial conditions are often idealized, but in the real world, oscillators may exhibit drift or frequency instability, affecting the time required for lock-in. Also the changes in operating temperature, supply voltage, or even aging of components can lead to frequency drifts, which may affect lock-in time and stability after the initial lock. This can be mitigated by adjusting the loop bandwidth of PLL.

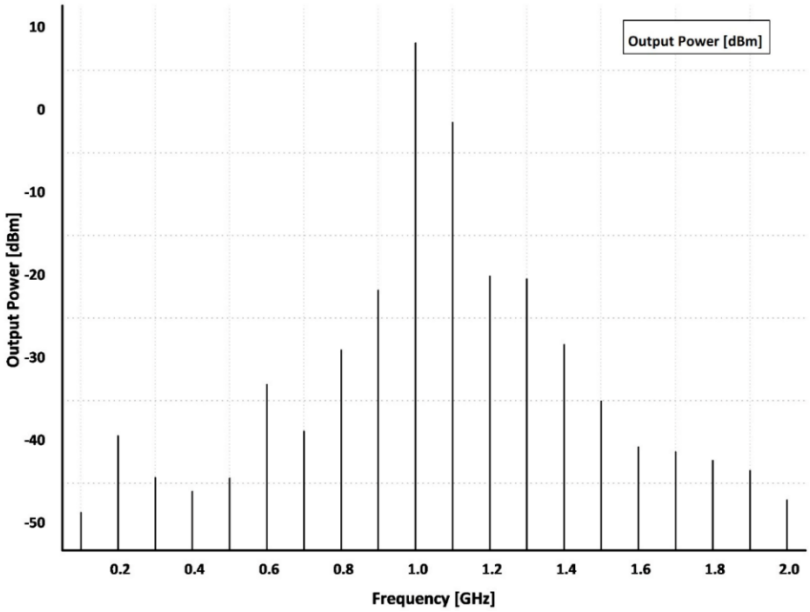


Fig. 11. Power spectrum of the SRD multiplier.

The loop filter bandwidth for optimum phase noise performance is thus equal to the frequency at which DRO phase noise intersects with the total phase noise of all in-band phase noise contributors. However, if the error frequency is higher than the loop bandwidth, it is attenuated by the loop filter, and the error becomes out of lock-in range. Hence, the bandwidth of the filter needs to be tuned such that the error frequency falls within and achieves the lock-in condition. Another important parameter is the phase margin, which is also closely associated with the damping factor. A high value of phase margin or damping factor is desirable, which minimizes the resonant peak near the cut-off frequency of the loop and makes the system more stable. The optimum values of phase margin correspond to the frequency point where the open-loop transfer function (magnitude) of PLL passes through the 0-dB axis. The noise that affects the phase-locked loop output phase noise comes mainly from the noise introduced by the reference source and the noise introduced by the DRO. The open loop transfer function can be determined using Eq. (8) based on the phase-frequency detector (PFD) gain factor (K_ϕ), voltage-controlled sensitivity of DRO (*KDRO*), and divider

count (N). An integration factor of $1/s$ is due to the presence of DRO in PLL [19]. Here *F(S)* is the closed loop transfer function of the loop filter.

$$L(S) = \frac{K_\phi 2\pi K_{DRO} F(S)}{Ns} \quad (8)$$

The phase noise values of various components, such as the PFD, reference oscillator, and frequency divider, are referred to from the datasheet and modelled in the ADIsimPLL software. Fig. 12 represents the total phase noise along with the free-running noise of integrated components. The amplitude curve in Fig. 13 passes through the 0 dB axis at the 230 kHz offset frequency.

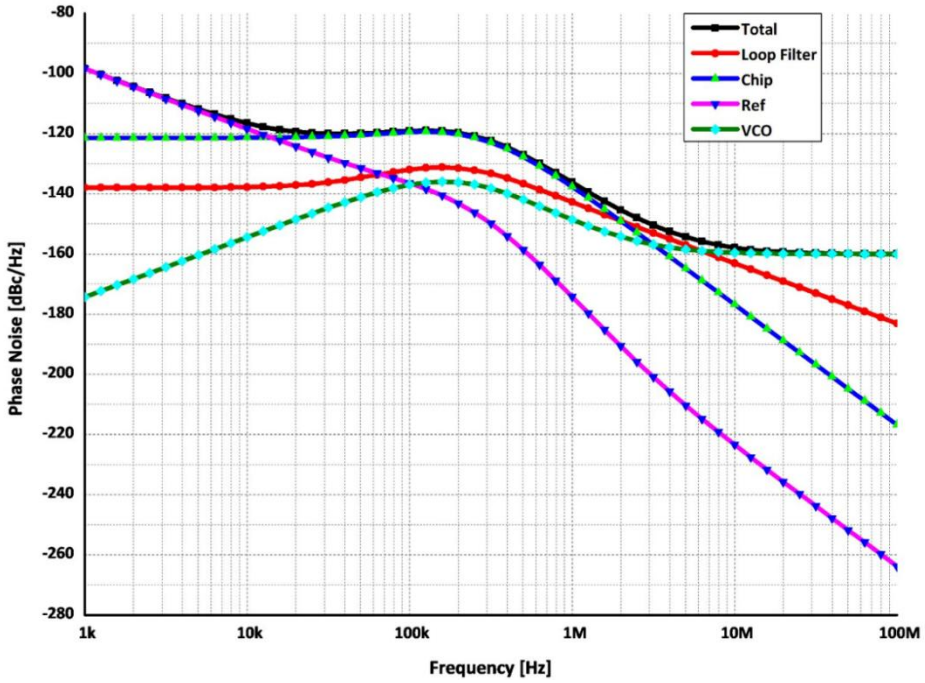


Fig. 12 Phase noise of PLDRO components.

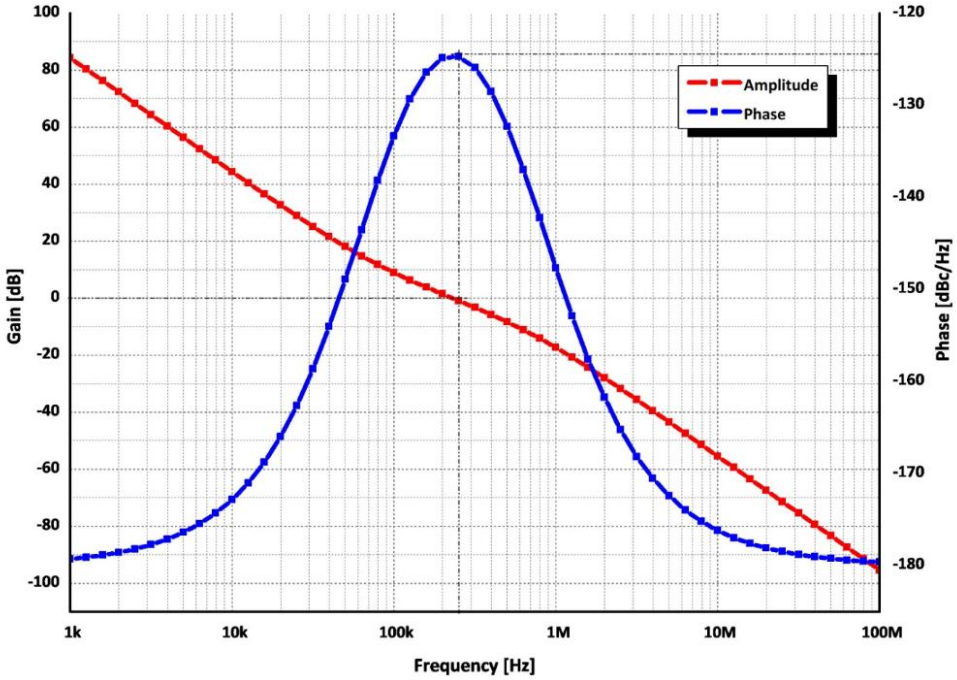


Fig. 13. Open loop gain and phase of active loop filter.

The phase angle that corresponds to the given frequency was found to be 125◦. Thus, the phase margin was calculated as 55◦, which can be optimized further to achieve the minimum peak at the cut-off frequency. The final schematic derived using the selected values of loop bandwidth and phase margin is shown in Fig. 14.

3. INTEGRATED PL-DRO SYSTEM

The designed components are then integrated into a system (Fig. 14). The reference crystal oscillator (O-LU25H) selected from NEL frequency controls has a stable frequency of 100 MHz and phase noise of -160 dBc/Hz at 10 kHz offset. The inclusion of the frequency multiplier using SRD imposes an additional degradation of 20 $\log_{10}(N)$ in the total phase noise, which has been considered while integrating the components. However, it is negligible over the noise degradation due to the frequency divider that would be introduced in the absence of a multiplier.

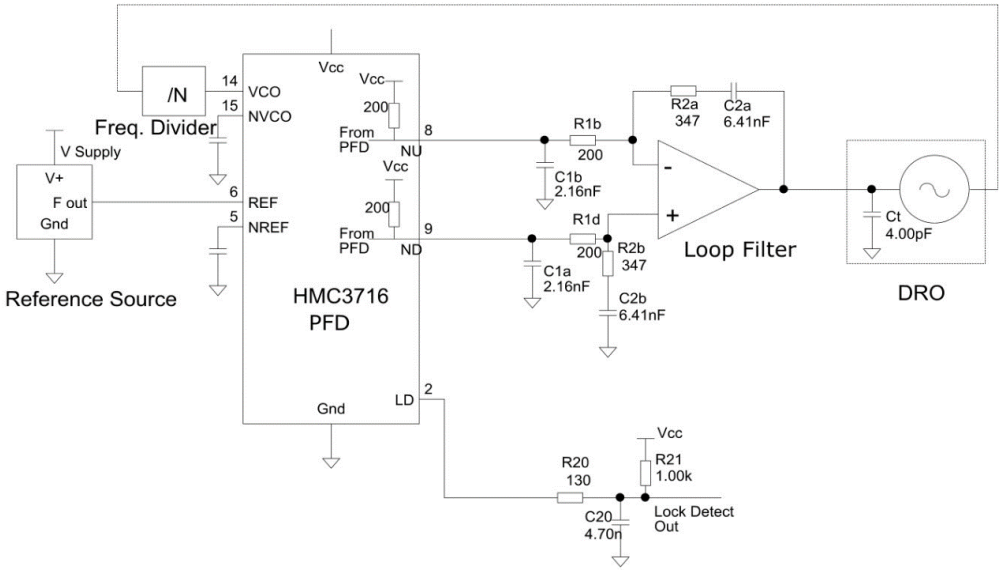
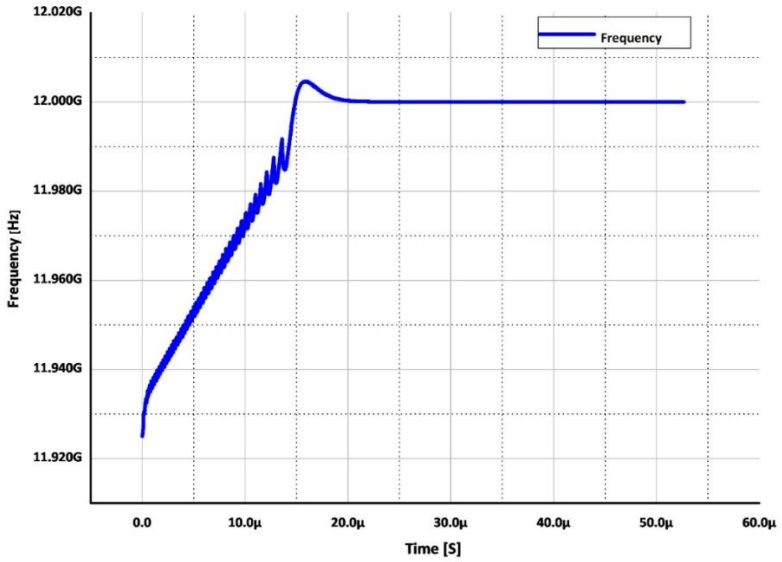


Fig. 14. Integrated schematic of PL-DRO.

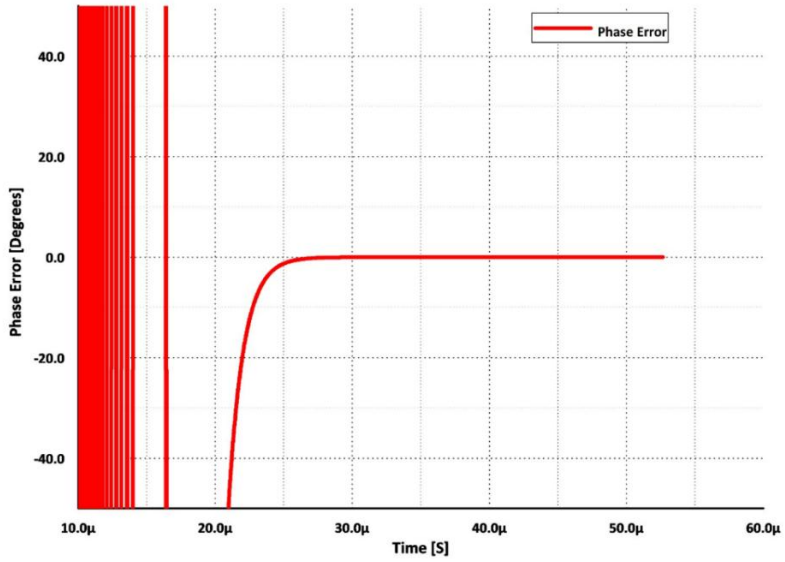
HMC3716LP4E from Analog Devices was selected as a PFD on account of its high phase-detection frequency up to 1300 MHz and very low phase noise of -153 dBc/Hz at 10 kHz offset frequency. The frequency fed back from DRO is divided by 12 (N = 12), which is then compared to the multiplier frequency (1 GHz). It can be achieved using an external divider, PE88D12000; since there is no inbuilt divider present inside the phase discriminator. It has been chosen since it has a low phase noise of -145 dBc/Hz (100 kHz offset), operates over a wide output frequency range from 8 MHz to 1.08 GHz, and supports a divide ratio of 12. It has been observed that the overall phase noise of PLDRO is -119 dBc /Hz at 100 kHz offset. Fig. 15a depicts the amount of time required to lock to frequency (1 kHz) as 26.3 μS, while Fig. 15b reveals the amount of time required to lock to phase (10◦) as 22.7 μS. The proposed scheme is then re-simulated for a reference frequency of 10 MHz.

Table 1 compares the performance of the proposed GaN based-PLDRO with that for the reference frequency of 100 MHz and conventional DPLL (without multiplier). The proposed design with a reference frequency of 100 MHz in Fig. 16 depicts significant results at the higher offset frequencies. This work is then compared with the state-of-the-art

published PL-DROs as shown in Table 2. The design is thus the most compact, low-cost, and efficient as compared to the existing literature.



(a)



(b)

Fig. 15. Lock-in time of PL-DRO: a) frequency; b) phase.

Table 1. Comparative performance analysis of PL-DRO and conventional DPLL (without multiplier)

Parameter	Desired		Digital PLL (ref. freq.-100 MHz)	SRD-PLDRO	
				Ref. freq. (10 MHz)	Ref. freq. (100 MHz)
Total phase noise [dBc/Hz]	100	-70	-77.78	-81.66	-78.42
	1 k	-95	-94.24	-95.56	-98.39
	10 k	-100	-105.4	-105.4	-116.6
	100 k	-110	-110.1	-110	-119.1
	1000 k	-130	-119.2	-139.6	-136.2
Time to lock to frequency		-	13.9 uS	33.4 uS	26.3 uS
Time to lock to phase		-	11.7 uS	26.7 uS	22.7 uS
Limitation			N = 120 (High phase noise at higher offset freq.)	N = 120 (Expensive)	N = 12 (needs external divider)

The design upon fabrication may lead to potential degradation in terms of phase noise, output power, lock-in time, stability, etc. Thus, use of high-quality components, temperature control, power supply filtering, mechanical isolation, and advanced PLL algorithms can mitigate these challenges, ensuring that the DRO performs as close to its simulated ideal as possible in realistic conditions. Understanding and addressing these practical challenges is crucial for achieving robust and reliable performance in RF systems.

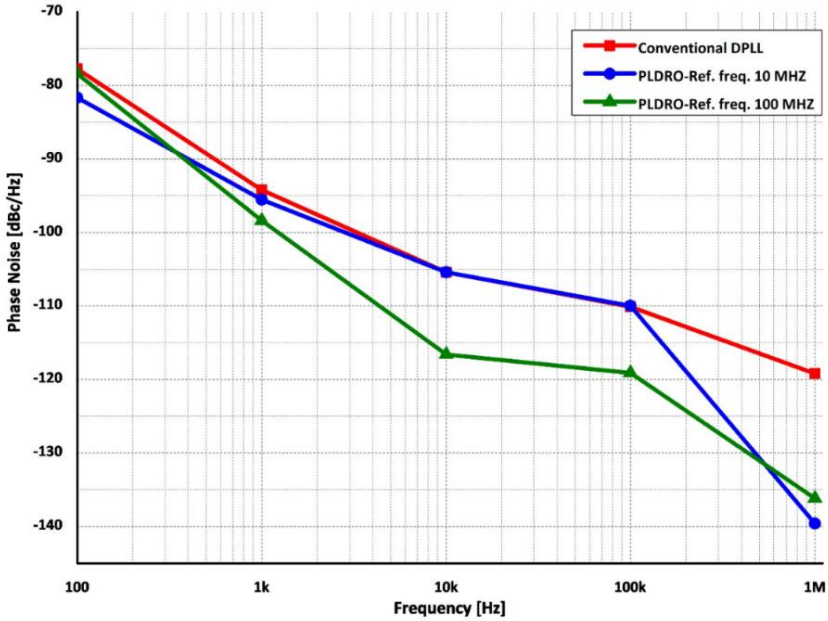


Fig. 16. Phase noise of conventional DPLL and PL-DRO (ref. freq. 10 MHz and 100 MHz).

Table 2. Comparative analysis between the proposed and the state-of-the-art PL-DRO (simulation results).

Ref.	[9]	[20]	[6]	[21]	[7]	[10]	This work
Device type	GaAs FET	HMIC	GaAs FET	GaAs FET	GaN HEMT	GaAs HEMT	GaN HEMT
PLL type	APLL	APLL	APLL	DPLL	APLL	APLL	SRD-PLL
Input ref. freq [MHz]	100	-	-	10	100	100	100
Output freq [GHz]	37	10	11.5	19.25	11	2.45	12
Spur level [dBc]	-	-	>-80	>-60	-	-	>-85
Phase noise [dBc/Hz]	-82 (@100 kHz) (measured)	-112.6 (@100 kHz) (simulated)	-111.3 (@10 kHz) -112(@100 kHz) (measured)	-106 (@100 kHz) (simulated)	-100 (@10kHz) (simulated)	-107 (@100 kHz) (measured)	-116 (@ 10 kHz) -119(@ 100 kHz) (simulated)

4. CONCLUSIONS

A GaN-based PLDRO was designed to cater to the required phase noise specifications for microwave systems. Several constituent designs of PLDRO have been investigated, and optimum results are presented. The proposed design signifies an ultra-low phase noise performance of -119 dBc / Hz at a 100 kHz offset frequency. Implementation of an oscillator using a GaN device has led to a significantly high amount of power. This has eliminated the requirement for an additional amplifier to drive the subsequent stages. Insertion of a frequency multiplier in the preceding stages of PFD has reduced the divider count in the

feedback loop of PLL. Thus, the proposed design enables it to be a suitable candidate for strategic use.

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