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A Novel 49-Level Inverter Topology with Reduced Component Count and Total Standing Voltage for PV Energy Systems

Muhammad Najwan Hamidi[1*], Dahaman Ishak[2]

[1, 2] School of Electrical and Electronic Engineering, Universiti Sains Malaysia, 14300 Nibong Tebal, Malaysia
E-mail: najwan@usm.my

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***Abstract*—** This paper introduces a novel 49 Level (49-L) inverter topology designed to overcome the limitations of traditional inverters in photovoltaic (PV) renewable energy systems. This design focuses on minimizing component count and total standing voltage (TSV) at high output levels, making it versatile for various applications. The proposed inverter incorporates a modified packed H-Bridge unit and basic units to optimize component usage and reduce switch voltage stress. Mathematical formulations for calculating switching angles are provided, simplifying switching signal generation and reducing processing requirements. The 49-level inverter undergoes rigorous testing under different load conditions, with analysis emphasizing key performance metrics such as total harmonic distortion (THD), switch voltage stress, TSV, and efficiency. Its suitability for PV system integration - particularly in standalone systems - is demonstrated, highlighting its potential for renewable energy applications. The obtained results unveil that the proposed inverter achieves low THD for voltage and current, meeting IEEE 519 standards. The voltage THD is found to be at the value of 1.66% under all loads. The current THD is found to be at 1.66% under resistive load and ranges from 0.11% to 0.14% under RL loads. Moreover, the inverter's efficiency - depending on load conditions - is found to range from 96% to 98%. Additionally, the proposed inverter performs well under dynamic conditions, with smooth transitions during changes in irradiation levels and load types. Furthermore, this topology is the most cost-effective compared to other recent multilevel inverter (MLI) designs. Finally, the proposed 49-level inverter offers a promising solution for PV renewable energy systems, delivering high power quality, efficiency, and flexibility.

***Keywords*—** Multilevel inverter; PV system; Asymmetrical sources; Total harmonic distortion; Total standing voltage.

Nomenclature

α	Weight Coefficient	Pf	Power Factor
θ	Switching Angle	POVR	Perturb & Observe-based Voltage Regulator
CF	Cost Function	PV	Photovoltaic
CHB	Cascaded H-Bridge	PWM	Pulse Width Modulation
FC	Flying Capacitor	$S_{Cn,n}$, $S_{Ln,n}$, $S_{Rn,n}$	Power Switch
I_{max}	Output Current Magnitude	THD	Total Harmonic Distortion
I_S	Switch Current	TSV	Total Standing Voltage
k	Switching Angle Position	TT-MLI	T-Type Multilevel Inverter
MLI	Multilevel Inverter	V_{DC}	Base DC Voltage Value
N_{DC}	Number of DC Sources	$V_{Ln,n}$, $V_{Rn,n}$	Voltage Source Magnitude
N_G	Number of Gate Drivers	Vmax	Output Voltage Magnitude
N_L	Number of Output Levels	$\boldsymbol{V_{S_{Ln}}, V_{S_{Rn}}, V_{S_{Cn}}}$	Switch Blocking Voltage
NPC	Neutral Point Clamped	V_{out}	Output Voltage
N_{SW}	Number of Switches		

* Corresponding author

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1. INTRODUCTION

Power electronics converters are essential components in PV renewable energy systems. Inverters, which convert DC input to AC output, are crucial for numerous home and industrial applications such as motor drivers, electric vehicles, and standalone power systems. Traditional two-level inverters produce AC output with identical peak values on both positive and negative cycles but have several drawbacks, including high electromagnetic interference, voltage stress on power devices, increased losses, high THD, restricted DC bus utilization, and significant filtering requirements [1-3]. In contrast, MLIs offer superior output power quality and have emerged as a better alternative. However, traditional MLIs also have their limitations. They typically require a higher number of components, such as power switches, particularly at higher output levels [4]. This increase in switches leads to more driving circuits, making the implementation of MLIs more complex and expensive [5].

Numerous MLI topologies have been proposed to minimize component count and address the issue of excessive switch voltage stress often seen in traditional designs. Many of these novel MLI structures incorporate an H-Bridge for polarity generation, yet this method often leads to significant voltage stress on the switches [6]. A more recent method, the packed H-Bridge, allows for connections on both sides of the bridge, offering a potential solution. Additionally, there are MLI topologies designed without a polarity generator to mitigate switch voltage stress, although these often require a greater number of components [7]. A considerable number of new MLIs employ isolated DC sources, as implementing non-isolated sources like the neutral point clamped (NPC) or flying capacitor (FC) can be difficult at high output levels due to the complexities of capacitor balancing control and the need for numerous capacitors [8]. Asymmetrical sources based MLIs represent a significant advancement within the isolated MLI family. They have gained popularity due to their ability to achieve a higher number of output voltage levels with the same or fewer components compared to symmetrical based MLIs [9]. This results in waveforms with reduced THD, often eliminating the need for passive filters by meeting IEEE 519 standards. Common asymmetrical source selection methods include binary and trinary configurations, although non-universal schemes also exist [10]. The modular nature of many new MLIs, making them easily scalable, further highlights the advantages of asymmetrical sources, which may require half the components of symmetrical sources for the same output quality [11].

Modulation technique is another crucial factor influencing inverter performance, specifically THD and efficiency. Traditional pulse width modulation (PWM) becomes increasingly complex at higher levels, requiring multiple carriers and significant processing power [12]. As an alternative, low switching frequency techniques can be employed, pre-calculating switching angles for optimal waveform accuracy, closely resembling a pure sinusoid [13]. This approach reduces switching losses, potentially improving efficiency. As presented in [3], a 5-Level inverter uses six IGBT switches. The switching frequency of the main inverter is only at 100 Hz, which helps to reduce the switching losses in the main inverter. However, it may also elevate THD due to increased low-order harmonics. Operating a MLI at high output levels can mitigate this issue, generating output waveforms with sufficiently low THD to offset the potential drawbacks of low switching frequency modulation [14].

In addition to inverters, DC-DC converters play a crucial role in PV renewable energy systems. Due to the variable output of renewable sources like PV panels, influenced by factors like solar irradiance, temperature, and weather conditions, DC-DC converters serve as an

interface between these sources and the inverter [15]. They regulate the PV panel output before it is fed to the inverter, often employing techniques like PI control. PI control techniques is also commonly used in hybrid with the more advanced artificial intelligence (AI) based techniques such as Fuzzy logic to achieve improved performance [16]. A recent advancement in DC voltage control for standalone systems is the use of the perturb & observe-based voltage regulator (POVR) [17]. While alternative methods like high-frequency transformer DC-AC-DC converters or additional inverters exist for interfacing PV modules with the inverter [18], DC-DC converters are generally preferred due to their flexibility and ability to harvest solar energy effectively with a wide voltage gain range.

This paper introduces a novel asymmetrical 49-L inverter designed to minimize component count and TSV at high output levels, making it suitable for various applications, including PV renewable energy systems. The inverter employs a modified packed H-Bridge unit alongside newly proposed basic units to optimize component usage and reduce switch voltage stress. Mathematical formulations for calculating switching angles are provided, formulated specifically for the proposed topology. These equations aim to simplify switching signal generation and reduce processing requirements. The 49-L inverter is rigorously tested under different load conditions, with analysis focusing on key performance metrics such as THD, switch voltage stress, TSV, and efficiency. Furthermore, the topology's applicability for PV system integration, particularly in standalone systems, is demonstrated, showcasing its potential for renewable energy applications.

2. SYSTEM MODELLING

2.1. Inverter Topology Structure

Fig. 1 illustrates the general structure of the proposed MLI topology, which comprises three main sections. The central modified packed H-Bridge forms the core, flanked by basic units on both the left and right sides. Each basic unit consists of two isolated DC sources ($V_{L/Rn,1}$ & $V_{L/Rn,2}$), two unidirectional switches ($S_{L/Rn}$, & $S_{L/Rn,\ 3}$), and a single bidirectional switch ($S_{L/Rn,2}$). Adding a basic unit on either side necessitates three additional unidirectional switches where two should be added to the bridge ($S_{C1,n}$ & $S_{C2,n}$ or $S_{C3,n}$ & $S_{C4,n}$) and one at the intersection between basic units ($S_{LI,n}$ or $S_{RI,n}$). The final basic unit on each side does not require this third switch. Notably, the proposed topology allows the voltage sources on the right-side basic units to be subtracted from the voltage sources on the left-side basic units, significantly expanding the range of achievable output levels.

The asymmetrical voltage source configuration proposed for this topology is defined by the ratio in Eq. (1) and the relationship in Eq. (2). For the voltage sources on the left-side basic units, as described by Eq. (1), the source magnitudes follow a binary pattern, with each subsequent voltage source having twice the magnitude of the previous one. For example, if there is one basic unit on the left-side with two DC sources, the first source ($V_{L1,1}$) will have a magnitude of V_{DC}, while the second source ($V_{L1,2}$) will have a magnitude of $2V_{DC}$. In contrast, the configuration of the DC sources on the right-side basic unit follows the relationship given in Eq. (2). Specifically, the first DC source on the right side ($V_{R1,1}$) will always have a magnitude equal to two times the sum of all DC sources on the left side, plus 1. Subsequent sources on the right side will also follow the binary pattern. For instance, with one basic unit on each side - comprising two DC sources on both the left and right sides—the left-side sources will have

magnitudes of V_{DC} and $2V_{DC}$, as previously described. The first source on the right-side ($V_{R1,1}$) will then have a magnitude of $[2(V_{DC}+2V_{DC})+1]$ which is equal to $7V_{DC}$. The second source on the right-side ($V_{R1,2}$) will follow the binary pattern, having double the magnitude, resulting in $14V_{DC}$.

$$V_{L1,1}:V_{L1,2}:V_{L2,1}:V_{L2,2}:V_{Ln,n} = V_{DC}:2V_{DC}:4V_{DC}:8V_{DC}:\left(2^{i-1}\right)V_{DC} \quad where\ i = 1,2,3,\ldots \tag{1}$$

$$V_{Rn,n} = \left(2^{i-1}\right)\left[2\left(\sum V_{Rn,1} + \sum V_{Rn,2}\right) + 1\right]V_{DC} \quad where\ i = 1,2,3,\ldots \tag{2}$$

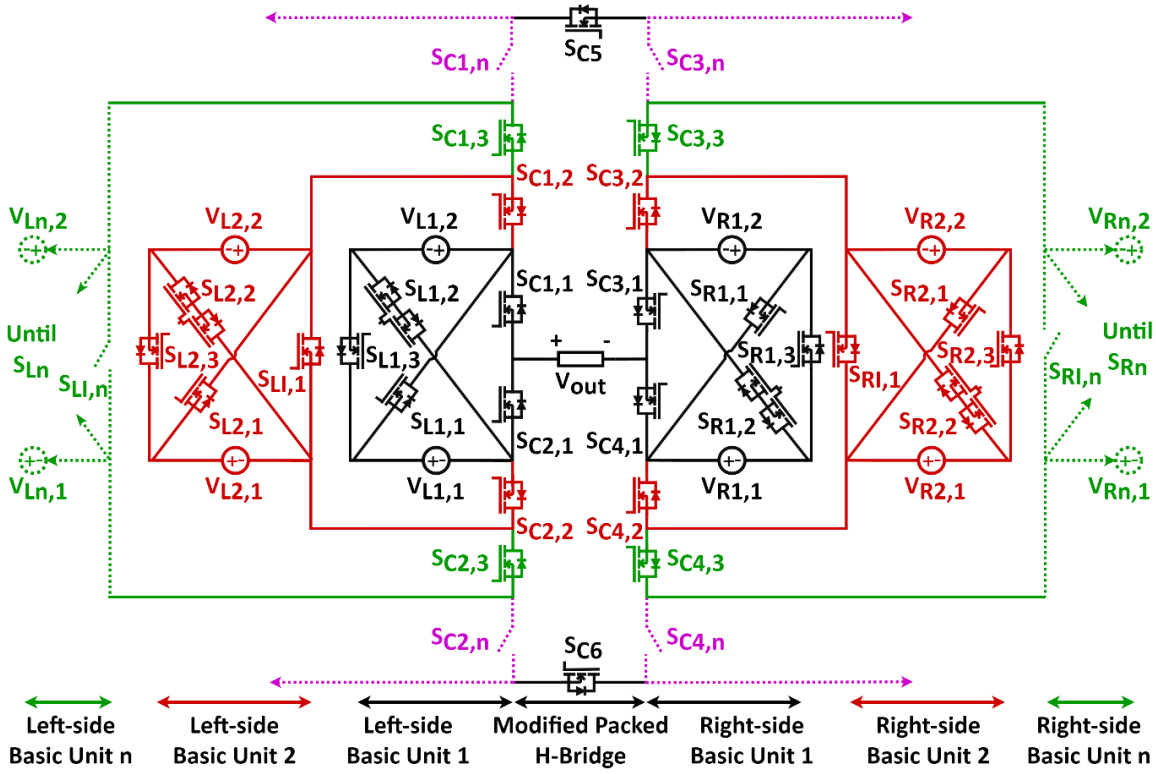

Fig. 1. General structure of the proposed topology.

Based on the general structure of the topology and the proposed asymmetrical voltage source configuration, the number of switching devices (N_{SW}), gate drivers (N_G), DC sources (N_{DC}), output levels (N_L) and the maximum magnitude of output voltage (V_{max}) can be determined as follows:

$$N_{SW} = 8 + \frac{5m-4}{2} \tag{3}$$

$$N_G = 2m + 6 \tag{4}$$

$$N_L = 2\left(2^{1+m} - 2^{1+\frac{m}{2}}\right) + 1 \tag{5}$$

$$V_{max} = \sum_{n=1}^{\infty}(V_{Ln,1} + V_{Ln,2} + V_{Rn,1} + V_{Rn,2}) \tag{6}$$

This work proposes the topology to be operated at 49-L, following the previously given example. In this configuration, the left-side basic unit contains two DC sources with magnitudes of V_{DC} and $2V_{DC}$, while the right-side basic unit contains two DC sources with magnitudes of $7V_{DC}$ and $14V_{DC}$. This number is chosen as it offers a balance between a high number of levels and a reasonable component count. The topology's design requires only two basic units to achieve the 49-L output. Specifically, this design utilizes 4 N_{DC}, 16 N_{SW}, and 14 N_G. While the topology can technically function with various voltage source configurations in

addition to Eq. (1), including symmetrical, alternative trinary, and binary configurations, these configurations can only generate 9-L, 17-L, and 31-L, respectively. Therefore, 49-L represents the maximum number of levels that can be generated by this topology with the same number of components.

Table 1 outlines the switching states for this configuration, designed to enable voltage source addition within and across basic units. This formulation also allows for the subtraction of left-side basic unit voltage sources from those on the right-side basic units. Fig. 2 provides illustrative examples of some of these switching combinations. Specifically, Fig. 2 (a) depicts the additive magnitudes of the DC sources on the left-side basic unit. Fig. 2 (b) illustrates the utilization of the DC source on a right-side basic unit. Fig. 2 (c) shows how the DC source from the left-side basic unit can be subtracted from the DC source on the right-side basic unit, while Fig. 2 (d) demonstrates how the DC source on the left-side basic unit can be added to that of the right-side basic unit. Additionally, Fig. 2 (e) through Fig. 2 (h) represent the same combinations as Fig. 2 (a) to Fig. 2 (d) but for the generation of the negative levels.

Table 1. Switching states of the proposed 49-L inverter.

V_{out}	ON Switches	V_{out}	ON Switches	V_{out}	ON Switches
0	$S_{C2,1};S_{C4};S_{C2,2};S_{C6}$	17	$S_{C1,1};S_{C3};S_{C2,2};S_{C6};S_{L3};S_{R2}$	-9	$S_{C2,1};S_{C4};S_{C1,2};S_{C5};S_{L2};S_{R1}$
1	$S_{C1,1};S_{C4};S_{C2,2};S_{C6};S_{L1}$	18	$S_{C2,1};S_{C3};S_{C1,2};S_{C6};S_{L3};S_{R3}$	-10	$S_{C2,1};S_{C4};S_{C1,2};S_{C5};S_{L3};S_{R1}$
2	$S_{C1,1};S_{C4};S_{C2,2};S_{C6};S_{L2}$	19	$S_{C2,1};S_{C3};S_{C1,2};S_{C6};S_{L2};S_{R3}$	-11	$S_{C1,1};S_{C4};S_{C2,2};S_{C5};S_{L3};S_{R2}$
3	$S_{C1,1};S_{C4};S_{C2,2};S_{C6};S_{L3}$	20	$S_{C2,1};S_{C1,2};S_{C6};S_{L1};S_{R3}$	-12	$S_{C1,1};S_{C4};S_{C2,2};S_{L2};S_{R2}$
4	$S_{C2,1};S_{C3};S_{C1,2};S_{C6};S_{L3};S_{R1}$	21	$S_{C2,1};S_{C3};S_{C2,2};S_{C6};S_{R3}$	-13	$S_{C1,1};S_{C4};S_{C2,2};S_{C5};S_{L1};S_{R2}$
5	$S_{C2,1};S_{C3};S_{C1,2};S_{C6};S_{L2};S_{R1}$	22	$S_{C1,1};S_{C3};S_{C2,2};S_{C6};S_{L1};S_{R3}$	-14	$S_{C1,1};S_{C4};S_{C1,2};S_{C5};S_{R2}$
6	$S_{C2,1};S_{C3};S_{C1,2};S_{C6};S_{L1};S_{R1}$	23	$S_{C1,1};S_{C3};S_{C2,2};S_{C6};S_{L2};S_{R3}$	-15	$S_{C2,1};S_{C4};S_{C1,2};S_{C5};S_{L1};S_{R2}$
7	$S_{C2,1};S_{C3};S_{C2,2};S_{C6};S_{R1}$	24	$S_{C1,1};S_{C3};S_{C2,2};S_{C6};S_{L3};S_{R3}$	-16	$S_{C2,1};S_{C4};S_{C1,2};S_{C5};S_{L2};S_{R2}$
8	$S_{C1,1};S_{C3};S_{C2,2};S_{C6};S_{L1};S_{R1}$	0	$S_{C1,1};S_{C3};S_{C1,2};S_{C5}$	-17	$S_{C2,1};S_{C4};S_{C1,2};S_{C5};S_{L3};S_{R2}$
9	$S_{C1,1};S_{C3};S_{C2,2};S_{C6};S_{L2};S_{R1}$	-1	$S_{C2,1};S_{C3};S_{C1,2};S_{C5};S_{L1}$	-18	$S_{C1,1};S_{C4};S_{C2,2};S_{C5};S_{L3};S_{R3}$
10	$S_{C1,1};S_{C3};S_{C2,2};S_{C6};S_{L3};S_{R1}$	-2	$S_{C2,1};S_{C3};S_{C1,2};S_{C5};S_{L2}$	-19	$S_{C1,1};S_{C4};S_{C2,2};S_{C5};S_{L2};S_{R3}$
11	$S_{C2,1};S_{C3};S_{C1,2};S_{C6};S_{L3};S_{R2}$	-3	$S_{C2,1};S_{C3};S_{C1,2};S_{C5};S_{L3}$	-20	$S_{C1,1};S_{C4};S_{C2,2};S_{C5};S_{L1};S_{R3}$
12	$S_{C2,1};S_{C3};S_{C1,2};S_{C6};S_{L2};S_{R2}$	-4	$S_{C1,1};S_{C4};S_{C2,2};S_{C5};S_{L3};S_{R1}$	-21	$S_{C1,1};S_{C4};S_{C1,2};S_{C5};S_{R3}$
13	$S_{C2,1};S_{C3};S_{C1,2};S_{C6};S_{L1};S_{R2}$	-5	$S_{C1,1};S_{C4};S_{C2,2};S_{C5};S_{L2};S_{R1}$	-22	$S_{C2,1};S_{C4};S_{C1,2};S_{C5};S_{L1};S_{R3}$
14	$S_{C2,1};S_{C3};S_{C2,2};S_{C6};S_{R2}$	-6	$S_{C1,1};S_{C4};S_{C2,2};S_{C5};S_{L1};S_{R1}$	-23	$S_{C2,1};S_{C4};S_{C1,2};S_{C5};S_{L2};S_{R3}$
15	$S_{C1,1};S_{C3};S_{C2,2};S_{C6};S_{L1};S_{R2}$	-7	$S_{C1,1};S_{C4};S_{C1,2};S_{C5};S_{R1}$	-24	$S_{C2,1};S_{C4};S_{C1,2};S_{C5};S_{L3};S_{R3}$
16	$S_{C1,1};S_{C3};S_{C2,2};S_{C6};S_{L2};S_{R2}$	-8	$S_{C2,1};S_{C4};S_{C1,2};S_{C5};S_{L1};S_{R1}$		

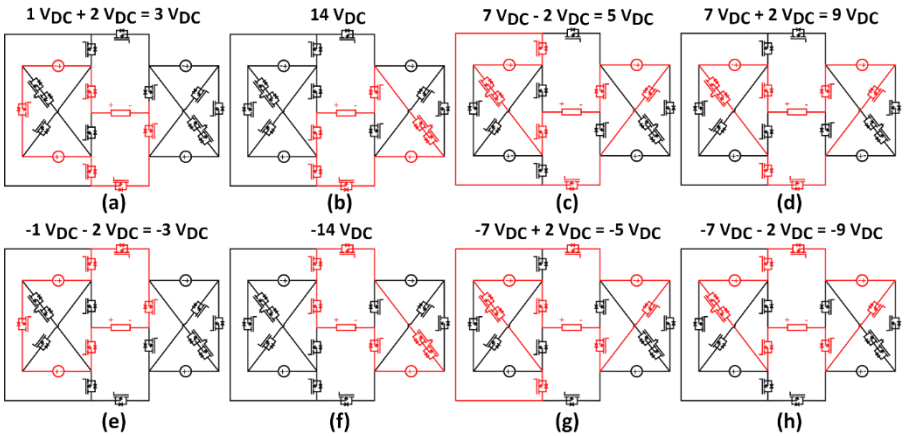

Fig. 2. Example of several selected switching states showcasing the topology's ability to have additive and subtractive voltage source combinations.

2.2. Blocking Voltage and Maximum Current

A critical design consideration is the blocking voltage of the switches, which guides the selection of appropriately rated components. As for the proposed 49-L inverter, the blocking voltages for the switches of the basic units can be expressed as

$$V_{S_{L1}} = V_{S_{L3}} = 2V_{DC} \quad (7)$$

$$V_{S_{L2}} = V_{DC} \quad (8)$$

$$V_{S_{R1}} = V_{S_{R3}} = 14V_{DC} \quad (9)$$

$$V_{S_{R2}} = 7V_{DC} \quad (10)$$

Conversely, the blocking voltages of the switches at the central bridge are as follows

$$\mathrm{V_{S_{C1,1}}} = \mathrm{V_{S_{C2,1}}} = \mathrm{V_{S_{C1,2}}} = \mathrm{V_{S_{C2,2}}} = 3\mathrm{V_{DC}} \quad (11)$$

$$\mathrm{V_{S_{C3}}} = \mathrm{V_{S_{C4}}} = \mathrm{V_{S_{C5}}} = \mathrm{V_{S_{C6}}} = 21\mathrm{V_{DC}} \quad (12)$$

After determining the blocking voltage of each switch, the TSV of the entire 49-L inverter configuration is calculated by adding together these individual switch voltages and is given as follows

$$TSV = 136V_{DC} \quad (13)$$

Differently, the maximum current flowing through the switches while conducting is equivalent to the peak load current. When turned off, the current through the switches drops to zero. Consequently, determining the suitable current rating for these switches is straightforward, requiring only knowledge of the peak load current (I_{max}). The maximum current for each switch is as follows

$$I_{S_{Cn}} = I_{S_{Ln}} = I_{S_{Rn}} = I_{max} \quad (14)$$

2.3. Switching Strategy

The high number of output levels in this topology renders standard PWM techniques like sinusoidal PWM (SPWM) impractical, as they necessitate numerous carrier signals. This, in turn, demands increased processing power and additional components, ultimately driving up implementation costs [12]. Instead, a more efficient approach is to control the switches using pre-calculated switching angles. Mathematical formulations for these angles, specifically derived for this MLI topology and building upon techniques from [19, 20], are employed. The objective is to generate a multilevel output that closely approximates a pure sinusoid, effectively minimizing the THD of the AC voltage and current output. Referring to the switching states in Table 1, the calculation of the switching angles can be performed through the utilization of the following equations

$$\theta_k = sin^{-1}\left[\frac{1}{N_L-1}(2k-1)\right] \quad for\ k = 1, 2, \ldots \frac{N_L-1}{2} \quad (15)$$

$$\theta_k = 180 - sin^{-1}\left[\frac{1}{N_L-1}(2k-1)\right]\ for\ k = \frac{N_L-1}{2}, \ldots, 2, 1 \quad (16)$$

$$\theta_{N_L} = 180° \quad (17)$$

$$\theta_j = 360 - \theta_k \quad for\ k = N_L - 1, \ldots, 2, 1 \quad (18)$$

where N_L represents the total number of output voltage levels produced by the MLI, θ_k denotes the switching angle positions for the first half of the levels (up to N_L-1), and θ_j signifies the switching angle positions for the second half of the levels (from N_L+1 up to $2N_L$-1). Fig. 3 illustrates the theoretical 49-L output, derived using Eq. (15) through Eq. (18) and the respective

switching angle patterns. The switching patterns are formulated based on the switching states presented in Table 1.

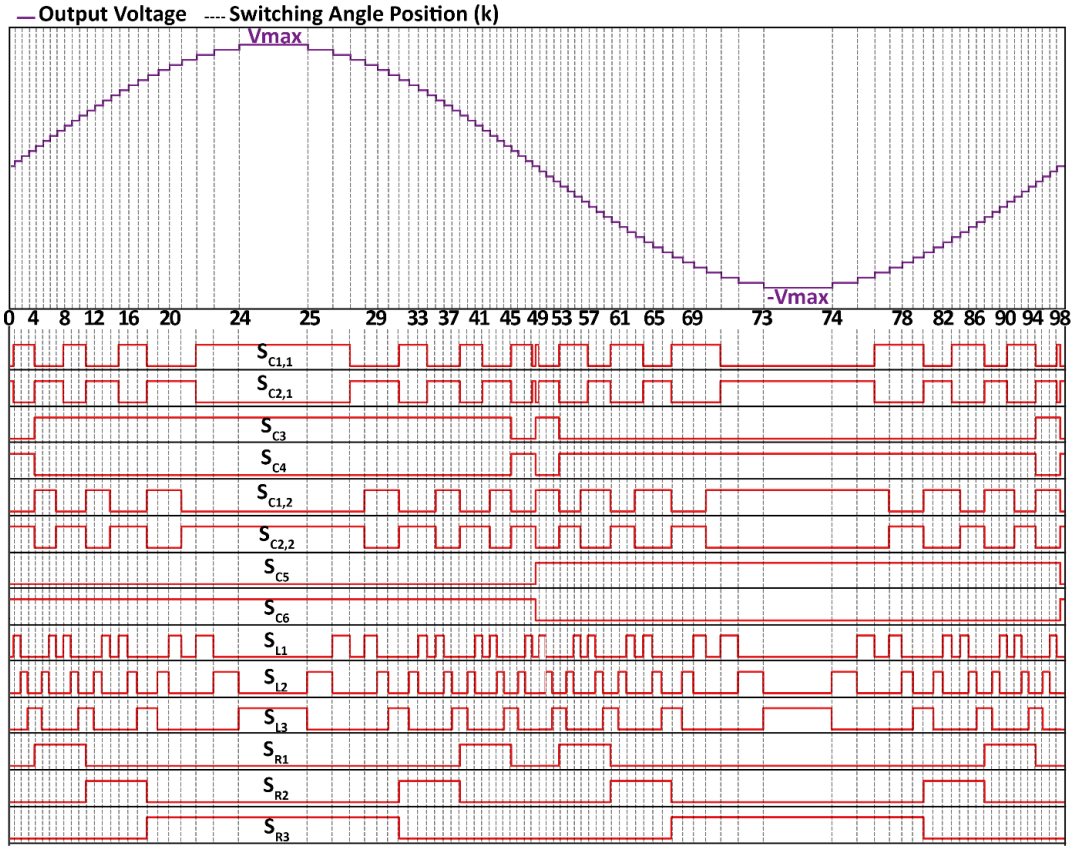

Fig. 3. Switching angle positions and the generated switching signals.

Eq. (15) is used to calculate the switching angles from the initial first level at k=1 up to the first maximum level at k = 24, as illustrated in Fig. 3 for the positive half-cycle. The sine term is employed to ensure that the angles align with a pure sinusoidal waveform, corresponding to the number of levels. As the number of levels increases, more switching angle points are patterned along the sinusoidal waveform. In this case, the term $(\frac{N_L-1}{2})$ in Eq. (15) corresponds to the value of k up to k = 24. For the remaining switching angles in the positive half-cycle, from k=25 to k=48, Eq. (16) is applied. This equation calculates each angle as 180° (angle of a full half-cycle) minus the corresponding switching angles obtained from Eq. (15), maintaining a similar pattern. At the midpoint of the two half-cycles, which occurs at k=49, the angle is 180°, as indicated in Eq. (17). Finally, all switching angles for the negative half-cycle can be determined by subtracting the angles obtained for the positive half-cycle from 360°, since the angle patterns for both cycles are analogous.

2.4. PV System Integration

As briefly mentioned in the introduction, the proposed 49-L inverter is demonstrated for its potential use in photovoltaic (PV) renewable energy systems. This demonstration involves testing the topology within a two-stage standalone PV system, the general structure of which is illustrated in Fig. 4. The control system from [17] is employed as the DC link control strategy. Four separate PV arrays, each with its own DC-DC converter, supply the four DC sources. The desired V_{max} is 325.27 V, corresponding to an RMS voltage of 230 V. To achieve this, reference voltages of 13.55 V, 27.11 V, 94.87 V, and 189.74 V are supplied to the controllers for the PV

sources V_{L1}, V_{L2}, V_{R2}, and V_{R1}, respectively, based on Eq. (1) and (2). The PV panel model used is the Jinko Solar Co. Ltd JKM200M-60B. A detailed discussion on the number of PV panels needed for each array is presented in the Results chapter.

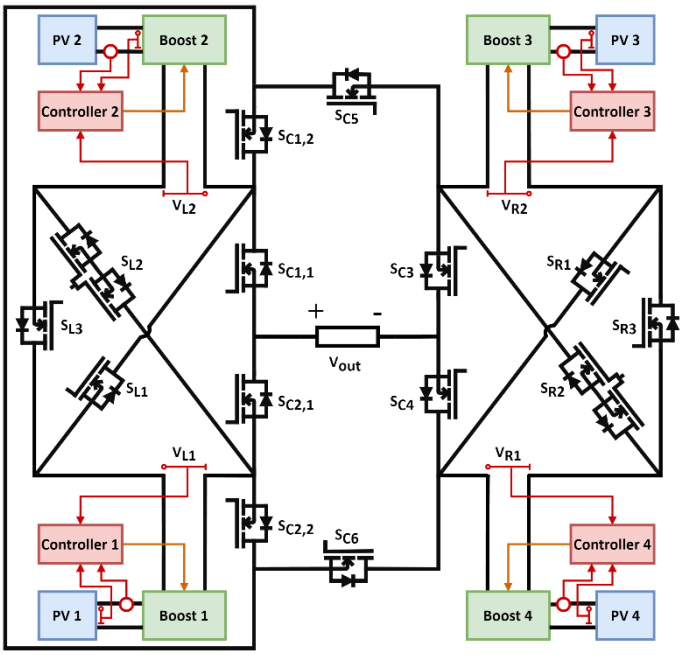

Fig. 4. PV integration of the proposed 49-L inverter.

2.5. Losses and Efficiency

To evaluate the efficiency of the 49-L inverter, it is essential to first analyze the losses, which have a significant impact on the inverter's performance. The two primary sources of these losses are conduction and switching losses in power semiconductor devices. In power electronics systems, either metal-oxide-semiconductor field-effect transistors (MOSFETs) or insulated-gate bipolar transistors (IGBTs) are typically used. In this study, IGBTs are chosen for all power switches. All calculations are based on the equations adapted from [21, 22].

Conduction losses occur when semiconductor devices are fully conducting. One of the most accurate models for IGBT conduction loss utilizes the parabolic interpolation method. Unlike linear approximations, this model fits the characteristic loss curves of any device, which are influenced by operating temperature and can be found in the device's datasheet. The model for IGBT conduction loss is expressed as follows:

$$P_{cond\_IGBT} = V_{ce(sat)} \times I_c \times D \tag{19}$$

where $V_{CE(sat)}$ represents the IGBT collector-emitter saturation voltage, I_C is the collector current, and D is the duty cycle. Unlike conduction loss, switching loss occurs during the transition of a device from its conducting state to its blocking state, and vice versa. The parabolic interpolation method also models the switching losses of IGBTs, which are given by:

$$P_{sw\_on\_IGBT} = E_{on} \times f \times \frac{V_{cc}}{V_{cc\_ds}} \tag{20}$$

$$P_{sw\_off\_IGBT} = E_{off} \times f \times \frac{V_{cc}}{V_{cc\_ds}} \tag{21}$$

where E_{on} is the IGBT turn-on energy loss, E_{off} is the IGBT turn-off energy loss, f_{sw} is the switching frequency, V_{CC} is the measured DC bus voltage, and V_{CC_ds} is the DC bus voltage

specified in the datasheet. Diode losses, which can be modelled similarly to IGBTs, are expressed as follows:

$$P_{cond\_Diode} = V_d \times I_F \times D \quad (22)$$

$$P_{sw\_off\_Diode} = E_{rr} \times f \times \frac{V_R}{V_{R\_ds}} \quad (23)$$

where V_d is the diode voltage drop, I_F is the diode forward current, E_{rr} is the reverse recovery energy loss, V_R is the measured reverse blocking voltage, and V_{R_ds} is the reverse blocking voltage specified in the datasheet. Diode losses are particularly relevant in the boost converter stages where diodes are present, as well as in the freewheeling diode of an IGBT. Therefore, the total loss of a system is the sum of all the conduction and switching losses of the switches.

In this study, efficiency is calculated by considering conduction and switching losses as the primary sources of loss. The overall efficiency can then be determined using the total loss value, as follows:

$$\eta = \frac{P_{in} - \sum P_{cond\_IGBT} - \sum P_{sw\_on\_IGBT} - \sum P_{sw\_off\_IGBT} - \sum P_{cond\_Diode} - \sum P_{sw\_off\_Diode}}{P_{in}} \quad (24)$$

3. TOPOLOGY COMPARISON

To assess the performance of the proposed 49-level inverter, it is thoroughly compared to established topologies found in recent research. The comparison focused solely on asymmetrically isolated source MLIs operated at their intended voltage source configurations. This ensures a fair evaluation.

The first topology compared is the cascaded H-Bridge (CHB) using the binary voltage sequence [23], chosen for its widespread use in various applications. Although typically operated symmetrically, it is adjusted for an asymmetric operation in this work for a fairer comparison. The remaining topologies selected for comparison are all introduced within the last four years. The next topology [24] utilizes a modified H-Bridge for polarity generation, aiming to reduce switch count and TSV. Another topology [25], tackles the challenges of THD and TSV, offering the advantage of operating under both symmetric and asymmetric sources while minimizing circuit devices.

The fourth topology [26], is an extended MLI with high and low voltage modules, expandable to higher voltage levels by adding sources only to the low voltage module. Another topology [27], is a modular single-phase MLI that can be cascaded for higher voltages, using four DC sources and nine switches. The comparison also included a new T-Type MLI (TT-MLI) [28] designed for renewable energy systems, using two asymmetrical DC sources in a 1:3 ratio. The final topology [29], focuses on reducing THD and switching losses.

In the comparison presented in Fig. 5, the proposed 49-level inverter ("T_1") is compared against other topologies identified by their reference numbers. The analysis focuses on the performance at the targeted 49-level output, although plots are drawn at different levels (N_L). In terms of N_{DC}, T_1 is second only to [25] at 49-L, yet it requires the fewest switches (N_{SW}). Regarding N_G, T_1 outperforms other topologies except [24] at the same output level. Considering the total component count (N_{DC}+N_{SW}+N_G), the proposed T_1 is the most efficient among the compared topologies.

The proposed topology T_1 exhibits lower average TSV than topologies [24-26] across all V_{max} values, but higher TSV than [23], [27-29]. To provide a more comprehensive evaluation, the cost function (CF) is analyzed at the targeted 49-L output. The CF, calculated using Eq. (25)

with α (weight coefficient) values of 0.5 and 1.5 [10, 30], is a metric used to assess the overall cost requirements of each topology. Notably, T1 demonstrates the lowest CF under both α values

$$CF = N_{DC} + N_{SW} + N_G + \alpha TSV_{PU} \quad (25)$$

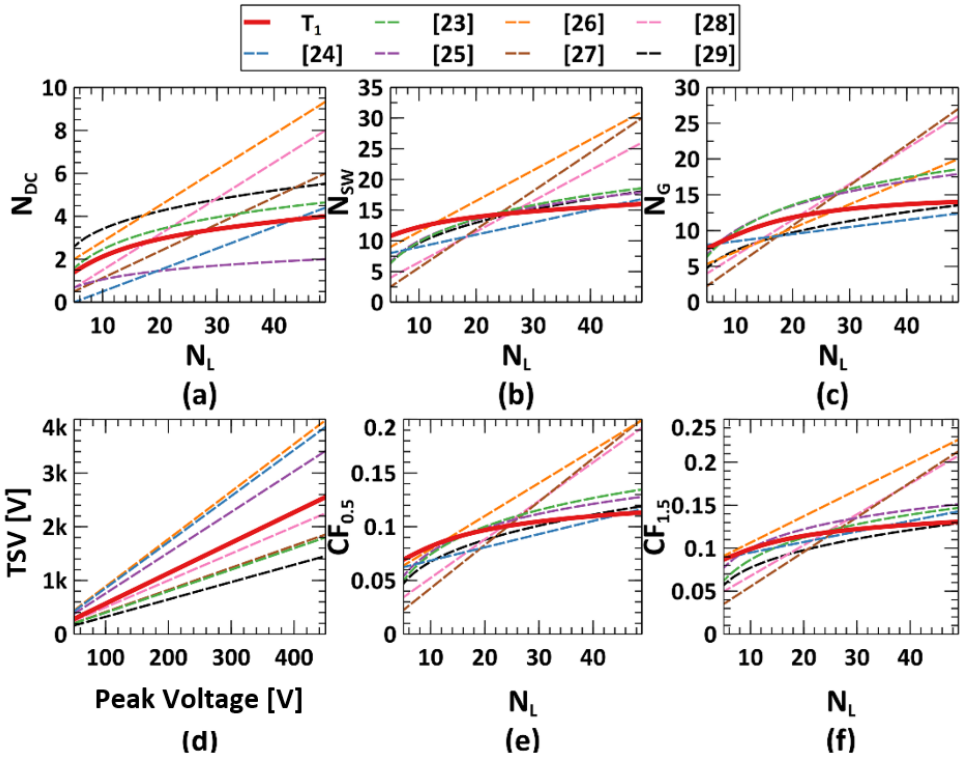

Fig. 5. Comparison of: a) N_{DC} vs N_L; b) N_{SW} vs N_L; c) N_G vs N_L; d) TSV vs V_{max}; e) CF at α=0.5.; f) CF at α=1.5.

4. RESULTS AND DISCUSSION

The proposed 49-L inverter was evaluated by testing its integration with PV sources as shown in Fig. 4. A 100 W resistive load was initially applied, with results presented in Fig. 6. Fig. 6 (a) demonstrates that the output waveforms successfully reached the target 230 Vrms after approximately 0.23 s. A closer view of the output waveforms in Fig. 6 (b) clearly confirms the successful generation of the 49 output levels. Under resistive load, the output voltage and current waveforms are in phase and exhibit the same stepped characteristics. The boost converter output voltages from the four PV stages (V_{L1}, V_{L2}, V_{R1}, and V_{R2}) are shown in Fig. 6 (c), verifying that the implemented control system correctly produced the required DC voltages of 13.55 V, 27.11 V, 94.87 V, and 189.74 V. Lastly, the FFT analyses of the output waveforms in Fig. 6 (d) reveal that both waveforms share the same THD value of 1.66% under resistive load.

Next, a resistive-inductive (RL) load of 100 W at a power factor (pf) of 0.5 is intentionally used to assess the topology's functionality under challenging pf conditions. Fig. 7 presents the findings. While Fig. 7 (a) displays the complete waveforms up to 0.5 seconds, Fig. 7 (b) provides a closer examination of the output waveforms. Similar to the resistive load test, the output voltage reaches 230 V rms after approximately 0.23 seconds. However, despite the voltage waveform maintaining its stepped pattern, the current waveform becomes smoother and loses its stepped pattern due to the RL load's filtering effect. This filtering, resembling an RL filter, allows only low-frequency signals to pass, blocking high-frequency

signals and noise at a cut-off frequency determined by R/2πL. Fig. 7 (d) confirms this with FFT analyses, showing a voltage THD of 1.66% and a reduced current THD of 0.11%. Additionally, Fig. 7 (c) demonstrates the boost converters' ability to produce the desired DC voltages without issue.

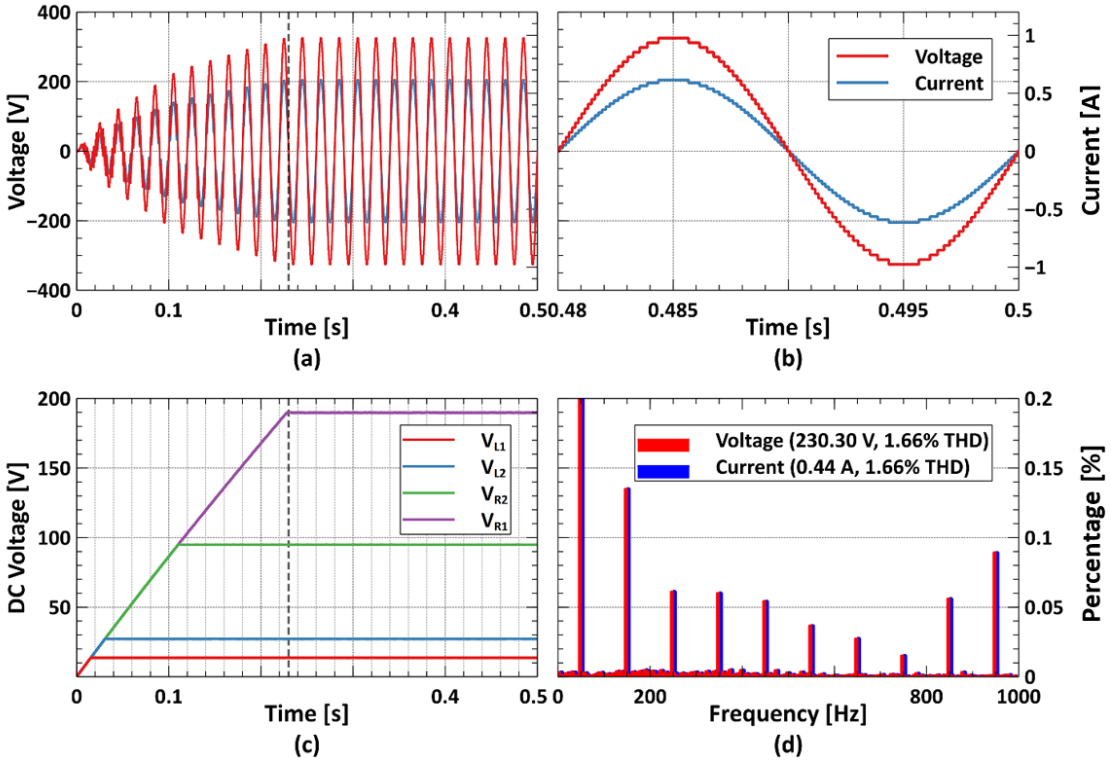

Fig. 6. Results under 100 W resistive load of: a) output voltage and current waveforms; b) close-up view of the output waveforms; c) boost converter voltages; d) FFT analyses of the output.

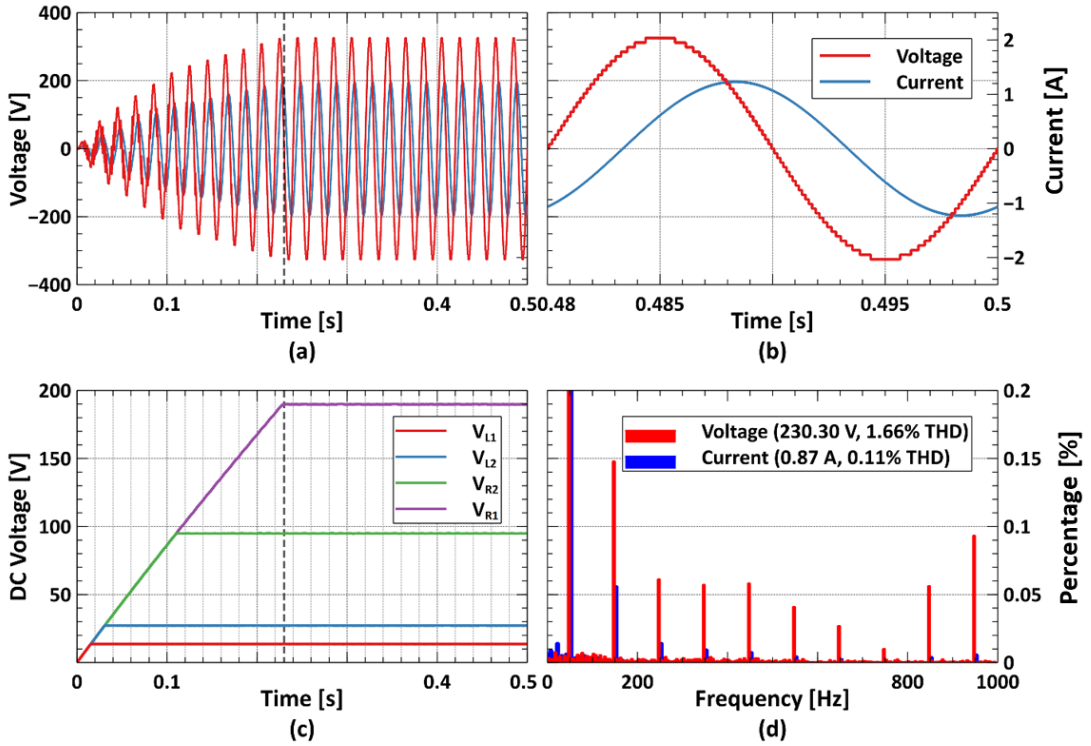

Fig. 7. Results under 100 W RL load at 0.5 pf of: a) output voltage and current waveforms; b) close-up view of the output waveforms; c) boost converter voltages; d) FFT analyses of the output.

Prior to an in-depth analysis of the 49-L inverter's characteristics, it is essential to grasp several supplementary aspects of its switching operation, as outlined in Table 2. "ON transitions" and "OFF transitions" denote the instances where a switch shifts from an OFF to ON state and vice-versa. "Conduction duration" indicates the cumulative time a switch remains ON. "Duty cycle average" represents the mean duty cycle of the switching signals. Finally, "average switching frequency" refers to the average frequency of these signals. Averages are calculated for duty cycle and switching frequency due to the absence of a regular pattern in the switching signals for the 49-L inverter, unlike conventional inverters. These elements from Table 2 are fundamental in determining the conduction, switching, and total losses of the switches, as detailed in the equations provided in Section 2.5.

The system then undergoes additional testing under varying combinations of resistive and RL loads to assess THD and efficiency. Efficiency is determined using the equations outlined in Section 2.5, considering only power switch losses. The IGBT model IKA08N65H5 is employed for this purpose. The results are presented in Fig. 8. Initially, resistive load values ranging from 100W to 500W are applied. As depicted in Fig. 8 (a), under resistive load, the output load had no significant impact on voltage and current THD, with all values remaining around 1.66%. In terms of efficiency, a slight decrease is observed with increasing power levels, as shown in Fig. 8 (b). The minimum and maximum measured efficiencies were 97.5% and 98.29%, respectively.

Table 2. Switching characteristics.

Switch	ON transitions	OFF transitions	Conduction duration [ms]	Average duty cycle [%]	Average switching frequency [Hz]
$S_{C,1}$	15	15	10.0	50.00	750
$S_{C,2}$	15	15	10.0	50.00	750
S_{C3}	3	3	10.0	50.00	150
S_{C4}	3	3	10.0	50.00	150
$S_{C1,2}$	13	13	10.0	50.00	650
$S_{C2,2}$	13	13	10.0	50.00	650
S_{C5}	1	1	10.0	50.00	50
S_{C6}	1	1	10.0	50.00	50
S_{L1}	28	28	5.25	26.26	1400
S_{L2}	28	28	5.76	28.82	1400
S_{L3}	14	14	6.41	32.05	700
S_{R1}	4	4	3.90	19.52	200
S_{R2}	4	4	4.64	23.18	200
S_{R3}	2	2	9.60	47.99	100

Next, the effect of varying RL load levels is examined. The target power is held constant at 300W while the pf is adjusted from 0.5 to 0.9. Fig. 8 (c) illustrates the THD values obtained at these different pf levels. Generally, a higher pf results in a higher THD at a fixed power, majorly due to the decreased filtering effect caused by the reduced proportion of inductive reactance in the load at higher pf. The minimum and maximum current THD measured are 0.109% and 0.14%, respectively. Conversely, efficiency improves with higher pf, as shown in Fig. 8 (d). This is attributed to the increased current drawn at lower pf, even at the same active power, which reduces efficiency. The minimum and maximum measured efficiencies are 96.04% and 97.84%, respectively.

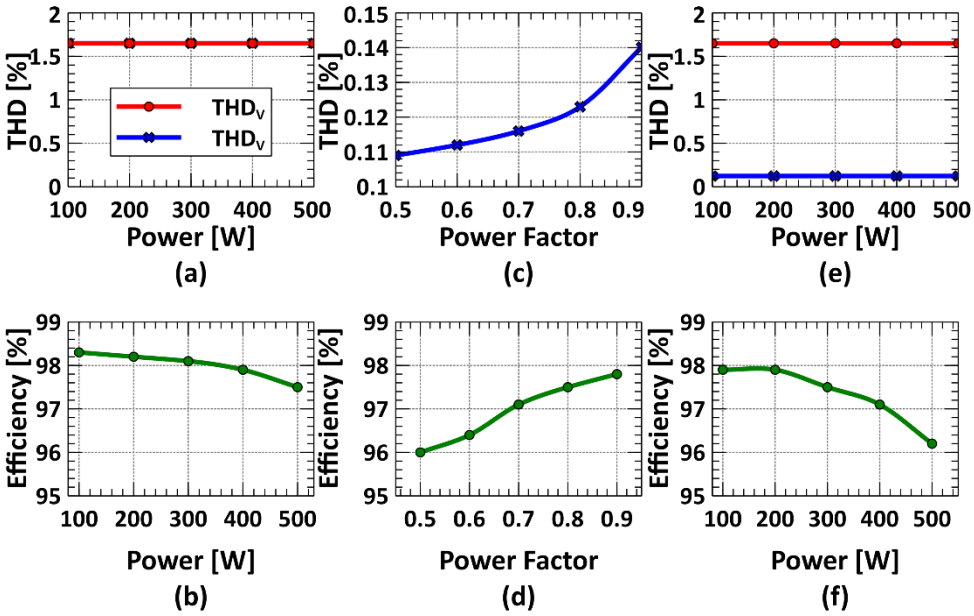

Fig. 8. Output THD and efficiency under: a) and b) resistive loads at different powers; c) and d) RL loads at different pf and fixed power; e) and f) RL loads at different powers and fixed pf.

Lastly, a final test is conducted using different RL load levels with a fixed pf of 0.8 and variable power levels ranging from 100 W to 500 W. As the pf remained constant, the voltage and current THD remained unchanged, as shown in Fig. 8 (e), confirming that output current THD is solely influenced by pf, not power level, and voltage THD is unaffected by load type. Throughout this test, voltage and current THD remained consistent at 1.66% and 0.123%, respectively. Efficiency decreased with higher power levels, as illustrated in Fig. 8 (f), aligning with the previous tests, indicating that efficiency is primarily related to power level. Measured efficiencies ranged from a minimum of 96.15% to a maximum of 97.88%.

The blocking voltage across the switches and the TSV of the inverter remain constant, regardless of the load levels and types tested. Fig. 9 displays the voltage waveforms across all 14 switches of the 49-L inverter, with their respective maximum blocking voltages labelled. These blocking voltages conform to the relationships established in Section 2.2. Therefore, the TSV can be determined by summing these individual blocking voltages. The calculated TSV is 1844.28 V, which is equivalent to 136.08 V_{DC}. This value is consistent with the relationship presented in Section 2.2.

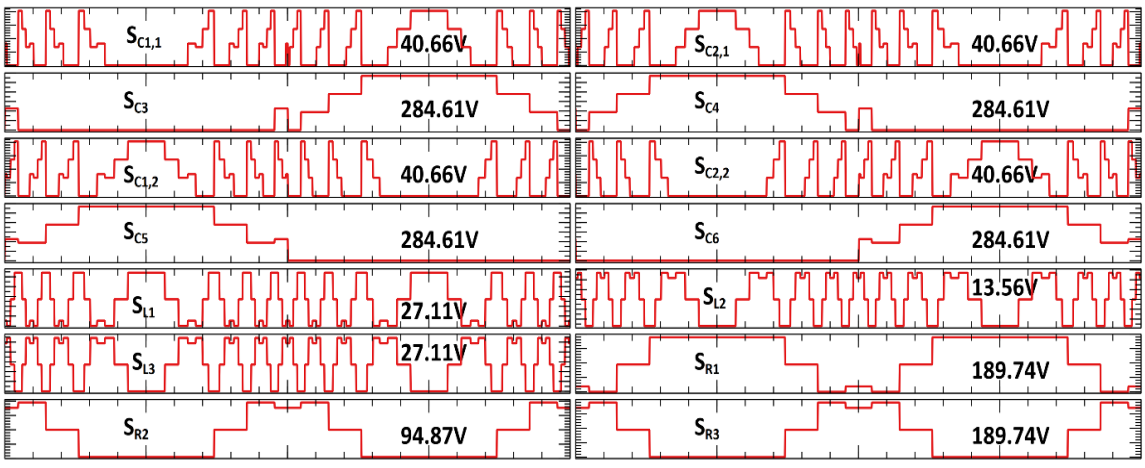

Fig. 9. Blocking voltages across switches.

After establishing the blocking voltages, the inverter underwent further testing to analyze power distribution among the four input sources. By quantifying the power contribution required from each source, appropriate supply sizing can be determined. This holds particular significance in renewable energy systems like PV systems, where the ideal number of PV panels per array can be identified. The results are illustrated in Fig. 10.

Fig. 10 (a) demonstrates that regardless of varying resistive load levels, the power demanded from sources V_{L1}, V_{L2}, V_{R4}, and V_{R3} consistently constitutes 1.28%, 3.35%, 28.93%, and 67.29% of the total power, respectively. Nearly identical observations were made under different RL load sets. When maintaining a fixed power factor while varying power levels, as depicted in Fig. 10 (c)-(d), the average power contribution from the sources remains at 1.27%, 3.34%, 28.92%, and 67.28%, respectively. Similarly, when varying power levels with a fixed power factor, as shown in Fig. 10 (e)-(f), the percentages are virtually consistent at 1.27%, 3.34%, 28.88%, and 67.16%, respectively. Understanding the power requirements of each source enables precise PV sizing, a crucial step in optimizing system efficiency.

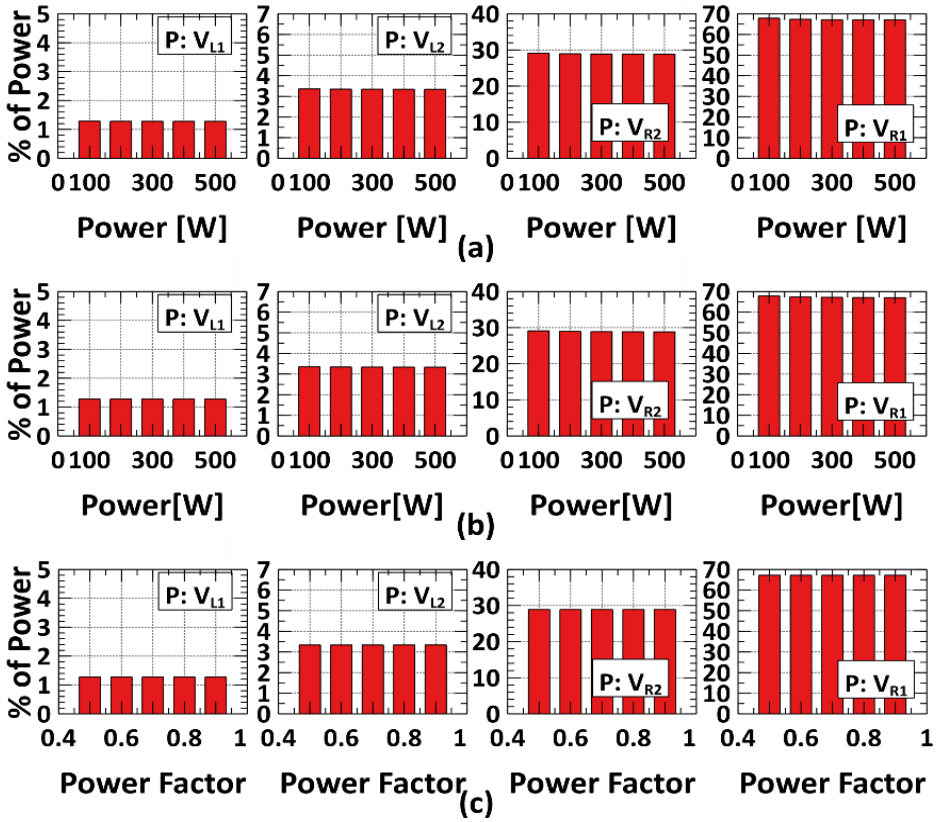

Fig. 10. Power sharing under: a) resistive loads at different powers; b) RL loads at different pf and fixed power; c) RL loads at different powers and fixed pf.

The final series of tests evaluated the 49-L inverter PV system's performance under dynamic conditions. To simulate varying sunlight, the system was subjected to fluctuating irradiation levels with a 100W load. Fig. 11 illustrates the results. The irradiance levels were adjusted incrementally, as shown in Fig. 11 (b). Fig. 11 (a) demonstrates that these abrupt changes in irradiation had minimal impact on the output waveforms. This stability is further emphasized in Fig. 11 (c)–(d). Additionally, Fig. 11 (b) reveals that the boost converter voltages remained consistent throughout all transitions.

Finally, the 49-L inverter PV system was subjected to a variety of load levels and types, with the results summarized in Fig. 12. Three load sets are selected which are a 500 W resistive

load, a 200 W RL load with a pf of 0.6, and another 100 W resistive load. Fig. 12 (a) demonstrates that these varying loads did not negatively impact the output waveforms. Fig. 12 (c)-(d) provide detailed views, highlighting the smooth transitions between load states. This smooth operation is further supported by Fig. 12 (b), which shows that, as with previous tests, there were no significant transient effects on the boost converter output voltages during load transitions.

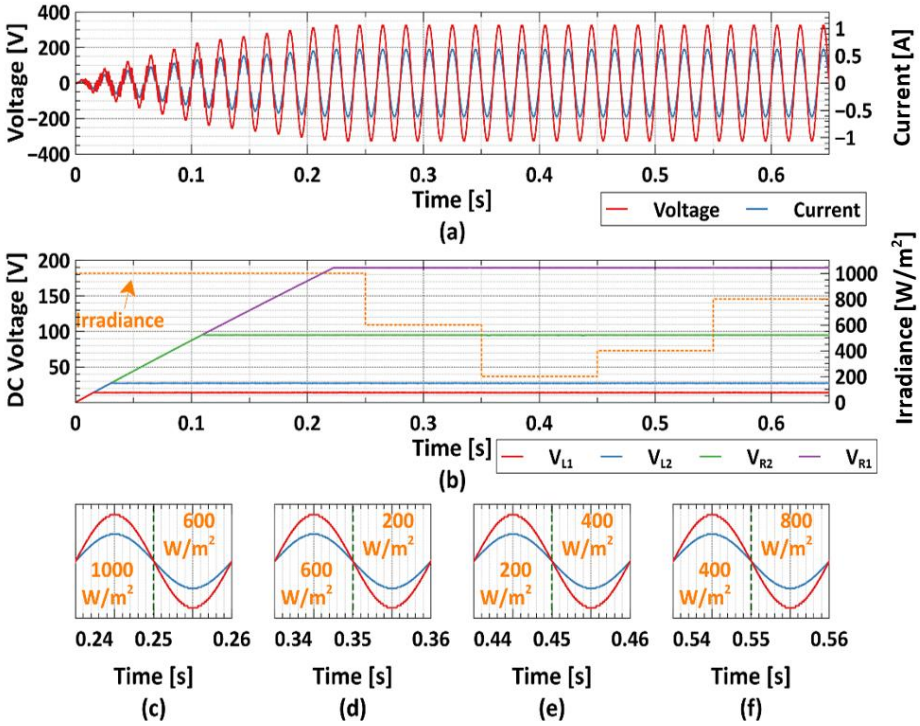

Fig. 11. Varying irradiance test results of a): output waveforms; b) boost converter voltages and irradiance levels; c) - f) closer views of the point of transitions.

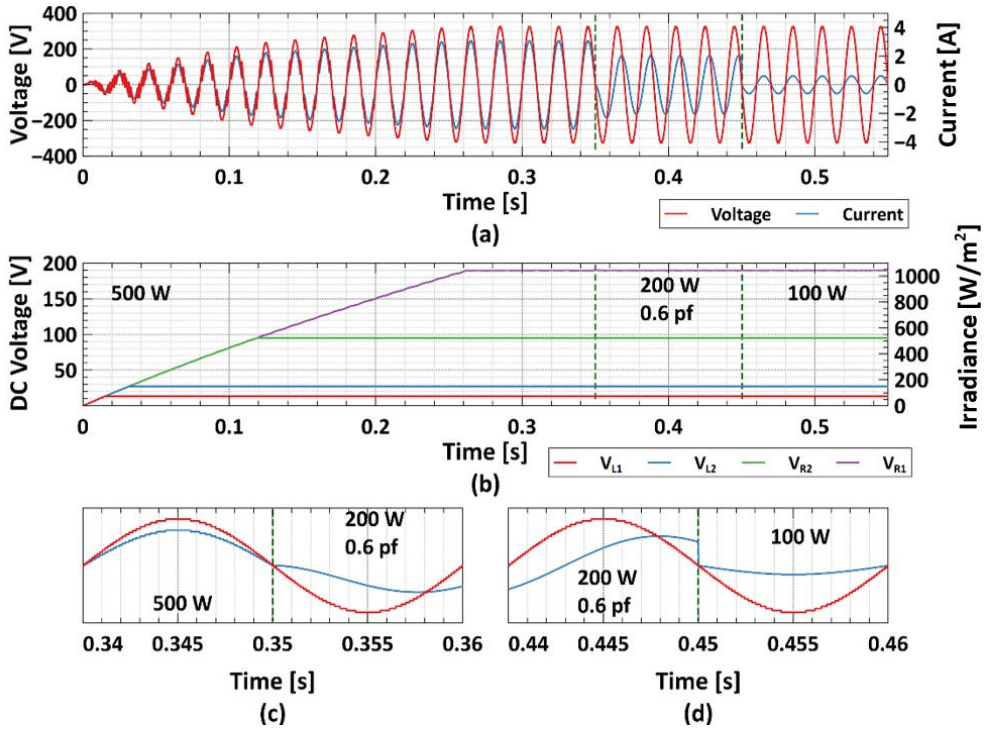

Fig. 12. Varying load test results of: a) output waveforms; b) boost converter voltages and irradiance levels; c) - d) closer view of the point of transitions.

5. CONCLUSIONS

This paper presents a novel 49-L inverter topology designed to address the limitations of traditional inverters in PV renewable energy systems. The proposed design focuses on minimizing component count and TSV at high output levels, making it suitable for various applications. The inverter incorporates a modified packed H-Bridge unit and n basic units to optimize component usage and reduce switch voltage stress. Mathematical formulations for calculating switching angles are provided, simplifying switching signal generation and reducing processing requirements. The 49-level inverter is rigorously tested under different load conditions, with analysis focusing on key performance metrics such as THD, switch voltage stress, TSV, and efficiency. The topology's applicability for PV system integration, particularly in standalone systems, is demonstrated, showcasing its potential for renewable energy applications.

The results indicate that the proposed inverter achieves a low THD of 1.66% for voltage and current under resistive loads and 0.11% - 0.14% for current under RL loads, meeting the IEEE 519 standards. The efficiency of the inverter ranges from 96% to 98%, depending on the load conditions. The inverter also demonstrates good performance under dynamic conditions, with smooth transitions during changes in irradiation levels and load types. The proposed 49-level inverter offers a promising solution for PV renewable energy systems, providing high power quality, efficiency, and flexibility. Additionally, at the targeted 49-L output, the proposed topology is also the most cost-effective topologies - with the lowest CF values at both tested α values of 0.5 and 1.5 - when compared to the other recent MLI

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