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Design of Multilayered XOR Gate Using Quantum Dot Cellular Automata

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***Abstract*—** The rapid advancement of microelectronics technology necessitates the development of high-speed, low-power devices. Quantum Cellular Automaton (QCA) is emerging as a promising technology enabling logic circuits with exceptional operating speeds. The XOR gate is crucial in nanocomputing applications, such as nano-processors and nano-communication units, and requires innovative design approaches. This paper presents a novel design of an XOR gate using a multilayered layout methodology within the QCA framework. The circuit's design and validation are performed using QCADesigner 2.0.3, while energy dissipation analysis is conducted with QCADesigner-E, resulting in an energy dissipation of 15 meV. Comprehensive parameter analysis, including cost functions, highlights the superiority of the proposed design. A comparative analysis with similar existing multilayered designs shows a 55% improvement in QCA-specific quantum cost. Notably, the proposed design eliminates the need for internal nodes within the layout, enhancing the methodology's applicability to higher-order and more complex circuits.

***Keywords*—** Crossovers**;** Multilayered designs**;** Quantum dot cellular automata**;** XOR gate; QCADesigner-E; QCADesigner 2.0.3.

1. INTRODUCTION

The physical restrictions of transistor miniaturization exacerbate power consumption and scaling issues in CMOS technology [1]. Furthermore, CMOS scaling is reaching its limits, limiting performance and energy efficiency advancements [2]. Promising alternatives are provided by emerging technologies such as Quantum Dot Cellular Automata (QCA) by leveraging nanoscale phenomena to achieve ultra-low power consumption, enhanced scalability, and potentially higher computational densities, thus addressing the shortcomings of CMOS and paving the way for next-generation computing paradigms [3]. Nowadays, QCA research is at its peak, with several designs accessible with modern computing and processors. However, further research into basic building blocks, such as the XOR gate, is required to mature this technology. XOR gates serve as indispensable building blocks in digital circuits for performing essential operations like addition, comparison, and error detection. Their versatile functionality and straightforward logic make them essential components in various computational tasks, contributing to the foundation of modern digital computing systems. Moreover, in error detection, XOR gates facilitate parity check codes, which are crucial for identifying single-bit errors during data transmission or storage, highlighting their indispensable role in modern computing systems. This paper presents a multilayered XOR gate design implemented with QCA technology. Subsequently, we delve into the design and

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simulation of the multilayered XOR gate, discussing its performance metrics. Note that there are two approaches for designing a circuit with QCA: multilayer and coplanar. Coplanar QCA designs, with cells arranged in a single layer, offer simplicity but face limitations in complexity and scalability. Multilayer QCA designs, on the other hand, allow for more complexity and scalability by stacking cells across multiple layers. This means that nanoscale computing systems will be able to do more and handle errors better.

The paper is structured as follows: Section 2 provides fundamental information on QCA. The literature review is included in Section 3. Section 4 elaborates on the design, simulation, and results of the multilayered XOR gate. Section 5 presents the parameter analyses, while Section 6 compares the findings with existing works. Section 7 provides a brief overview of the findings and recommendations for further study to round out the article.

2. FUNDAMENTALS OF QCA

Some basic terminologies related to this technology are generally used in all QCA designs. The QCA basic unit cell takes on a square shape composed of four quantum dots situated at each corner of the square, as referenced in [4]. Each cell measures 18 *nm* long, with a total area of 324 nm^2. Fig. 1a illustrates the binary logic 1 and logic 0 polarization states, which are defined based on the electron positions [5]. One of its fundamental building blocks is the majority gate, which is necessary for complex logic operations because it computes the majority logic function of its inputs. Another essential part that allows for signal inversion and various circuit functions is the inverter, which reverses the input logic state. The typical layout of a QCA inverter is shown in Fig. 1b. In QCA, wires act as channels for information to travel between cells, enabling computation and communication throughout the circuit [5], as shown in Fig. 1c. These fundamental building blocks open the door to ultra-low power, high-speed computing paradigms because they are made of quantum dots and operate according to quantum principles. Next, the Majority Voter (MV) is an essential component of QCA circuits. Fig. 1d illustrates a typical three-input majority gate layout consisting of five cells: three inputs, one output, and a central decision-making cell [5]. The MV uses majority logic, as Eq. (1) indicates, which combines inputs A, B, and C to obtain the output. The logic function M (A, B, C) is then applied to three inputs (A, B, and C) as follows:

$$M(A, B, C) = AB + BC + CA \quad (1)$$

The distinct architecture and constituents of QCA present auspicious prospects for surmounting the constraints of traditional technologies and propelling progress in nanoscale computing systems. To fully realize the potential of QCA for various applications, including data processing and quantum computing, ongoing research is essential. Researchers are working to optimize QCA designs and fabrication techniques. Cells are placed on substrates according to a placement algorithm in QCA, and the QCA clock controls their routing. An irregular four-phase clocking method is utilized to synchronize the information flow. The power needed for calculation is also provided via QCA clocking. Most of the time, there are several phases. A clock zone clocks a range of cells simultaneously in QCA architecture as opposed to clocking each cell independently. The QCA clock comprises four distinct stages: hold, release, relax, and switch, illustrated in Fig. 1f [4-6]. A 90° gap is assumed between consecutive phases. The process begins during the switch phase, where the tunneling barrier between two dots rises. Subsequently, the barrier decreases from high to low in the third phase

as the system transitions into the hold phase. Finally, the cell remains unpolarized during the relax stage with no inter-dot barrier [6].

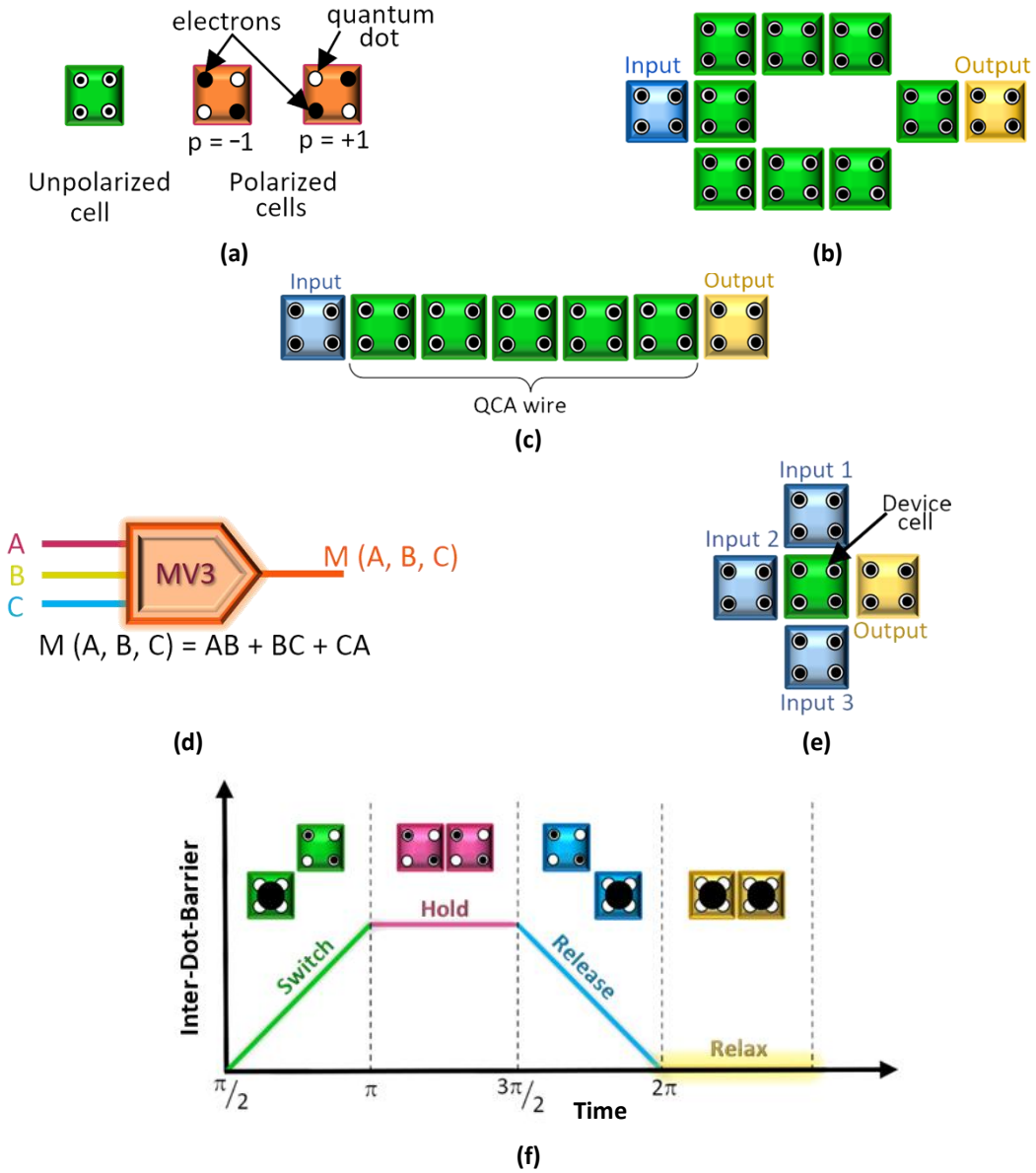

Fig. 1. QCA fundamentals: a) cell states; b) QCA inverter layout; c) wire; d) majority gate schematic; e) majority gate typical layout; e) clock phases.

3. LITERATURE STUDY

Numerous contributions such as wires [7], inverters [8], multiplexers [9], and more enrich the QCA literature, with ongoing efforts in similar veins continuing to expand its depth. In the QCA literature, numerous excellent designs of XOR gates exist, with the majority characterized by very small cell counts and single-layered layouts devoid of crossover-based designs. However, each design carries its own set of advantages and disadvantages. In this study, we focused on a selection of XOR gate designs from the literature that are comparable to our current work.

A novel XOR gate has been designed using 41 QCA cells with 0.75 clock latency [10]. This structure has three majority gates with an inverter, and no crossover was used. One main shortcoming in this design is that one input node is placed inside the circuit, so there is no

scope to develop the circuit further. In [11], an XOR gate design utilizing 40 QCA cells based on three majority gates was proposed. This design was suggested to have a 0.75 clock cycle latency employing a multilayer crossover approach. However, a notable drawback in this design is the placement of either an input or an output node within the circuit. An XOR gate was crafted using 70 QCA cells and three majority gates [12]. It boasts a 0.75 clock cycle latency and employs coplanar crossovers. However, a primary drawback of this design is the placement of one input node within the circuit. A new XOR gate has been developed employing 45 QCA cells utilizing four majority gates and four inverters with a clock latency of 0.50 [13]. The primary drawback of this design is a higher count of basic design blocks. In [14], two XOR gates consisting of 84 and 51 cells were suggested, each employing two majority gates with a 0.75 clock cycle latency and devoid of crossovers. However, the main drawback of these designs is their higher cell count. In [15], a fault-resistant XOR layout was devised employing three majority gates and an inverter. It comprises 73 QCA cells and features a 0.75 clock delay, with no employment of crossovers. However, a notable drawback lies in the positioning of the input node within the circuit. Furthermore, in [16], an Ex-OR logic is introduced that utilizes three majority gates, one inverter, and 44 QCA cells with a 0.75 clock cycle latency. Notably, while no crossovers are needed, the output node is kept within the circuit, as depicted in the design layout, limiting further development possibilities for this design. A different XOR gate design was suggested in [17], employing 85 QCA cells integrating three majority gates and two inverters without crossovers. This configuration exhibits a latency of 1.25 clock cycles. However, its disadvantages include the elevated cell count and the resulting delay.

This work identified several excellent XOR architectures during the literature study. However, most works suffer from internal input/output nodes, high cell counts, or significant delays. This work presents an XOR gate with a solution that eliminates the need for internal input/output nodes, offering a more manageable cell count and delay. This work introduces a novel multilayered XOR gate with a complexity of 38 cells and a delay of 0.75 clock. It employs three majority gates and does not require internal input/output nodes.

4. THE PROPOSED XOR GATE

This section discusses the simulation tool, proposed QCA layout, and design reliability. As mentioned earlier, this work proposes a multilayered XOR gate, and the layout is designed and verified using the QCADesigner simulation platform.

4.1 Simulation Tool

This design layout is developed using QCADesigner 2.0.3 [18], a widely recognized simulation tool for evaluating QCA circuit performance. This tool utilizes the Bistable Approximation Engine to calculate the state of QCA cells based on a time-dependent approach. It integrates a computational model that includes dynamics of QCA cell polarization, interactions between cells, and clocking mechanisms to simulate circuit operations accurately. Users can configure circuit layouts, set input states, and simulate circuit behavior under diverse conditions through its Graphical User Interface. This tool determines output signals by assessing QCA cell polarization states, considering Coulombic interactions

and energy barriers between adjacent cells, thereby providing detailed insights into circuit functionality and performance.

4.2 Suggested Layout

In this work, we present a multilayered two-input XOR gate. The truth table of the XOR function is exhibited in Table 1. Fig. 2a shows the schematic of the suggested XOR gate. It utilizes three majority gates and two inverters. There are wire crossings at the input lines; hence, we have utilized the multilayered design approach in QCA to deal with wire crossings efficiently. It's worth mentioning that A and B are the two inputs of the XOR gate, where B is the least significant bit (LSB) and A is the most significant bit (MSB). The QCA cell arrangement of the proposed XOR gate is illustrated in Fig. 2b. It is a QCA-based multilayered two-input XOR gate layout comprising 38 QCA cells. Distributing components across multiple layers effectively utilizes area, reduces signal propagation delays, and enhances overall performance. The input line A and the output line Y are located at the bottom layer (main cell layer), and the input B is located at the top layer (upper layer). Different layers of the proposed layout are depicted in Fig. 2.

The main cell layer is shown in Fig. 2c, the middle layer in Fig. 2d, and the upper layer in Fig. 2e. This strategic placement and routing of components ensure efficient operation and faster circuit performance. However, scaling this methodology to larger circuits presents challenges such as alignment and synchronization across layers, increased fabrication complexity, and thermal management. Addressing these challenges requires advanced clocking schemes, precision manufacturing techniques, and efficient thermal management strategies.

Table 1. Logic table of the XOR gate.

Inputs		Output
A (MSB)	B (LSB)	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

This circuit has three majority gates, two inverters, and one multilayered wire crossover. For smooth signal transmission, we have used a maximum of three clock phases out of four through the worst path from the input node to the output node, and hence, the latency of the design is estimated at 0.75 clock cycles. Its total area is 0.06 μm^2. It uses three constant inputs: two fixed polarizations of -1.00 (binary 0) and one fixed polarization of 1.00 (binary 1). It does not use any translated or rotated cells. Simulation results are validated against the expected truth table outcomes, as depicted in Fig. 2f.

4.3 Scalability of the Proposed QCA XOR Gate Design

We expect that the proposed QCA design of the XOR gate will offer a compact, scalable, and efficient solution for implementing higher-order logic functions. The proposed QCA XOR gate design, with its lower cell counts and full input-output accessibility, shows great promise for scaling up to more complex circuits like half adders, full adders, and subtractors, where

XOR gates are unavoidable primitive components. The accessibility of all input and output nodes simplifies interconnections, supports modular design, and ensures efficient signal transmission, leading to faster and more reliable operations. This compact design saves space and reduces power consumption, making it ideal for integrating more logic gates within a chip. However, scaling this design to larger circuits and systems poses several challenges that must be addressed to harness the full potential of QCA technology in practical applications, such as mainly signal propagation delay and clock & synchronization through increased complexity.

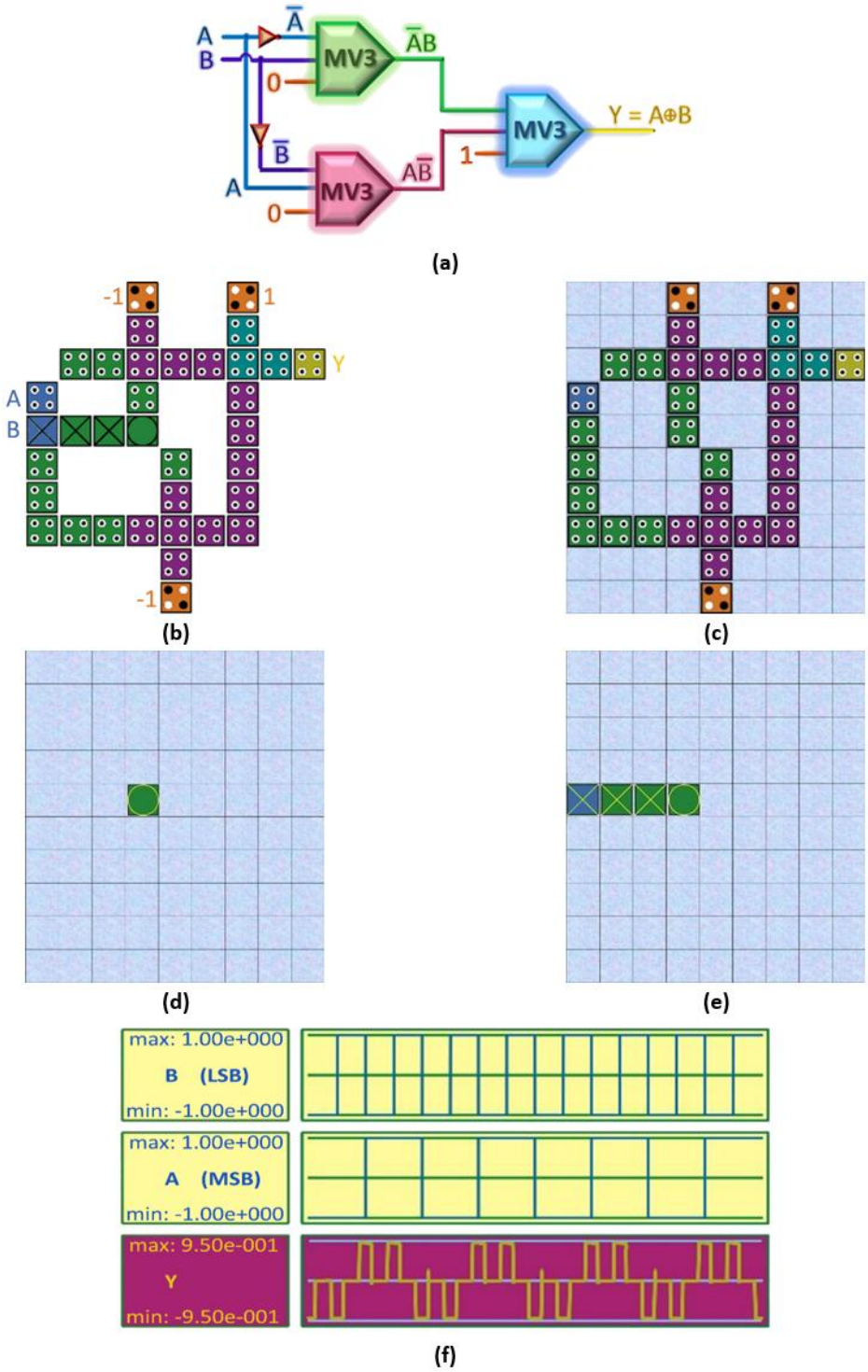

Fig. 2. The proposed design: a) schematic; b) QCA layout; c) main cell layer; d) middle layer; e) upper layer; f) simulation output.

These would be overcome by a hierarchical design approach, interconnect optimization, and power management techniques. As a future work, we can optimize the interconnections in the smaller circuits and then reassemble them hierarchically, significantly reducing the signal propagation delay and improving the system's overall performance. The use of faster clocking zones is one of the techniques that can enhance signal transmission in larger circuits.

5. ANALYSIS

Beyond the various design parameters outlined in the preceding section, we conducted an analysis of energy dissipation, cost estimations, and an introductive idea about the fault tolerance for the design. This section delves into these analyses to facilitate a more comprehensive comparison with related studies.

5.1. Energy Dissipation

Energy dissipation in QCA circuits is a critical factor for evaluating their performance and efficiency. To measure it for a multilayered design, the QCADesigner-E (QDE) tool [19] provides detailed energy dissipation reports, including the total energy consumed and energy loss distribution across different circuit parts. The overall energy dissipation for our circuit amounts to 15 meV, with an average energy dissipation of 1.37 meV per cycle.

The QDE tool extends the functionalities of the original QCADesigner tool by incorporating detailed energy models that account for the unique characteristics of QCA technology. The tool simulates the switching activity of QCA cells and the influence of the clocking field, which drives the computation by modulating the potential barriers between cells. This involves modeling the cell-to-cell interactions and the energy transfer mechanisms within the QCA array [20].

5.2. Cost functions

We, furthermore, have conducted a comprehensive cost analysis of the proposed QCA circuit. The cost of QCA circuits can be evaluated in terms of several specific metrics, which reflect different aspects of performance and efficiency. This analysis encompasses three distinct types of cost functions [21], detailed below.

$$\textit{Area-delay cost (ADC)} = \textit{total area} \times \textit{delay}^2 \quad (2)$$

$$\textit{Energy-delay cost (EDC)} = \textit{energy}^2 \times \textit{delay}^2 \quad (3)$$

$$\textit{QCA-specific cost (QSC)} = n[MV^2+NG^2+WC^2]\times D^2 \quad (4)$$

Here, MV, NG, and WC denote the number of majority gates, NOT gates, and wire crossings in the proposed design, respectively, n= number of layers.

According to the Eqs. (2)-(4), the proposed design's ADC, EDC, and QSC are 0.03375 units, 0.00013 units, and 21.94 units, respectively.

5.3. Fault tolerance

Fault tolerance in a QCA circuit refers to its ability to maintain reliable and correct operation despite the presence of defects or faults. It typically incurs hardware overhead and performance degradation with redundant components or devices, such as Triple Modular Redundancy (TMR), where three circuit copies operate in parallel, and the output is determined

by majority voting [12]. These faults can arise from various sources, including manufacturing imperfections, environmental conditions, or operational stresses. For example, a stuck-at-fault might make a QCA cell always stay in one state, like '0' or '1', even when it should change based on inputs. Missing cells, which can happen during manufacturing, can completely mess up how the circuit computes XOR operations, leading to incorrect results. Problems with the wiring between cells, like breaks or faults, can slow down or completely stop signals from moving through the circuit, making it fail. QCA circuits are also sensitive to temperature or electrical noise changes, which can introduce errors or cause circuit parts to stop working correctly [22].

To fix these issues in real applications, engineers use strategies such as systematic testing of QCA blocks during design phases to establish methodologies for developing defect-tolerant circuits. Detailed cell numbering and fault-tolerant design mitigate missing cell issues. Analyzing energy distribution and cell polarities aids in constructing rotation-resistant circuits. Addressing cell misalignment involves identifying and correcting orientation errors. It underscores the significance of fault tolerance in enhancing the robustness and reliability of QCA systems, which are crucial for high-performance, energy-efficient computing [22].

Fault tolerance of the proposed design is an important research direction and is beyond the scope of the current experiment. We consider this as a future extension of our work. Therefore, future studies will pursue the development of a fault-tolerant XOR gate.

5.4. Reliability

The reliability of a QCA circuit means it can consistently work correctly over time and in different conditions without breaking down. It should reliably give the correct outputs for inputs it receives, even if there are minor environmental changes. Implementing fault-tolerant design principles ensures continued operation despite individual cell failures. Rigorous testing during fabrication and simulation phases identifies and addresses potential defects early on. Careful layout design and clocking schemes optimize signal propagation and minimize interference.

Moreover, using advanced lithography and precise manufacturing techniques reduces variability and enhances consistency [17]. Analysis of the proposed design's reliability in a practical context is an essential realm of research beyond the scope of the current experiment. We intend to explore this as a future extension of our work.

6. COMPARISON WITH SIMILAR DESIGNS

The proposed design uses three cells less than the latest relevant optimum design [10]. Furthermore, the works in [10] and [11] lack both full input-output accessibilities and energy calculation, which is an inferior analysis compared to this work. The delay is also identical for both the proposed and the prior design. The comparison tables are presented in Tables 2 (in which CC denotes cell count, TA: total area, D: delay, LT: layer type, LC: layer count, CT: crossover type, NA: not applicable, ML: multilayered, EC: energy calculation, I/O: full input/output accessibility, Y: yes, N: no) and Table 3 (in which # denotes count, MV: majority voter, NG: NOT gate, WC: number of crossovers, TE: total energy in meV, ADC: area-delay cost, EDC: energy-delay cost, QSC: QCA specific cost). The proposed design underwent a rigorous analysis of parameters, including energy dissipation. This work explores three cost functions, which are tabulated below.

Considering the only multilayered design in [11] among all the mentioned preceding studies here, our proposed design eliminates crossover counts to one yet maintains all nodes outside the architecture, resulting in a 55% superiority in terms of QSC. Thus, higher-order circuit design and wire-crossing implementations are simplified in a multilayered approach.

Table 2. Design parameters of the existing and the proposed designs.

Ref.	CC	TA	D	LT	LC	CT	EC	I/O
[10]	41	0.04	0.75	Single	1	NA	N	N/Y
[11]	40	0.04	0.75	Multiple	3	ML	N	Y/N
[12]	70	0.06	1.25	Single	1	NA	N	N/Y
[13]	45	0.05	0.50	Single	1	NA	N	Y/Y
[14]	84	0.06	0.75	Single	1	NA	N	Y/Y
[14]	51	0.04	0.75	Single	1	NA	N	Y/Y
[15]	73	0.06	0.75	Single	1	NA	Y	Y/Y
[16]	44	0.05	0.75	Single	1	NA	Y	Y/N
[17]	85	0.08	1.25	Single	1	NA	N	Y/Y
Proposed	38	0.06	0.75	Multiple	3	ML	Y	Y/Y

Table 3. Energy and cost functions of the existing and the proposed designs.

Ref.	#MV	#NG	#WC	TE	Cost functions		
					ADC	EDC	QSC
[10]	3	1	0	NA	0.023	NA	~5
[11]	3	2	4	NA	0.023	NA	~49
[12]	3	1	0	NA	0.094	NA	~16
[13]	4	4	0	NA	0.013	NA	8
[14]	2	2	0	NA	0.034	NA	~8
[14]	2	1	0	NA	0.023	NA	~3
[15]	3	1	0	198.54	0.034	0.022	~6
[16]	3	1	0	0.05	0.028	1×10^{-09}	~6
[17]	3	2	0	NA	0.125	NA	~21
Proposed	3	2	1	15	0.034	0.00013	~22

7. CONCLUSIONS

This paper introduced an innovative layout design approach for XOR gates employing QCA, a technology renowned for facilitating high-speed and low-power digital circuits. We achieved an impressive result through meticulous design and validation processes using QCADesigner 2.0.3 and energy dissipation analysis in QCADesigner-E (QDE). Furthermore, rigorous parameter analysis, including cost functions, underscored the superiority of the proposed design, showcasing a significant improvement in different parameters. The findings demonstrate the efficacy of multilayered layout design within the QCA framework, particularly in addressing the critical need for high-speed and low-power consumption devices, such as XOR gates, essential in nanocomputing applications. Importantly, the proposed design eliminates the necessity for internal nodes within the layout; thereby extending the applicability of this methodology to higher-order and more complex circuits.

Although this investigation has produced encouraging outcomes, numerous paths remain for additional exploration and enhancement. One potential direction is to investigate the scalability of the poposed design methodology to larger circuits and systems, exploring its feasibility in real-world applications beyond XOR gates. Moreover, incorporating fault tolerance and reliability analysis techniques would enhance the robustness of QCA-based circuits, making them more viable for practical deployment.

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