JJEE
Volume 10 | Number 4 | December 2024 | Pages 563-593

Jordan Journal of Electrical Engineering

ISSN (print): 2409-9600, ISSN (online): 2409-9619

Homepage: jjee.ttu.edu.jo

Analog CMOS Design in Nanometer Regime

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Received: Dec 28, 2023 *Revised: Mar 19, 2024* *Accepted: Mar 30, 2024* *Available online: August 19, 2024*

***Abstract*—** There is no doubt that the short-channel effects have affected the analysis and design of modern analog CMOS integrated circuits significantly. Thus, models that take into account these effects must be adopted in order to obtain more accurate results. In this paper, the AC small-signal low-frequency equivalent circuit of the short-channel MOSFET transistor is developed using an appropriate model. The impact of short-channel effects on the operation of basic building blocks of analog integrated circuits such as basic amplifier configurations, cascode stage, differential amplifier and composite transistor is investigated quantitatively. Additionally, the nonlinear distortion is investigated using the adopted model.

***Keywords*—** Building blocks of analog integrated circuits; CMOS design; Nanometer regime; Nonlinear distortion; Short-channel effects; Unity-gain frequency.

Nomenclature

v_{GS}	The total gate-to-source voltage	L	The effective channel length
V_{GS}	The pure dc gate-to-source voltage	$(W/L)_n$	The aspect ratio of the NMOS transistor
v_{gs}	The pure ac gate-to-source voltage	T	The absolute temperature
v_{DS}	The drain-to-source voltage	q	The electronic charge
v_{SB}	The source-to-body voltage	y	The linearized body-effect coefficient
V_{thn}	The threshold voltage	η	The drain-induced barrier lowering (DIBL) coefficient
V_{thn0}	The threshold voltage at $v_{SB} = v_{DS} = 0$ V	v_{sat}	The free-electron saturation velocity
V_{th}	The thermal voltage	μ_{0n}	The mobility of free electrons at low electric fields
V_{DSsat}	The drain-to-source voltage at the edge of saturation	μ_{eff}	The effective mobility of free electrons
i_D	The total drain current of the MOS transistor	θ	The mobility-degradation effect parameter
I_D	The pure dc drain current	λ	The channel-length modulation effect parameter
i_d	The pure ac drain current	n_n	The subthreshold-swing coefficient
C_{ox}	The gate-oxide capacitance per unit area	η_{NWE}	The factor accounting for the narrow-width effect
C_d	The depletion-layer capacitance per unit area	C_L	The load capacitance
C_{GS}	The gate-to-source capacitance	v_{in}	The input voltage of the amplifier
C_{GD}	The gate-to-drain capacitance	v_{out}	The output voltage of the amplifier
W	The effective channel width	V_{DD}	The power-supply voltage

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DOI: https://doi.org/10.5455/jjee.204-1703756483

1. INTRODUCTION

There is no doubt that CMOS technology is the technology of choice in analog, digital, and mixed-signal systems due to its ease of fabrication, high density of integration, and low power consumption. Due to the dominance of the deep-submicron CMOS technology in the digital domain, analog CMOS circuits should be investigated in correspondence with deep-submicron CMOS technologies in order to explore their limits of compatibility in mixed circuits. In order to properly design a CMOS circuit, simulation must be performed in order to check the validity of the design [1]. However, a first-order hand quantitative analysis must also be performed in order to obtain a rough estimation of the results and to gain a physical insight into the operation of the circuit [2]. In order to simplify the hand analysis and gain physical insight into the circuit operation, simple models should be used. The price paid for simplicity, however, is degraded accuracy and the designer will inevitably face the well-known compromise problem, simplicity versus accuracy.

One of the most important challenges in designing nanometer CMOS analog circuits is the reduction of V_{DD} with a slower reduction of V_{thn} [3]. Specifically, in order to reduce the power consumption in digital circuits and to reduce the probability of device breakdown, V_{DD} scales down with technology scaling. In fact, for CMOS technologies older than and up to 5 μm, the adopted power supply was 5 V. For technologies beginning from 0.35 μm and newer, the value of V_{DD} has steadily decreased [4]. In order not to degrade speed, V_{thn} reduces also with technology scaling. However, reducing V_{thn} slightly causes a significant increase in the subthreshold leakage. So, V_{thn} decreases at a slower rate compared to that of V_{DD}. The result is that the V_{DD}/V_{thn} ratio decreases with technology scaling. However, reducing V_{DD} causes difficulties with designing analog circuits due to the reduced voltage headroom and the increased $1/f$ noise [5, 6]. Scaling down the dimensions causes also difficulties with matching [7]. The third challenge is the significant change of the threshold voltage with the channel length [4]. The fourth challenge is the reduction of the overdrive voltage with technology scaling. In fact, the overdrive voltage of MOS devices is limited to typically 0.1 or 0.2 V. This poses a serious problem in the circuit techniques that include stacks such as cascodes and double cascodes.

Also, other issues arise with the design of analog and RF circuits in deep-submicron technologies such as the reduced dynamic range and the degraded performance of MOS switches in switched-capacitor circuits, sigma-delta circuits [4], multiplexers, sample-and-hold circuits, and data converters [8].

These challenges require a careful design of modern CMOS analog circuits. In spite of the fact that the analog circuits are the dominant ones in 5-μm chips that are dated back to the seventies, the digital circuits become the dominant ones in 5-nm chips in 2016 [9]. However, the need still arises for designing analog circuits as they act as the interface to digital ones. Also, mixed-signal circuits are employed in digital networking and digital-storage systems in order to obtain a low bit-error rate and high-quality storage [10]. Thus, analog circuits must keep pace with the evolving digital circuits.

Also, an important issue that is becoming more important with technology scaling is the effect of the leakage current. The leakage currents increased with technology scaling due to the increased device density, reducing the threshold voltage, and adopting thinner gate dielectrics [11]. The leakage currents include the weak-inversion leakage, drain-induced barrier lowering leakage, gate-induced drain leakage, and gate-oxide tunneling current [12].

Channel-engineering techniques such as retrograde well, and halo doping were proposed for reducing the leakage. Also, various circuit techniques have been developed for reducing the leakage currents such as the LECTOR (leakage control transistor), input-vector control, dual stack, sleepy keeper, sleepy stack, forced transistor stacking, super-cutoff CMOS, and multi threshold CMOS [13, 14]. However, since leakage-power consumption is a major issue with digital circuits, this issue will not be pursued further here.

Basic building blocks of analog integrated circuits such as basic amplifier configurations, cascode stage, differential amplifier, and composite transistor were already investigated quantitatively in [15] using the familiar square-law long-channel MOSFET transistor model. However, this model is no longer valid for the quantitative analysis of analog MOSFET circuits in nanometer regime as many short-channel effects were not taken into account in this model. In this paper, the small-signal low-frequency equivalent circuit will be developed using a short-channel model and it will be adopted in the quantitative analysis of the previously mentioned basic building blocks. Then, the main differences between these blocks in short channel and long channel regimes will be discussed. Note that according to the classification in [16, 17], there are four levels of CMOS processes according to the adopted minimum feature size. If the minimum feature size is smaller than 1 μm, it is called a *submicron process*, if it smaller than 0.25 μm, it is called a *deep-submicron process*, if it is smaller than 100 nm, it is called a nanometer process, and if it smaller than 45 nm, it is called a *deep-nanometer process*.

The remainder of this paper is organized as follows: Section 2 discusses some of the previous works related to analog CMOS design in modern processes. Section 3 presents the more accurate MOSFET transistor model that is adopted in the analysis in this paper and the corresponding small-signal equivalent circuit is developed also in this section. Section 4 investigates the quantitative analysis of the basic building blocks of CMOS analog integrated circuits using the developed equivalent circuit. Section 5 discusses the nonlinear distortion. Finally, Section 6 concludes the paper and points for future work are introduced in Section 7.

2. PREVIOUS WORK

In this section, some of the previous works that are related to designing CMOS analog circuits in modern processes is presented. In [18], a criticism to the rules of thumb for determining the device sizing was discussed and an accurate approach for quick estimation of short-channel transistor sizing was proposed. In [19, 20], the initial sizing for the analog CMOS circuits was investigated and compared in deep-submicron processes in the three different regions of inversion: weak, moderate, and strong. S. Dash et al proposed an approach for determining the optimum design for analog circuits [21]. This approach is based on the analogy with the drops of water when searching for a probable path to flow from high to low altitudes. It is aptly called river formation dynamics. The authors claimed that this scheme is effective when applied to multi-objective problems. G. Gielen et al have proposed analysis tools that identify the variability and reliability problems in analog circuits [17]. In his work, G. Gielen applied the sense-and-react mechanism. This mechanism depends simply on using monitors to monitor the operation of the circuit in a continuous manner, then feed this information to a controller. This controller acts to apply compensating actions on the circuit in order to compensate for any aging-induced errors, thus guaranteeing the proper and optimal operation of the circuit at all times and under all conditions. These circuits are aptly called

aging-resilient or self-healing circuits. Alternatively, feedback and replica circuits can be used [22].

In [23, 24], an automated approach for transistor sizing of cell-level analog circuits in short-channel CMOS processes using SPICE-quality device models and constrained optimization techniques was presented. This approach depends on combining device model equations and Kirchhoff's current law (KCL) equations, thus allowing for simultaneous optimization of transistor sizing and solution of dc operating point and the ability to explore new trade-offs by just properly modifying the specifications instead of having to manipulate a set of weights in a cost function. In [25], N. Makris et al have investigated the effect of temperature on the key design parameters that affect the analog design such as mobility, threshold voltage, slope factor, and DIBL factor. According to this approach, all the transconductances including the output conductance can be estimated in weak and moderate inversions and over a large temperature range.

It was found in [26] that the channel-length modulation and the short-channel effects are very crucial in designing analog circuits with good performance. These two effects can be controlled by both gate oxide thickness and channel engineering techniques. In [27], the effects of stress and reliability on the nanoscale analog circuit design have been investigated and alteration to device geometries in order to mitigate these effects was studied. This is in order to avoid deficiencies after post layout extraction and the associated relay out, thus reducing the time to market. Finally, a previous study developed an empirical relationship of the drain current in the saturation region that is valid in deep-submicron technologies [28].

3. ADOPTED MOSFET TRANSISTOR MODEL AND DEVELOPED EQUIVALENT CIRCUIT

In this section, the mathematical large-signal model adopted for the short-channel MOS transistor, which is adopted in this paper, is presented. Also, the small-signal low-frequency equivalent circuit for the MOS transistor in saturation is developed using the adopted model.

In spite of its popularity and simplicity, the Shichman-Hodges square-law MOSFET model [29] will not be adopted in this paper. This is due to the fact that it overestimates the drain current as it completely ignores the velocity-saturation and mobility-degradation effects which are very significant in short-channel devices [30].

The velocity-saturation effect can be taken into account by raising the gate-overdrive voltage to the power, a, which varies between 1 and 2 [31] with a equal to 2 for long-channel devices in which the velocity-saturation effect can be neglected altogether and a approaches 1 (corresponding to the linear model) as the velocity-saturation effect gets severer [30]. a equals 1 in the case of full velocity saturation.

The most important trade-off that is encountered in selecting a suitable model for the quantitative analysis is "simplicity versus accuracy." As a compromise between these two conflicting requirements, the following linear model will be adopted. When V_{GS} is smaller than V_{thn}, the device operates in the subthreshold region. In this case, the drain current can be expressed as follows [32]:

$$I_D = I_{0n} e^{\left(\frac{V_{GS}-V_{thn}}{n_n V_{th}}\right)} \left[1 - e^{-\frac{V_{DS}}{V_{th}}}\right] \quad (1)$$

where I_{0n} is given by:

$$I_{0n} = \mu_{0n} C_{0x} \left(\frac{W}{L} \right)_n (n_n - 1) V_{th}^2 \quad (2)$$

V_{th} is the thermal voltage which can be found from:

$$V_{th} = \frac{KT}{q} \quad (3)$$

n_n is given by [33]:

$$n_n = 1 + \frac{C_d}{C_{ox}} \quad (4)$$

The threshold voltage of a short-channel MOSFET transistor varies with V_{SB} and V_{DS} according to the following relationship [12]:

$$V_{thn} \approx V_{thn0} + \gamma V_{SB} - \eta V_{DS} \quad (5)$$

Now, when V_{GS} is larger than V_{thn} and V_{DS} is smaller than V_{DSsat}, M operates in the triode region with a drain current given by:

$$I_D = \mu_{eff} C_{ox} \left(\frac{W}{L} \right)_n \left[(V_{GS} - V_{thn}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (6)$$

μ_{eff} can be expressed as [34]:

$$\mu_{eff} = \frac{\mu_{0n}}{1 + \theta (V_{GS} - V_{thn})} \quad (7)$$

V_{DSsat} is given by

$$V_{DSsat} = (1 - k)(V_{GS} - V_{thn}) \quad (8)$$

where k is given by:

$$k = \frac{1}{1 + \frac{2 v_{sat} L}{\mu_{eff} (V_{GS} - V_{thn})}} \quad (9)$$

It is obvious from the previous equations that there is an interdependence between these equations due to the existence of the parameter, k. For typical parameters of the nanometer CMOS technologies, k can be put equal to 0 and thus its effect can be neglected safely throughout this paper. When V_{GS} is larger than V_{thn} and V_{DS} is larger than V_{DSsat}, M operates in the saturation region. Assuming full velocity saturation, the drain current can be written as [35]:

$$I_D = W C_{ox} v_{sat} (V_{GS} - V_{thn})(1 + \lambda V_{DS}) \quad (10)$$

It must be noted that the word "saturation" here is related to the saturation of the carriers' velocity with increasing the electric field and not the constancy of the drain current with the drain-to-source voltage [36].

3.1. Small-Signal Analysis

Adopting the same philosophy in deriving the small-signal equivalent circuit for the long-channel MOSFET transistor [37], we will assume that an ac signal with a small value is superimposed on the dc voltage applied on the gate terminal. So, the total gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs} \quad (11)$$

where v_{GS} (with small symbol and capital subscript) denotes the total instantaneous value including the dc and ac values, V_{GS} (with capital symbol and subscript) denotes the pure dc voltage, and v_{gs} (with small symbol and subscript) denotes the pure ac voltage. Substituting v_{GS} from Eq. (11) into Eq. (10) results in the total drain current in saturation being:

$$i_D = WC_{ox}v_{sat}\left(V_{GS} + v_{gs} - V_{thn}\right) \tag{12}$$

where λ is assumed to be zero for simplifying the analysis. The drain current is thus the sum of two currents; the first one is the pure dc drain current which is equal to:

$$I_D = WC_{ox}v_{sat}\left(V_{GS} - V_{thn}\right) \tag{13}$$

and the pure ac drain current which is equal to:

$$i_d = WC_{ox}v_{sat}v_{gs} \tag{14}$$

i.e.

$$i_D = I_D + i_d \tag{15}$$

with I_D and i_d given by Eqs. (13) and (14), respectively. An obvious difference between the short-channel and long-channel devices is that there is no restriction on the value of the gate-to-source signal voltage in order to ensure linearity. This is in contrast to the long-channel case in which the ac gate-to-source voltage is restricted to satisfy the following condition [37]:

$$v_{gs} << 2\left(V_{GS} - V_{thn}\right) \tag{16}$$

So, the nonlinear distortion in short-channel devices is expected to be less than that in long-channel devices; a point that will be confirmed in Section 5.

3.2. Small-Signal Low-Frequency Equivalent Circuit

In order to develop the small-signal low-frequency equivalent circuit of the short-channel MOS transistor, it can be noted that the ac drain current, i_d, depends on the following voltages:

1. The gate-to-source voltage through the transistor transconductance.
2. The drain-to-source voltage through two effects; the channel-length modulation and DIBL effects; and
3. The substrate-to-source voltage through the body effect.

So, i_d can be represented as follows:

$$i_d = g_m v_{gs} + g_{mb}v_{bs} + g_{md}v_{ds} + g_{ds}v_{ds} \tag{17}$$

where g_m, g_{mb}, and g_{md} are the transconductances of the gate, body, and drain, respectively. g_{ds} represents the variation of the drain current with the drain-to-source voltage due to the channel-length modulation effect. To derive the relationships for these parameters, we define the gate transconductance as the ratio between the variation of the drain current and that of the gate-to-source voltage with constant v_{BS} and v_{DS}. So,

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \ (v_{BS} \text{ and } v_{DS} = \text{constants}) \tag{18}$$

From Eq. (12), we get

$$g_m = WC_{ox}v_{sat} \tag{19}$$

which is a constant value that can be determined by parameters related to the process technology and the device channel width. This is in contrast to the transconductance of the long-channel square-law device which is dependent on both the biasing conditions, the technology, and the device dimensions. Since g_m does not depend on the biasing current, the

only way to increase the transconductance and hence the voltage gain is to make the device wider as g_m is proportional to W. The sensitivity of g_m to W in short-channel devices is larger than that in long-channel devices in which g_m is proportional to $\sqrt{W}$ for a constant drain current as evident from [37]:

$$g_m = \sqrt{2k_n'\left(\frac{W}{L}\right)_n I_D}\,. \tag{20}$$

g_{mb}, g_{md}, and g_{ds} can be defined in a similar manner as follows:

$$g_{mb} = \frac{\partial i_D}{\partial v_{BS}}\ (v_{GS} \text{ and } v_{DS} = \text{constants}) = \frac{\partial i_D}{\partial V_{thn}}\frac{\partial V_{thn}}{\partial v_{BS}} \tag{21}$$

From Eqs. (12) and (5), we get

$$\frac{\partial i_D}{\partial V_{thn}} = -WC_{ox}v_{sat} \tag{22}$$

and

$$\frac{\partial V_{thn}}{\partial v_{BS}} = -\gamma \tag{23}$$

respectively. So,

$$g_{mb} = \gamma WC_{ox}v_{sat} = \gamma g_m \tag{24}$$

Finally, g_{md} can be defined as follows:

$$g_{md} = \frac{\partial i_D}{\partial V_{thn}}\frac{\partial V_{thn}}{\partial v_{DS}} \tag{25}$$

From Eq. (5), we get

$$\frac{\partial V_{thn}}{\partial v_{DS}} = -\eta \tag{26}$$

So,

$$g_{md} = \eta WC_{ox}v_{sat} = \eta g_m \tag{27}$$

Finally, g_{ds} (the drain conductance) can be found from

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}}\ (v_{GS}, v_{BS} = \text{constants}) = \lambda WC_{ox}v_{sat}\left(V_{GS} - V_{thn}\right) = \lambda I_D \tag{28}$$

So,

$$r_o = \frac{1}{g_{ds}} = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}, \tag{29}$$

where r_o is the drain resistance and V_A is the Early voltage. Eq. (29) is similar to its long-channel counterpart. The small-signal ac equivalent circuit for the short-channel MOSFET device can thus be drawn as shown in Fig. 1(a).

Now, since v_{ds} is the voltage applied across the terminals of the dependent voltage-controlled current source, $g_{md}v_{ds}$, then the source-absorption theorem can be applied here [37]. Thus, the dependent current source, $g_{md}v_{ds}$, can be replaced by a resistance equal to the inverse of the controlling factor, g_{md} (= ηg_m). So, the circuit can be reduced as shown in Figs. 1(b) and 1(c). In other words, the DIBL effect can be taken into account in the small-signal analysis of the short-channel MOS devices simply by replacing r_o by $r_o//(1/\eta g_m)$. The reduction of the output resistance of the NMOS transistor in short-channel devices reflects the degraded performance in current sources implemented using saturation-region operated MOSFET

devices. Also (taking into account that the body terminal is ac-grounded), if the gate is ac-grounded, the body effect can be taken into account simply by replacing each g_m by $g_m + g_{mb} = g_m (1 + \gamma)$.

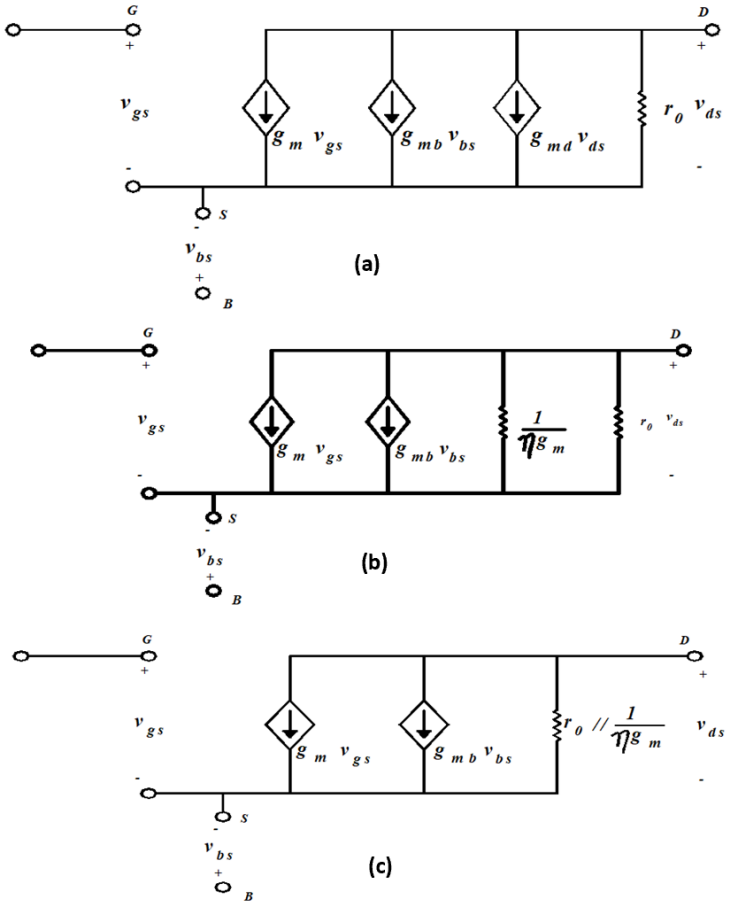

Fig. 1. a) The small-signal AC equivalent circuit for the short-channel MOSFET transistor; b) the circuit of (a) with the source-absorption theorem applied; c) the circuit of (b) with the two resistances, r_o and $1/\eta g_m$, combined in parallel.

If the short-channel MOSFET device is operated in the triode region, then

$$i_D = \frac{\mu_{0n}}{1+\theta(v_{GS}-V_{thn})} C_{ox}\left(\frac{W}{L}\right)_n \left[(v_{GS}-V_{thn})v_{DS} - \frac{1}{2}v_{DS}^2\right] \tag{30}$$

So,

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{\mu_{0n}C_{ox}}{1+\theta(v_{GS}-V_{thn})}\left(\frac{W}{L}\right)_n v_{DS} - \mu_{0n}C_{ox}\left(\frac{W}{L}\right)_n \left[(v_{GS}-V_{thn})v_{DS} - \frac{1}{2}v_{DS}^2\right]\frac{\theta}{\left[1+\theta(v_{GS}-V_{thn})\right]^2} \tag{31}$$

For deep-triode region in which v_{DS} is small compared to $2(v_{GS} - V_{thn})$, we can neglect the term $1/2v_{DS}^2$ relative to $(v_{GS} - V_{thn})v_{DS}$, so

$$g_m \approx \frac{\mu_{0n}C_{ox}}{1+\theta(v_{GS}-V_{thn})}\left(\frac{W}{L}\right)_n v_{DS} - \mu_{0n}C_{ox}\left(\frac{W}{L}\right)_n \frac{\theta(v_{GS}-V_{thn})v_{DS}}{\left[1+\theta(v_{GS}-V_{thn})\right]^2}$$

$$= \frac{\mu_{0n}C_{ox}}{1+\theta(v_{GS}-V_{thn})}\left(\frac{W}{L}\right)_n v_{DS}\left[1 - \frac{\theta(v_{GS}-V_{thn})}{1+\theta(v_{GS}-V_{thn})}\right] \tag{32}$$

which is very nonlinear. So, the use of the MOSFET transistor as an amplifier in the triode region is avoided which is also the case with long-channel devices. In deep-triode region, the drain current can be written as:

$$i_D = \frac{\mu_{0n}}{1+\theta(v_{GS}-V_{thn})} C_{ox}\left(\frac{W}{L}\right)_n (v_{GS}-V_{thn})v_{DS} \tag{33}$$

The MOSFET transistor can thus be utilized as a voltage-controlled resistance as its long-channel counterpart except that the sensitivity to the controlling voltage, v_{GS}, is degraded due to the mobility-degradation effect.

3.3. Unity-Gain Frequency

An important transistor parameter that is used to indicate the intrinsic speed of the transistors is the unity-gain frequency. The unity-gain frequency is defined as the frequency at which the short-circuit current gain of the common-source amplifier configuration becomes unity [37]. Adopting the small-signal equivalent circuit of Fig. 1(c) and adding the two internal capacitances, C_{GS} and C_{GD}, it can be shown that:

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{34}$$

the same expression as that of the long-channel devices; an expected result as short-circuiting the drain and source terminals eliminates the effects of the channel-length modulation and the DIBL. For typical values of C_{GS} and C_{GD}, C_{GS} is much larger than C_{GD}. So, neglecting C_{GD} in Eq. (34) and substituting C_{GS} by $2/3WLC_{ox}$ [37] and g_m by $WC_{ox}v_{sat}$ result in

$$f_T \approx \frac{WC_{ox}v_{sat}}{2\pi.\frac{2}{3}WLC_{ox}} = \frac{3v_{sat}}{4\pi L} \tag{35}$$

It is apparent that as the minimum feature size, L, is decreased with technology scaling, f_T increases. Intuitively, a smaller device has smaller internal capacitances, and the charge carrier must travel a shorter distance in it in order to keep pace with the change in the input signal, thus obtaining a higher speed. If compared with the long-channel device, g_m is to be substituted in Eq. (34) by [37]:

$$g_m = \mu_{on}C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{thn}) \tag{36}$$

So, the corresponding expression for f_T in long-channel devices is:

$$f_T \approx \frac{\mu_{on}C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{thn})}{2\pi.\frac{2}{3}WLC_{ox}} = \frac{3\mu_{on}(V_{GS} - V_{thn})}{4\pi L^2} \tag{37}$$

So, f_T increases with the decrease in the minimum feature size in both long-channel and short-channel devices; however, with a larger increasing rate with long-channel devices due to the dependence on $1/L^2$. In fact, for devices with channel lengths smaller than 45 nm, f_T may reach 100 GHz. So, it can be expected that the design of circuits in CMOS technology operating at around 10 GHz can be rather systematic and straightforward. However, with the continued downscaling of CMOS devices, there are some challenges that are associated with the design of radiofrequency (RF) circuits in CMOS technology.

It must be noted that the transit frequency is estimated for the maximum value of V_{DD}. This is not the case in practical circuits, as approximately half V_{DD} is typically applied. Consequently, the transit frequency of a transistor in practical circuits is significantly lower; typically, 50% smaller [38]. The reader can refer to [39] for the relationship between the transit frequency and the drain current at different drain-to-source voltages for a 100-nm CMOS technology. Secondly, due to the reduction of the V_{DD}/V_{thn} ratio with technology scaling, the overdrive voltage decreases.

Refer to Fig. 2 for a qualitative plot for the dependence of f_T on $1/L$ [40]. It must be noted, however, that when operating in the subthreshold regime, f_T is given by [41]:

$$f_T = \frac{1}{2\pi} \frac{I_D}{50\varepsilon_{ox} n_n V_{th} W} \tag{38}$$

Thus, the unity-gain frequency, and correspondingly the intrinsic device speed, do not increase with decreasing the channel length at these low current levels.

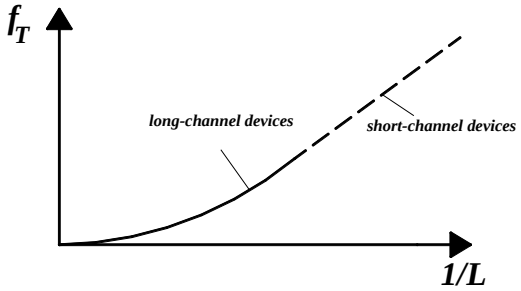

Fig. 2. Dependence of f_T on the inverse of the channel length in both long-channel and short-channel devices [40].

4. BUILDING BLOCKS OF ANALOG INTEGRATED CIRCUITS

In this section, the basic building blocks of analog integrated circuits such as single-stage amplifiers, cascode stages, current mirror, differential amplifier, composite transistor, op-amp, and low-noise amplifier, will be analyzed quantitatively using the small-signal equivalent circuit developed in Section 3.

4.1 Single-Stage Amplifiers

Refer to Fig. 3 for a common-source MOSFET transistor, M, loaded by a resistive load, R_D. We will first perform the large-signal analysis. When v_{in} is smaller than V_{thn}, M operates in the subthreshold region, thus the input-output relationship is given by:

$$I_{0n} e^{\left(\frac{v_{in}-V_{thn}}{n_n V_{th}}\right)} \left[1 - e^{-\frac{v_{out}}{V_{th}}}\right] = \frac{V_{DD} - v_{out}}{R_D} \tag{39}$$

The voltage gain can be found by differentiating Eq. (39) with respect to v_{in} or, alternatively, one can resort to [42] for the small-signal equivalent circuit of the MOS transistor in the subthreshold region. However, operating the MOS transistor as an amplifier in the subthreshold region is associated with a very tight voltage headroom. Also, it must be noted that the sensitivity of the drain current to the change in the gate-to-source voltage is larger in the subthreshold region compared to that in the saturation region due to the exponential dependence depicted in Eq. (39).

If v_{in} increases above V_{thn}, i_D begins to flow through R_D and v_{out} lowers. Assuming that V_{DD} is sufficiently large, then M operates in the saturation region, and we have:

$$v_{out}(t) = V_{DD} - R_D W C_{ox} v_{sat} \left(v_{in} - V_{thn}\right)\left(1 + \lambda v_{out}\right) \tag{40}$$

Also,

$$V_{thn} = V_{thn0} - \eta v_{DS} = V_{thn0} - \eta v_{out} \tag{41}$$

and the body effect is absent here. So,

$$v_{out}(t) = V_{DD} - R_D W C_{ox} v_{sat} \left(v_{in} - V_{thn0} + \eta v_{out}\right)\left(1 + \lambda v_{out}\right) \tag{42}$$

Differentiating both sides of Eq. (42) with respect to v_{in}, we obtain:

$$\frac{\partial v_{out}}{\partial v_{in}} = A_v = -R_D W C_{ox} v_{sat}\left(v_{in} - V_{thn0} + \eta v_{out}\right)\left(\lambda A_v\right) - R_D W C_{ox} v_{sat}\left(1+\lambda v_{out}\right)\left(1+\eta A_v\right) \tag{43}$$

from which the voltage gain, A_v, can be derived. The same result can be obtained with the aid of the small-signal equivalent circuit shown in 0Fig. 4.

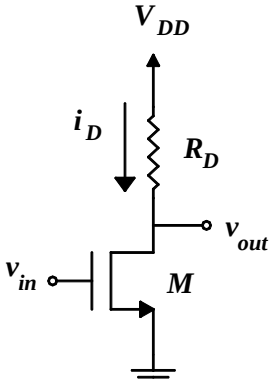

Fig. 3. A common-source stage with a resistive load.

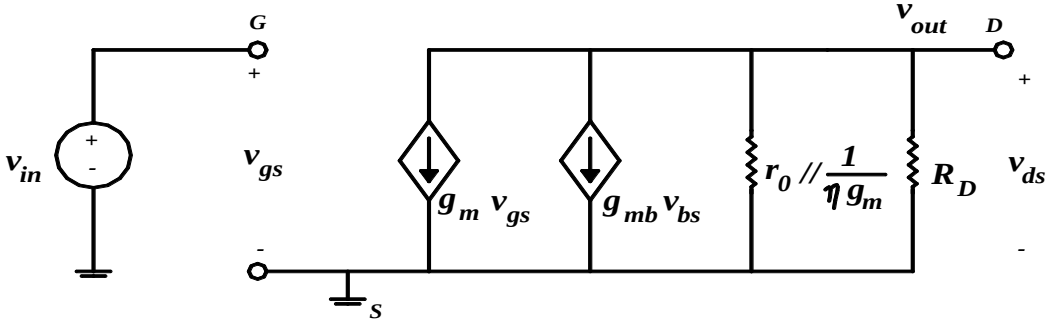

Fig. 4. The small-signal equivalent circuit of Fig. 3.

The body-effect current source, $g_{mb}v_{bs}$, can be replaced by an open circuit, thus:

$$A_v = -g_m\left(r_0 \,//\, \frac{1}{\eta g_m} \,//\, R_D\right) \tag{44}$$

where the voltage gain is obviously lower than its value when neglecting the effects of r_0 and η. In order to gain an insight into the parameters affecting the voltage gain, neglect for the moment the effects of r_0 and η, thus:

$$A_v = -g_m R_D = -WC_{ox} v_{sat} \frac{V_{RD}}{I_D} \tag{45}$$

In contrast to the long-channel device, the transconductance is independent of the input voltage, hence the amplifier is expected to be more linear, a desirable effect. If the resistive load is replaced by an ideal current source, the voltage gain will be the intrinsic one and is given by:

$$A_{v0} = -g_m\left(r_0 \,//\, \frac{1}{\eta g_m}\right) = \frac{-g_m r_0}{1+\eta g_m r_0} \tag{46}$$

Substituting r_o and g_m into Eq. (46) results in

$$A_{v0} = \frac{-WC_{ox} v_{sat}\dfrac{V_A}{I_D}}{1+\eta WC_{ox} v_{sat}\dfrac{V_A}{I_D}} = \frac{-WC_{ox} v_{sat} V_A}{I_D + \eta WC_{ox} v_{sat} V_A} \tag{47}$$

which indicates that the open-circuit voltage gain decreases with the increase in I_D. This is an expected result as the gain in this case is determined by r_0 and g_m while $r_0 = 1/\lambda I_D$ and g_m is independent of I_D.

Now, refer to Fig. 5 for the circuit schematic of the common-source stage with a current-source load that is implemented by a PMOS device.

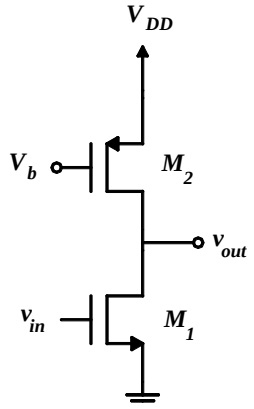

Fig. 5. The circuit schematic of the common-source stage with a PMOS current-source load, M_2.

The voltage gain can be easily found to be:

$$A_v = -g_{m1}\left(r_{01} // \frac{1}{\eta_1 g_{m1}} // r_{02} // \frac{1}{\eta_2 g_{m2}} \right) \tag{48}$$

Note that since the transistor transconductance, g_m, is independent of the signal level, there is no need to add a degeneration-source resistance that was used to linearize the amplifier with its associated reduction in gain. This seems to be an advantage for short-channel devices. Now, the performance of the common-source amplifier with diode-connected load is investigated. The small-signal equivalent resistance, R, of the diode-connected NMOS transistor can be found from the equivalent circuit shown in Fig. 6.

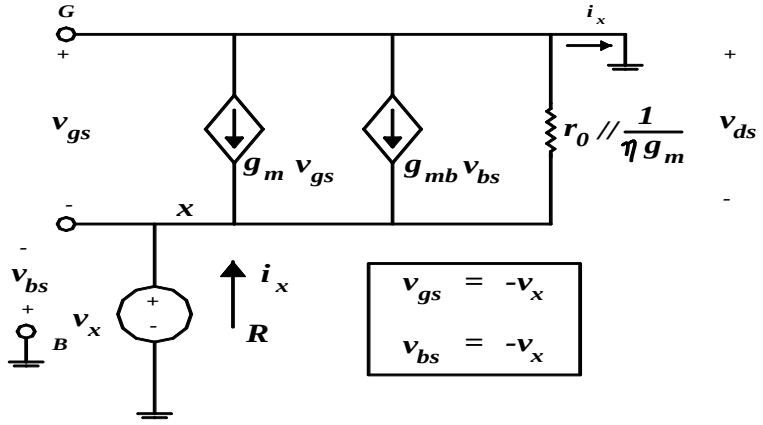

Fig. 6. The small-signal equivalent circuit of the diode-connected MOSFET device.

The resistance, R, can be shown to be given by:

$$R = \frac{v_x}{i_x} = \frac{1}{(g_m + g_{mb})} // r_0 // \frac{1}{\eta g_m} = \frac{1}{g_m(1+\chi+\eta)} // r_0 \tag{49}$$

If the diode–connected MOSFET is used as a load on the common-source amplifier as shown in Fig. 7, then the voltage gain will be:

$$A_v = -g_{m1}\left[r_{01} // \frac{1}{\eta_1 g_{m1}} // \frac{1}{g_{m2}(1+\chi_2+\eta_2)} // r_{02} \right] \tag{50}$$

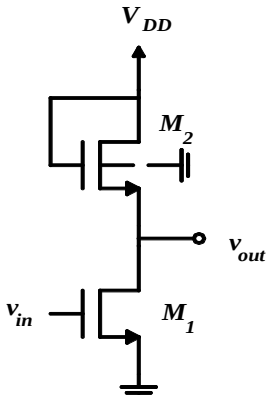

Fig. 7. The diode-connected transistor, M_2, used as a load on the amplifying device, M_1.

The circuit schematic of the source-follower stage is shown in Fig. 8.

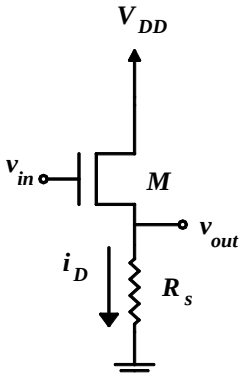

Fig. 8. The circuit schematic of the source-follower stage.

When v_{in} is smaller than V_{thn}, M operates in the subthreshold region and the voltage gain can be found by adopting the equivalent circuit in [42]. When v_{in} exceeds V_{thn}, M operates in saturation. So,

$$v_{out} = i_D R_s = R_s W C_{ox} v_{sat} \left(v_{GS} - V_{thn}\right) \tag{51}$$

where λ is assumed to be zero for simplicity. Considering that:

$$V_{thn} = V_{thn0} - \eta v_{DS} - \gamma v_{BS} = V_{thn0} - \eta\left(V_{DD} - v_{out}\right) - \gamma v_{BS} \tag{52}$$

and

$$v_{GS} = v_{in} - v_{out} \tag{53}$$

then

$$v_{out} = R_s W C_{ox} v_{sat} \left[v_{in} - v_{out} - V_{thn0} + \eta\left(V_{DD} - v_{out}\right) + \gamma v_{BS}\right] \tag{54}$$

Differentiating the above equation with respect to v_{in} results in:

$$\frac{\partial v_{out}}{\partial v_{in}} = A_v = R_s W C_{ox} v_{sat} \left[1 - A_v - \eta A_v + \gamma \frac{\partial v_{BS}}{\partial v_{in}}\right] \tag{55}$$

Now, since

$$v_{out} = v_{SB} \tag{56}$$

as the body is connected to ground, then

$$\frac{\partial v_{BS}}{\partial v_{in}} = -A_v \tag{57}$$

Substituting $\frac{\partial v_{BS}}{\partial v_{in}}$ from Eq. (57) into Eq. (55) results in

$$\therefore A_v = \frac{g_m R_s}{1 + g_m R_s (1 + \eta + \gamma)} \tag{58}$$

The voltage gain can also be found from the small-signal equivalent circuit shown in Fig. 9 as:

$$A_v = \frac{v_{out}}{v_{in}} = g_m \left[R_s // r_0 // \frac{1}{g_m} // \frac{1}{g_{mb}} // \frac{1}{\eta g_m} \right] \tag{59}$$

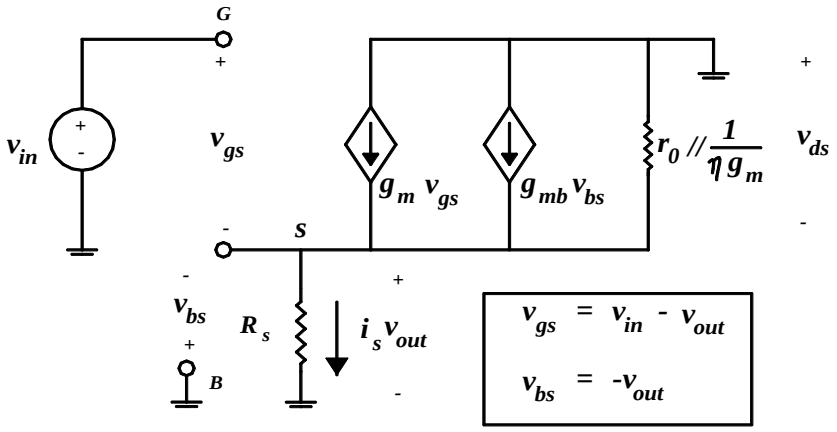

Fig. 9. The small-signal equivalent circuit of the source-follower stage of Fig. 8.

If r_o is assumed to be infinite, the same result as that of Eq. (58) will be obtained. If R_s are r_o are much larger than $1/g_m$, $1/g_{mb}$, and $1/\eta g_m$, then

$$A_v = g_m \left[\frac{1}{g_m} // \frac{1}{g_{mb}} // \frac{1}{\eta g_m} \right] = \frac{1}{1 + \chi + \eta} \tag{60}$$

Thus, the voltage gain of the source-follower stage decreases due to the substrate and DIBL effects. This degrades the performance of the source-follower stage as a voltage buffer. The output resistance of the source-follower stage can be found with the aid of the small-signal equivalent circuit shown in Fig. 10, in which v_{in} is deactivated, as:

$$R_{out} = \frac{v_x}{i_x} = r_0 // \frac{1}{g_m (1 + \chi + \eta)} \tag{61}$$

Refer to Fig. 11 for the circuit schematic of the common-gate stage. When M operates in saturation, we have:

$$v_{out} = V_{DD} - i_D R_D = V_{DD} - R_D W C_{ox} v_{sat} (V_b - v_{in} - V_{thn}) \tag{62}$$

where V_b is the gate-biasing voltage. Differentiating both sides of Eq. (62) with respect to v_{in}, we obtain:

$$\frac{\partial v_{out}}{\partial v_{in}} = -R_D W C_{ox} v_{sat} \left(0 - 1 - \frac{\partial V_{thn}}{\partial v_{in}} \right) \tag{63}$$

Since

$$V_{thn} = V_{thn0} - \eta v_{out} + \eta v_{in} + \gamma v_{in} \tag{64}$$

as the body is connected to ground, then:

$$A_v = -g_m R_D (-1 + \eta A_v - \eta - \gamma) \tag{65}$$

So, the voltage gain is given by:

$$A_v = \frac{g_m R_D (1+\eta+\gamma)}{1+g_m R_D} \tag{66}$$

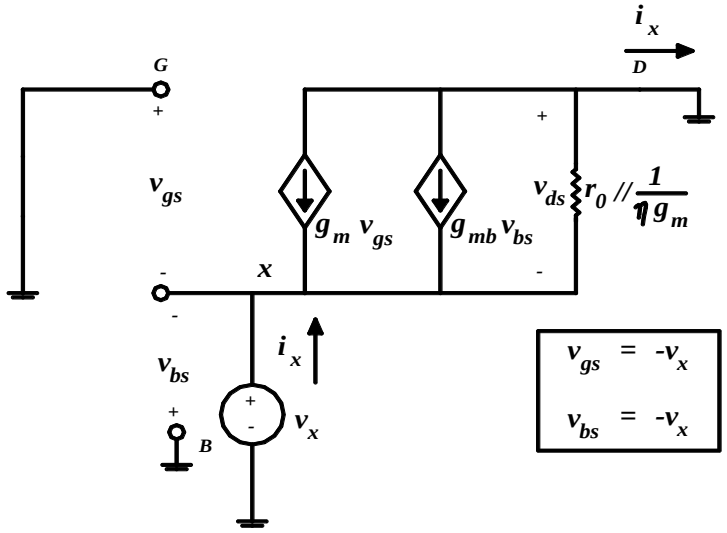

Fig. 10. The small-signal equivalent circuit used to find the output resistance of the source-follower stage.

It is obvious from Eq. (66) that the body and DIBL effects increase the voltage gain. Intuitively, the body effect causes the threshold voltage to increase with the increase in v_{in}, thus decreasing i_D and increasing v_{out}, i.e. obtaining a larger v_{out} for the same v_{in} which means an increase in the voltage gain. The small-signal analysis yields a voltage gain equal to:

$$A_v = \left(R_D // r_0 // \frac{1}{\eta g_m} \right) \left[g_m (1+\eta+\chi) // \frac{1}{r_0} \right] \tag{67}$$

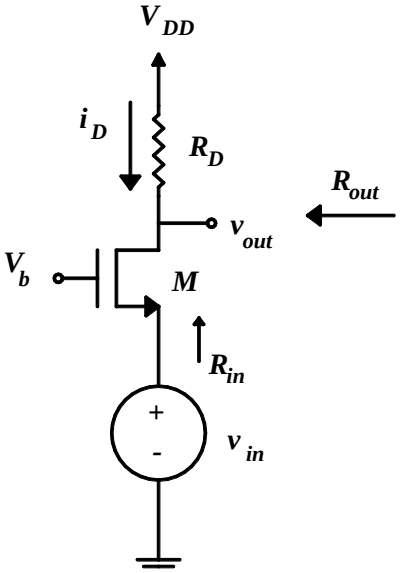

Fig. 11. The circuit schematic of the common-gate stage.

Now, for evaluating the input resistance, R_{in}, refer to Fig. 12 for the common-gate stage. R_{in} is given by:

$$R_{in} = \frac{v_x}{i_x} = \frac{R_D + \left(r_0 // \frac{1}{\eta g_m} \right)}{1 + (g_m + g_{mb}) \left(r_0 // \frac{1}{\eta g_m} \right)} \tag{68}$$

Interestingly, the body effect decreases the input resistance of the common-gate stage making it more suitable for use as a current buffer. This can be explained intuitively as follows: If the source voltage increases, there will be two supporting effects; the first one is the decrease in i_D due to decreasing v_{GS} and the second is the increase in V_{thn} due to the body effect. The result is that the current decreases by a larger amount due to the body effect, thus a decrease in the input resistance results. However, the body-effect parameter deceases with technology scaling [43]. Obviously, if the internal resistance of the input-signal source were taken into account, it would appear in series with the input resistance just found. Finally, the output resistance can be found as:

$$R_{out} = R_D // r_o // \frac{1}{\eta g_m} \tag{69}$$

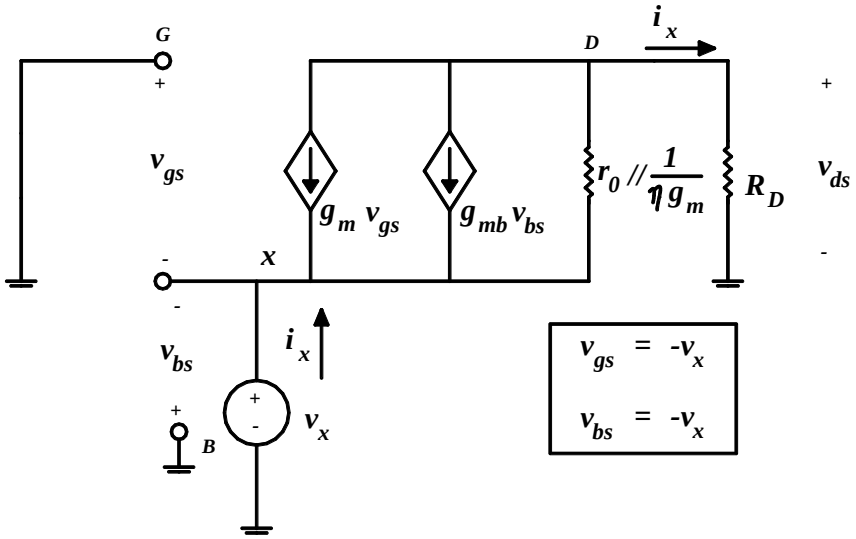

Fig. 12. The small-signal equivalent circuit used to find the input resistance of the common-gate stage.

Now, investigating the cascode stage is in order. As known, the cascode stage increases the output resistance of the amplifying device and in turn the voltage gain increases. Refer to Fig. 13 for the circuit schematic of the cascode stage [14]. Since

$$R_{out1} = r_{o1} // \frac{1}{\eta_1 g_{m1}} \tag{70}$$

then

$$R_{out} = \left[1 + \left(g_{m2} + g_{mb2}\right)\left(r_{02} // \frac{1}{\eta_2 g_{m2}}\right)\right]\left(r_{01} // \frac{1}{\eta_1 g_{m1}}\right) + \left(r_{01} // \frac{1}{\eta_1 g_{m1}}\right) \tag{71}$$

So, R_{out} can be approximated to:

$$R_{out} \approx \left[1 + \left(g_{m2} + g_{mb2}\right)\left(r_{o2} // \frac{1}{\eta_2 g_{m2}}\right)\right]\left(r_{o1} // \frac{1}{\eta_1 g_{m1}}\right) \tag{72}$$

If the following inequality applies

$$\left(g_{m2} + g_{mb2}\right)\left(r_{02} // \frac{1}{\eta_2 g_{m2}}\right) >> 1 \tag{73}$$

Then

$$R_{out} \approx \left(g_{m2} + g_{mb2}\right)\left(r_{o2} // \frac{1}{\eta_2 g_{m2}}\right)\left(r_{o1} // \frac{1}{\eta_1 g_{m1}}\right) \tag{74}$$

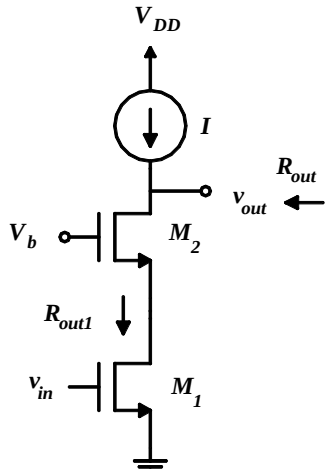

Fig. 13. The circuit schematic of the cascode stage.

That is, M_2 boosts the output impedance of M_1 by a factor equal to the intrinsic gain of the cascode transistor, M_2. An important note must be referred to here: The first one is that the intrinsic gain of M_2 decreases with technology scaling, thus the enhancement in the output resistance by cascoding decreases. Thus, there will be a bad need to use more than two stacked devices with the associated decrease in the allowable voltage swing [44]. The good news, however, is that the additional voltage headroom decreases with technology scaling. This is due to the fact that the minimum additional voltage required by each device to be in saturation is (1 - k) (v_{GS} – V_{thn}) keeping in mind that k increases with technology scaling.

4.2 Current Mirror

Due to the dependence of the drain current on the channel width not the aspect ratio in the saturation region, the current-mirroring ratio between the output and reference currents in a MOS current mirror is also related to the device widths not the aspect ratios. This is a very important result. Another important issue should be considered here. The MOS devices operating as current sources should be fabricated with relatively long channel lengths. This is due to the dependence of the output resistance of the current source in a direct-proportion manner on the channel length, L, through the following relationship:

$$R_{out} = r_o = \frac{V_A}{I_D} = \frac{V_A^{'} L}{I_D} \tag{75}$$

where r_0, V_A, V_A', and I_D are the output resistance of the MOS device in saturation, the Early voltage, the Early voltage per unit channel length, and the dc drain current, respectively. So, in order to obtain a good current source, the channel length, L, should be increased which is a typical design convention [45, 46]. In older CMOS technologies, the channel width needs also to be increased in order to keep the drain current at a certain level and in order not to degrade the circuit's performance. However, in deep-submicron CMOS technologies, the matter differs and there is no need to scale the channel width with the channel length in order to keep their ratio intact.

4.3 Differential Amplifier

In this section, the large-signal analysis of the MOS differential amplifier is performed using the adopted MOS model. Refer to Fig. 14 for the MOS differential pair.

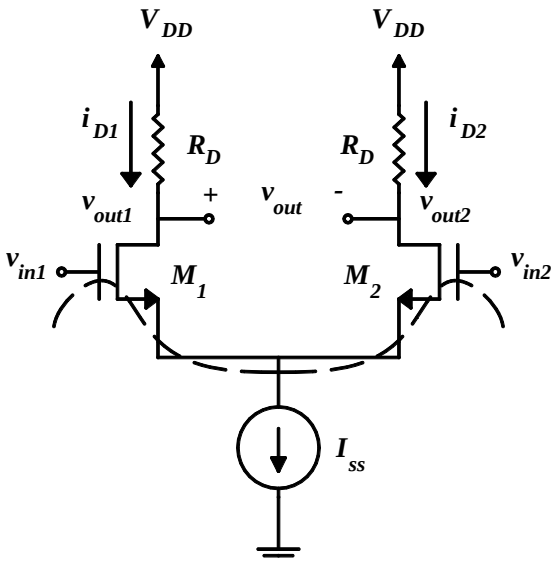

Fig. 14. The circuit schematic of the MOS differential amplifier.

By KVL around the indicated dashed loop, we get:

$$-v_{in1}+v_{GS1}-v_{GS2}+v_{in2}=0$$

$$\therefore v_{in1}-v_{in2}=v_{GS1}-v_{GS2} \tag{76}$$

For a short-channel MOS device operating in saturation, we have (neglecting the channel-length modulation for simplicity):

$$i_D = WC_{ox}v_{sat}(v_{GS} - V_{thn})$$

$$\therefore v_{GS} = V_{thn} + \frac{i_D}{WC_{ox}v_{sat}} \tag{77}$$

Substituting v_{GS} from Eq. (77) into Eq. (76) results in

$$v_{in1}-v_{in2}=\frac{\left(i_{D1}-i_{D2}\right)}{WC_{ox}v_{sat}} \tag{78}$$

The two sides were assumed to be perfectly matched. Now, the single-ended output voltages, v_{out1} and v_{out2}, can be evaluated from

$$v_{out1}=V_{DD}-i_{D1}R_D \tag{79}$$

and

$$v_{out2}=V_{DD}-i_{D2}R_D \tag{80}$$

respectively. The differential output voltage, v_{out}, is thus

$$v_{out}=v_{out1}-v_{out2}$$

$$\therefore v_{out}=-R_D\left(i_{D1}-i_{D2}\right) \tag{81}$$

From Eq. (78), we have:

$$(i_{D1} - i_{D2}) = WC_{ox}v_{sat}(v_{in1} - v_{in2}) \tag{82}$$

and since

$$i_{D1}+i_{D2}=I_{ss} \tag{83}$$

we get

$$i_{D1}=\frac{I_{ss}}{2}+\frac{WC_{ox}v_{sat}\left(v_{in1}-v_{in2}\right)}{2} \tag{84}$$

and

$$i_{D2} = \frac{I_{ss}}{2} - \frac{WC_{ox}v_{sat}\left(v_{in1} - v_{in2}\right)}{2} \tag{85}$$

Recognizing $WC_{ox}v_{sat}$ as g_m and $v_{in1} - v_{in2}$ as Δv_{in}, we have:

$$i_{D1} = \frac{I_{ss}}{2} + \frac{g_m \Delta v_{in}}{2} \tag{86}$$

and

$$i_{D2} = \frac{I_{ss}}{2} - \frac{g_m \Delta v_{in}}{2} \tag{87}$$

The value of the differential input voltage, Δv_{in1}, at which the current source, I_{ss}, is entirely steered into the M_1 branch, can be found from Eq. (84) by putting i_{D1} equal to I_{ss} and $(v_{in1} - v_{in2})$ equal to Δv_{in1}. So,

$$\Delta v_{in1} = \frac{I_{ss}}{WC_{ox}v_{sat}} = \frac{I_{ss}}{g_m} \tag{88}$$

By the same token, if $(v_{in1} - v_{in2})$ is equal to $-\Delta v_{in1}$, the current source, I_{ss}, is entirely steered into the M_2 branch. Refer to Figs. 15 and 16 for $(i_{D1} - i_{D2})$ and $v_{out} = (v_{out1} - v_{out2})$ versus $(v_{in1} - v_{in2})$, respectively. Substituting $(i_{D1} - i_{D2})$ from Eq. (82) into Eq. (81) results in:

$$v_{out} = -R_D WC_{ox}v_{sat}\left(v_{in1} - v_{in2}\right) \tag{89}$$

So, the small-signal *differential* voltage gain is:

$$A_v = \frac{v_{out}}{\left(v_{in1} - v_{in2}\right)} = -R_D WC_{ox}v_{sat} = -g_m R_D \tag{90}$$

The equivalent transconductance of M_1 and M_2 denoted by G_m is:

$$G_m = \frac{\Delta i_D}{\Delta v_{in}} = \frac{i_{D1} - i_{D2}}{v_{in1} - v_{in2}} = WC_{ox}v_{sat} = g_{m1} = g_{m2} \tag{91}$$

The equilibrium overdrive voltage, $(v_{GS} - V_{thn})_{equil}$, is defined as the overdrive voltage of M_1 or M_2 at which $i_{D1} = i_{D2} = I_{ss}/2$ for a zero differential input voltage. So, from Eq. (77), we have:

$$\left(v_{GS} - V_{thn}\right) = \frac{i_D}{WC_{ox}v_{sat}}$$

$$\therefore \left(v_{GS} - V_{thn}\right)_{equil} = \frac{I_{ss}}{2WC_{ox}v_{sat}} \tag{92}$$

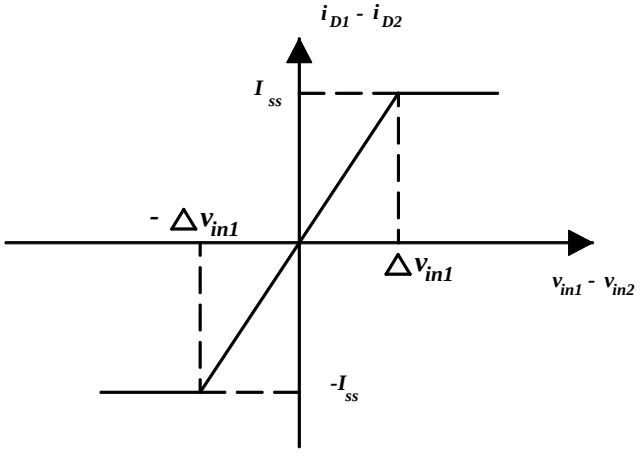

Fig. 15. The variation of $(i_{D1} - i_{D2})$ versus $(v_{in1} - v_{in2})$; (note the perfectly linear relationship).

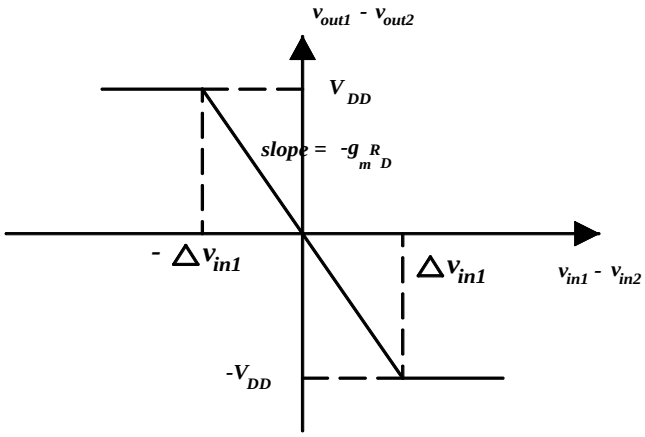

Fig. 16. The variation of ($v_{out1} - v_{out2}$) versus ($v_{in1} - v_{in2}$); (note the perfectly linear relationship).

which is equal to $\Delta v_{in1}/2$. The relationships in Figs. 15 and 16 revealed that there is no need to increase I_{ss} as with the case of long-channel devices with the associated increase in power consumption in order to enhance the linearity of the differential pair [14]. This is in contrast to the long-channel MOS differential amplifier. One of the main disadvantages of the long-channel MOS differential amplifier is its nonlinearity which necessitates the use of a compensating square-root circuit to obtain a linear differential amplifier [47].

Finally, since the drain current is proportional to the gate-overdrive voltage in deep-submicron technologies, the voltage difference required to steer the entire current into one of the branches is $2V_{OV}$ compared to $\sqrt{2}\,V_{OV}$ in the long-channel devices. Thus, the speed of the MOS current-mode logic (MCML) family is expected to decrease.

4.4 Cascode-Differential Amplifier

For the cascode-differential amplifier shown in Fig. 17 [14], the voltage gain is given by [14]:

$$A_v \approx -g_{m3} r_{o3} g_{m1} r_{o1} \tag{93}$$

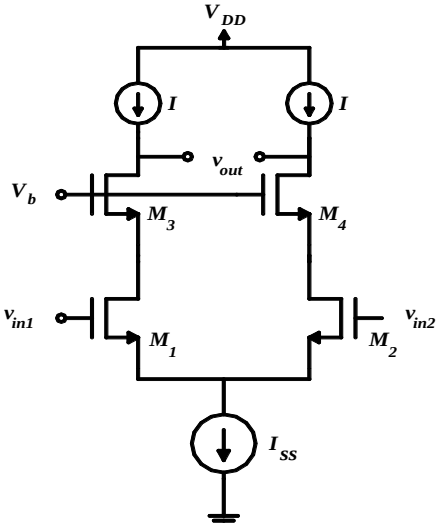

Fig. 17. The circuit schematic of the cascode-differential amplifier.

In case of identical device dimensions and biasing, we obtain:

$$g_{m1} = g_{m3} = g_m \tag{94}$$

and

$$r_{o1} = r_{o3} = r_o \tag{95}$$

Then,

$$A_v \approx -g_m^2 r_0^2 \tag{96}$$

Since g_m is constant and does not change with the channel length while r_o is directly proportional to the channel length, the voltage gain of the cascode-differential amplifier is expected to be directly proportional to the square of the channel length. This is in contrast to the long-channel devices in which g_m increases with decreasing the channel length for a constant gate-overdrive voltage. In this case, the gain will not change with decreasing L. So, the voltage gain is expected to degrade faster with device scaling in short-channel devices. The same conclusion can be drawn for the telescopic cascode-differential amplifier.

As a final note, since the common-mode rejection ratio (CMRR) of the differential amplifier is directly proportional to the output resistance of the MOS transistor realizing the biasing current source [37] and since the latter depends on the channel length in a direct manner also, it is expected that the CMRR degrades with scaling down the channel length. Thus, the immunity of the differential amplifier to the mismatch effects is expected to degrade.

4.5 CMOS Composite Transconductor

CMOS composite transconductors have applications in voltage-controlled resistors, integrators, floating inductors, continuous-time filters, and phase-locked loops [48 - 50]. It can be implemented using the circuit schematic shown in Fig. 18.

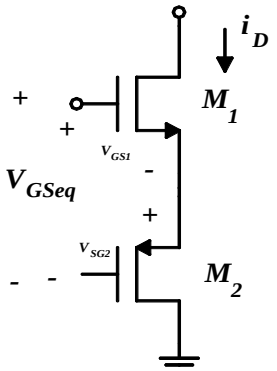

Fig. 18. The circuit schematic of the CMOS composite transconductor.

Assuming that M_1 and M_2 are saturated and neglecting λ, χ, and η for simplifying the analysis, we obtain:

$$i_{D1} = W_1 C_{ox} v_{sat} \left(v_{GS1} - V_{thn} \right) \tag{97}$$

$$i_{D2} = W_2 C_{ox} v_{sat} \left(v_{SG2} - \left| V_{thp} \right| \right) \tag{98}$$

So,

$$v_{GS1} = V_{thn} + \frac{i_D}{W_1 C_{ox} v_{sat}} \tag{99}$$

and

$$v_{SG2} = \left| V_{thp} \right| + \frac{i_D}{W_2 C_{ox} v_{sat}} \tag{100}$$

So, the voltage v_{GSeq} is:

$$v_{GSeq} = v_{GS1} + v_{SG2} = V_{thn} + \left|V_{thp}\right| + i_D\left[\frac{1}{W_1 C_{ox} v_{sat}} + \frac{1}{W_2 C_{ox} v_{sat}}\right] \tag{101}$$

Defining the equivalent threshold voltage as:

$$V_{theq} = V_{thn} + \left|V_{thp}\right| \tag{102}$$

and the equivalent device transconductance parameter as:

$$k_{eq} = \frac{k_1 k_2}{k_1 + k_2} \tag{103}$$

where

$$k_1 = W_1 C_{ox} v_{sat} \tag{104}$$

and

$$k_2 = W_2 C_{ox} v_{sat} \tag{105}$$

we arrive at the equivalence shown in Fig. 19.

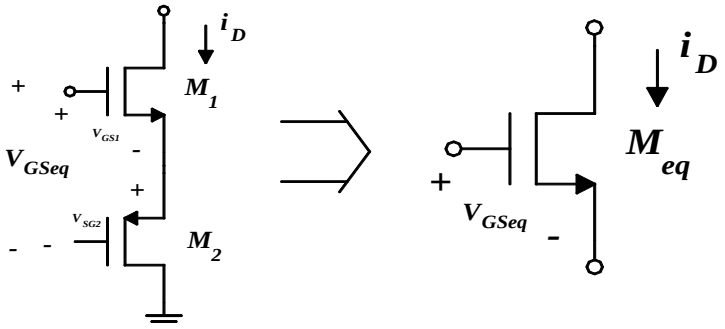

Fig. 19. The equivalence of the CMOS composite transconductor with a single NMOS transistor.

Now, the circuit schematic of the single-ended transconductor is shown in Fig. 20.

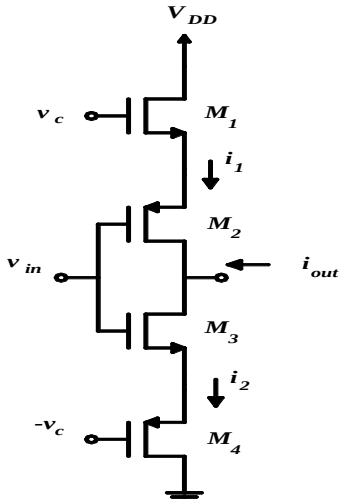

Fig. 20. The circuit schematic of the single-ended CMOS transconductor.

The output current can be found from:

$$i_{out} = i_2 - i_1 \tag{106}$$

where i_1 and i_2 are the currents of the composite transconductors (M_1 and M_2) and (M_3 and M_4), respectively. So,

$$i_1 = k_{1eq}\left(v_c - v_{in} - V_{theq}\right) \tag{107}$$

$$i_2 = k_{2eq}\left(v_{in} + v_c - V_{theq}\right) \tag{108}$$

Thus,

$$i_{out} = i_2 - i_1 = 2k_{eq}v_{in} \tag{109}$$

where

$$k_{1eq} = k_{2eq} = k_{eq} \tag{110}$$

So, i_{out} is linearly related to the input voltage, v_{in}, through the proportionality factor, $2k_{eq}$. The equivalent transconductance value is thus:

$$G_m = 2k_{eq} \tag{111}$$

This is in contrast to the transconductor implemented using long-channel devices in which the equivalent transconductance is dependent on the controlling voltage, v_c. Thus, short-channel CMOS composite transconductors can no longer be used as voltage-controlled resistors. Finally, refer to Fig. 21 for the differential-input single-ended output transconductor. Assuming that the four transistors, M_1–M_4, operate in saturation and the differential pair, M_1 and M_2, are matched and the current mirror composed by M_3 and M_4 are also matched with unity current gain, then it can be shown that:

$$i_{out} = i_1 - i_2 = WC_{ox}v_{sat}(v_1 - v_2) = g_m v_{id} \tag{112}$$

where v_{id} is the differential-input voltage. This is in contrast to the long-channel case where:

$$i_{out} = \sqrt{I_{ss}}v_{id}\sqrt{1 - \frac{v_{id}^2}{4I_{ss}}} \tag{113}$$

in which i_{out} is nonlinearly related to v_{id}.

4.6 Effect on the Op-Amp Performance

Due to the reduction of the intrinsic gain of MOS devices in deep-submicron CMOS technologies, the open-loop gain of the op-amp decreases significantly [51]. Since the performance metrics of analog circuits depend on the open-loop gain of the op-amp, a bad need arises to adopt gain-boosting techniques such as flipped-voltage follower, regulated cascode, and positive feedback [52]. The price paid is either the need to adopt higher power supplies or a reduction in the allowable output voltage swing. One method is to use cascading in order to increase the overall gain; however, at the expense of more difficulty of compensation [53].

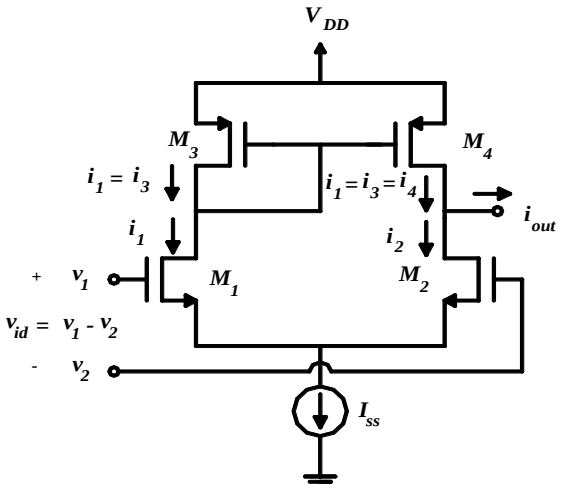

Fig. 21. The circuit schematic of the differential-input single-ended output transconductor.

4.7 Effect on the Low-Noise Amplifier Performance

Due to the hot-electron effects associated with the velocity saturation of the carriers in the channel region, the thermal noise of the channel is expected to increase with technology scaling. The down scaling of the channel length causes the channel thermal noise to decrease while the reduction in the transconductance causes it to increase [14]. These two contradicting effects seem to cancel each other and thus the channel thermal noise is expected to remain constant with CMOS scaling. On the other hand, by the effect of increasing the data throughput of the circuits and hence the frequency of operation, the flicker or $1/f$ noise is expected to decrease and can thus be safely neglected. This is typically the case for most applications except of course those associated with low data rate such as medical equipment (hearing aids, pace-makers, wearable wristwatch), self-powered devices (the contactless smart cards), the electronic watch, microsensor node, and radio-frequency identification (RFID) cards. The ratio between the channel thermal noise and the flicker noise is expected to increase with technology scaling.

5. NONLINEAR DISTORTION

In this section, the nonlinear distortion of a typical common-source amplifier (as that shown in Fig. 3) will be investigated using the short-channel model. The nonlinear distortion can be quantified by applying a single-tone sinusoidal voltage at the input of the amplifier and determining the amplitude of the second harmonic relative to that of the fundamental. In saturation,

$$i_D = WC_{ox}v_{sat}\left(v_{GS} - V_{thn}\right)\left(1+\lambda v_{DS}\right) \tag{114}$$

Suppose that a signal, $V_m \cos\omega t$, is superimposed on the dc gate-to-source voltage, V_{GS}. So,

$$i_D = WC_{ox}v_{sat}\left(V_{GS} - V_{thn} + V_m\cos\omega t\right)\left[1+\lambda\left(V_{DD} - i_D R_D\right)\right] \tag{115}$$

After substituting for V_{thn} by $V_{thn0} - \eta v_{DS} = V_{thn0} - \eta(V_{DD} - i_D R_D)$, neglecting the term containing λi_D^2 for simplifying the analysis, and performing simple mathematical manipulations, we obtain:

$$i_D = \frac{a\left[b + V_m\left(1+\lambda V_{DD}\right)\cos\omega t\right]}{c\left[1+\dfrac{\lambda R_D V_m WC_{ox}v_{sat}\cos\omega t}{c}\right]} \tag{116}$$

where a, b, and c are given by

$$a = WC_{ox}v_{sat} \tag{117}$$

$$b = \left(V_{GS} + \eta V_{DD} - V_{thn0}\right)\left(1+\lambda V_{DD}\right) \tag{118}$$

and

$$c = 1+\lambda R_D WC_{ox}v_{sat}\left(V_{GS} + \eta V_{DD} - V_{thn0}\right) + \eta R_D WC_{ox}v_{sat}\left(1+\lambda V_{DD}\right) \tag{119}$$

respectively. If V_m is assumed to be sufficiently small, then the following approximation can be used:

$$\frac{1}{1+x} \approx 1-x \quad \text{(when x << 1)} \tag{120}$$

So,

$$i_D \approx \frac{a}{c}\left[b + V_m(1+\lambda V_{DD})\cos\omega t\right]\left[1 - \frac{\lambda R_D V_m W C_{ox} v_{sat}\cos\omega t}{c}\right] \tag{121}$$

Since

$$\cos^2\omega t = \frac{1}{2}\left[1+\cos 2\omega t\right] \tag{122}$$

then, the amplitudes of the first and the second harmonics, A_{F1} and A_{F2}, are:

$$A_{F1} = \frac{a}{c}\left|V_m(1+\lambda V_{DD}) - \frac{b\lambda R_D V_m W C_{ox} v_{sat}}{c}\right| \tag{123}$$

and

$$A_{F2} = \frac{a\lambda R_D V_m^2 W C_{ox} v_{sat}(1+\lambda V_{DD})}{2c^2} \tag{124}$$

respectively. Obviously, the larger the magnitude of V_m, the larger the magnitude of the harmonics that appear in Eq. (121).

The total-harmonic distortion (THD), defined as the rms value of the harmonic components of the output signal, excluding the fundamental, expressed as a percentage of the rms value of the fundamental, can be found as

$$THD = \frac{a\lambda R_D V_m W C_{ox} v_{sat}(1+\lambda V_{DD})}{2\left|ac(1+\lambda V_{DD}) - ab\lambda R_D W C_{ox} v_{sat}\right|} x100\% \tag{125}$$

It is evident that the nonlinear distortion in short-channel devices is merely due to the channel-length modulation effect. The term including λ in the drain-current equation results in the appearance of the second-order harmonic.

This is in contrast to the long-channel devices in which the nonlinear distortion is due to both the channel-length modulation and the inherent square-law dependence. So, it can be said that nonlinear distortion is less perceptible in deep-submicron technologies. From Eq. (125), it is apparent that in order to reduce the second-order harmonic distortion, the gate-overdrive voltage of the amplifying device should be increased.

This makes a physical sense as increasing ($V_{GS} - V_{thn}$) overwhelms the effect of the factor ($1 + \lambda v_{DS}$) which is the cause of the nonlinear distortion. Also, the channel length can be increased in order to reduce λ [37], thus enhancing the linearity at the expense of the area.

6. CONCLUSIONS

In this paper, a quantitative analysis of the building blocks of the MOS analog integrated circuits using a short-channel MOS model was performed and the main differences between this analysis and the analysis using the long-channel model were illustrated. These differences can be stated as follows:

- The drain current in saturation is no longer dependent on the channel length, L, but on the channel width, W.
- The sensitivity of the transconductance, g_m, to channel width, W, in short-channel devices is larger than that in long-channel devices in which g_m is proportional to $\sqrt{W}$ for a constant drain current.
- Many computational circuits that use MOS transistors cannot be fabricated with short-channel lengths. This poses a lower limit on the area of these circuits.
- The voltage headroom required by each stacked device decreases with technology scaling.

- There is no restriction on the value of the gate-to-source signal voltage in order to ensure linearity. This is in contrast to the long-channel case in which the ac gate-to-source voltage is restricted to be much smaller than twice the gate-overdrive voltage.
- The output resistance of the short-channel MOS transistor decreases with scaling due to the decrease in the Early voltage and the appearance of the DIBL effect. This reflects the degraded performance in current sources implemented using saturation-region operated MOSFET devices.
- The use of the MOSFET transistor as an amplifier in the triode region is not preferred due to its nonlinearity. This seems to be the only similarity with the long-channel devices.
- The MOSFET device can be used as a voltage-controlled resistance in the deep-triode region with a weaker control for the V_{GS} knob due to the mobility-degradation effect.
- The amplifier is expected to be more linear, a desirable effect. So, there is no need to add a degeneration-source resistance in order to linearize the circuit with its associated reduction in gain. This seems to be an advantage for short-channel devices.
- The body effect decreases the input resistance of the common-gate stage making it more suitable for use as a current buffer.
- The use of the source-follower as *a voltage buffer* is degraded due to reducing its gain.
- The intrinsic gain decreases with technology scaling, thus the enhancement in the output resistance by cascoding decreases.
- The input-output relationship of the differential amplifier is perfectly linear (if the channel-length modulation effect is neglected).
- The need increases to use gain-boosting techniques in accordance with op-amps.
- The voltage gain of the cascode-differential amplifier is expected to be directly proportional to the square of the channel length in contrast to the long-channel devices in which the gain does not change with the channel length.
- It is expected that the CMRR of the differential amplifier degrades with scaling down the channel length. Thus, the immunity of the differential amplifier to the mismatch effects is expected to degrade.
- The ratio between the channel thermal noise and the flicker noise is expected to increase with technology scaling.
- Short-channel CMOS composite transconductors can no longer be used as voltage-controlled resistors.
- The nonlinear distortion in short-channel devices is merely due to the channel-length modulation effect in contrast to the long-channel case in which the nonlinear distortion arises due to both the channel-length modulation effect and the square-law dependence. In order to reduce the total-harmonic distortion, the gate-overdrive voltage and/or the channel length of the amplifying device should be increased.

7. FUTURE WORK

The work presented in this paper can be extended by adopting one of the following points:

- The subthreshold region seems to be promising due to its ultra-low power consumption. Also, the near-threshold region seems promising due to the saving of an appreciable

power consumption in this regime at the cost of an insignificant degradation in performance [54 - 58]. In fact, there is an increasing number of applications that require operation in these regions such as the biomedical applications [59 - 62]. So, the author suggests investigating the performance of the basic building blocks in the subthreshold and near-threshold regions in accordance with deep-submicron CMOS technologies.

- The gate-tunneling current can be neglected safely with older CMOS technologies. However, due to the adoption of ultra-thin oxides with deep-submicron technologies, its importance increases. So, investigating the effect of the gate-tunneling current on the performance of analog CMOS circuits seems to be a good point for future work. The reader can refer to [63, 64] as an initial guide with this point.
- The g_m/I_D design methodology is an important design method [65 - 67]. Since this method depends on the adopted model, the g_m/I_D design methodology needs to be investigated in accordance with deep-submicron regimes.
- New devices such as FinFET are becoming more versatile in order to overcome the short-channel effects associated with planar technology [68, 69]. The reader is encouraged to investigate the performance of the main analog building blocks using FinFETs.
- As the technology advances, the operation goes towards higher frequencies of operation [70]. Thus, developing appropriate models that are suitable for RF operation seems to be a good topic for research.

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