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An Optimized Temperature Compensated Ring Oscillator with Low Power Consumption and Low Variation

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***Abstract*—** In this paper a low power ring oscillator with three differential delay stages and one output buffer stage is designed for Radio Frequency Identification (RFID) applications. The proposed oscillator is designed with neural network model and its parameters are optimized with Teaching–Learning Based Optimization (TLBO) algorithm. The central frequency of the oscillator becomes independent of the temperature with the help of two temperature compensation techniques. In the first technique, the PMOS load transistor of each stage is connected to the NMOS diode connected - in series - transistor. Since these two transistors work in complement of each other, the temperature variation of each stage's output voltage is decreased. In the second technique, the current variation of oscillator stages versus temperature is reduced since the diode connected transistor is employed in the current source structure. The simulation is done in 0.18 µm Complementary Metal-Oxide Semiconductor (CMOS) technology with the help of Cadence software and the chip area of the layout designed with this software is 19×25 µm². The designed oscillator exhibits the following parameters: a central frequency of 7.5 MHz, the power dissipation is 238 nW and the frequency deviation is 210 ppm/°C in the temperature range of 0 to 120°C, the noise phase and the period jitter are -87.05 dBc/Hz and 0.578 ns (rms), respectively, at 100 KHz offset frequency and 10000 clock cycle.

***Keywords*—** Low power consumption; Ring oscillator; Temperature coefficient; Teaching–Learning Based Optimization.

1. INTRODUCTION

Radio Frequency Identification (RFID) is the automatic detection system that uses radio frequency for detecting persons and objects. It usually includes one reader and one tag. The RFID tag is categorized into three groups such as active, semi passive and passive. The passive tags don't have on-chip battery and they are supplied by waves sent from the reader. Based on Friis equation the blocks of the tag should have the minimum power dissipation to increase the reading range [1-5]. In general, the RFID passive tag includes four main blocks such as power management unit, processor, sensor, and analog front end. According to Fig. 1, an oscillator has been used to adjust the sensor and the processor block. Since there is no battery in the passive tag, all used blocks such as oscillators must be low powered to increase the reading range.

Most of the data transmission between the tag and the reader is done based on Electronic Product Code Class 1 Generation 2 (EPC C1 G2) protocol and due to this protocol, the frequency deviation should be lower than 4% [6]. The oscillators in tags are commonly used in three structures: Phase Locked Loop (PLL), RC relaxation and ring oscillator. The PLL oscillator has a low frequency deviation, but it consumes more power [7]. The RC relaxation oscillator unlike the PLL oscillator have higher frequency deviation and lower power dissipation, so they are

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seldom used in the RFID tags [8-10]. The single output ring oscillator [11, 12] and differential ring oscillator [13,14] are more common for the RFID tag design because the capacitance is not used in these circuits and consequently the power dissipation and the frequency deviation have the lowest value.

In [11], to reduce power consumption, PMOS and NMOS transistors are used for each stage, so the swing voltage of the ring oscillator stages is reduced. The oscillator presented in [12] is a single output oscillator that has low power loss and high frequency deviation. Also, the presented oscillator in [6] is the differential ring oscillator that uses the temperature compensator for decreasing the frequency deviation while its power consumption is considerable.

To improve the frequency stability and spectrum purity of the oscillator, the noise phase and jitter parameters should be minimized. By using the high-quality LC tank, the phase noise and jitter can be minimized but the low chip area of the RFID tag makes the limitation of using this technique [15, 16].

In this paper the ring oscillator with three differential delay stages and one output buffer stage is designed with the aim of low power dissipation and frequency deviation related to the temperature. To decrease the output frequency deviation versus the temperature, the temperature variation of output swing voltage and the temperature variation of biasing current of differential stages should be minimized. W and L of the proposed oscillator transistors are optimized with Teaching–Learning Based Optimization (TLBO) algorithm for increasing the frequency and having lower power dissipation and lower frequency deviation.

In section 2, the structure of the proposed oscillator is studied. The neural network and optimization with TLBO algorithm are considered in section 3 and section 4 presents the simulation results.

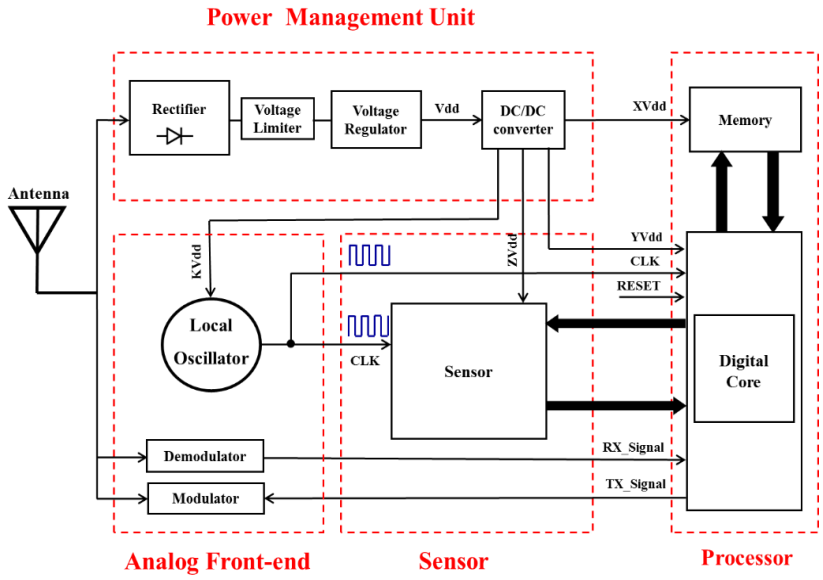

Fig. 1. Block diagram of the passive tag.

2. THE DESIGNED OSCILLATOR

Fig. 2 shows the proposed oscillator. In each stage the differential delay cell with the active load are used. The differential delay stages reduce the common mode noise and provide 50% duty cycle for the output waveform. Since the dependency of the threshold voltage and the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

transistors transconductance is very high related to the temperature the differential delay stages of the oscillator have low thermal stability. By using the resistor or the compensator operational amplifier the desired thermal stability is created. As the temperature coefficient of the resistors is high and the circuit with the employed operational amplifier is very complicated they are hardly ever used.

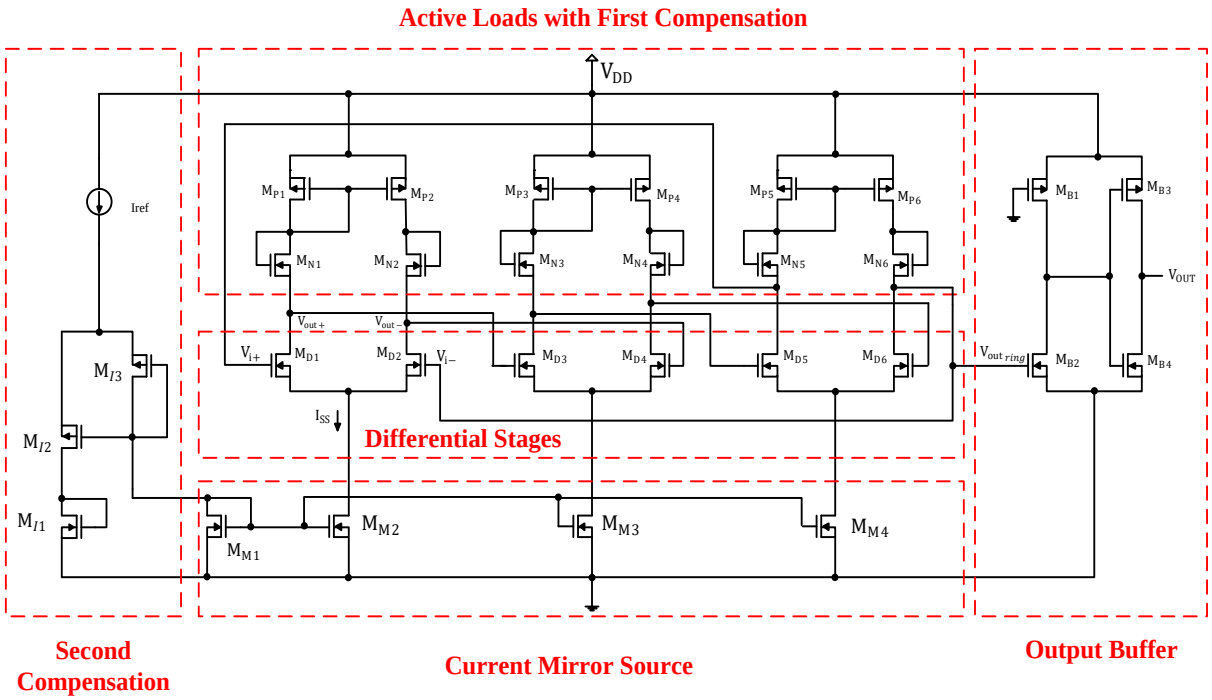

Fig. 2. The proposed oscillator circuit.

In this article, two techniques of controlling the temperature changes of the load and controlling the temperature changes of the current source are used to ensure the thermal stability of the output frequency. For making independent of the output voltage of the oscillator delay stages related to the temperature two transistors such as MN and MP are employed in series for each stage like Fig. 3 [17, 18]. Based on Fig. 3 MN1 and MP1 are biased in the sub-threshold region. In this case due to VdsP1 and VdsN1 $\geqslant$ 4VT , the shown currents are calculated as Eq. (1) and Eq. (2).

$$I_{subP} = K_P \left(\frac{W}{L}\right)_P {V_T}^2 exp\left(\frac{V_{gsP}-V_{thP}}{nV_T}\right) \quad (1)$$

$$I_{subN} = K_N \left(\frac{W}{L}\right)_N {V_T}^2 exp\left(\frac{V_{gsN}-V_{thN}}{nV_T}\right) \quad (2)$$

where k = μC_{ox}, (μ is the mobility, C_{ox} is the gate-oxide capacitor per unit area), n is the slope of sub- threshold, V_{gsN} is the gate-source voltage of the NMOS transistor, V_{gsP} is the gate-source voltage of PMOS transistor, V_T is the thermal voltage, V_{thN} and V_{thP} are the threshold voltages of the NMOS and PMOS transistors, respectively.

Given the fact that $I_{subN} = I_{subP}$, the voltages of active load terminals are achieved as Eq. (3) and Eq. (4).

$$V_{load} = -V_{gsP} + V_{gsN} \quad (3)$$

$$V_{load} = -\left(nV_T \, ln\frac{\beta_N}{\beta_P} + V_{gsN} + V_{thP} - V_{thN}\right) + V_{gsN} \quad (4)$$

where $\beta_N = K_N(W/L)_N$ and $\beta_P = K_P(W/L)_P$. The output node voltage of each stage, V_{out-} , is calculated as Eq. (5) and its temperature dependency is based on Eq. (6).

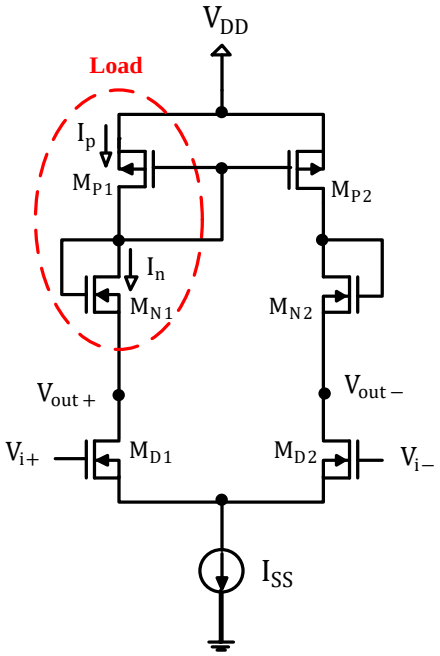

Fig. 3. One differential delay stage with load temperature compensation.

$$V_{load} = -\left(nV_T\, ln\frac{\beta_N}{\beta_P} + V_{gsN} + V_{thP} - V_{thN}\right) + V_{gsN} \tag{5}$$

$$\frac{\partial V_{out-}}{\partial T} = \frac{\partial V_{thP}}{\partial T} - \frac{\partial V_{thN}}{\partial T} + n\, ln\left(\frac{K_P\left(\frac{W}{L}\right)_P}{K_N\left(\frac{W}{L}\right)_N}\right) \times \frac{k_B}{q} \tag{6}$$

where k_B is the Boltzmann constant and q is the charge of electron. K_P and K_N parameters are proportional to $T^{-3/2}$ that in this case are eliminated. Given the fact that the threshold voltage has a reverse relationship with the temperature the output voltage can be independent of the temperature by setting the size of transistors M_N and M_P.

Based on Fig. 2 by using M_{I1}-M_{I3} transistors the current of oscillator delay stages becomes independent of temperature. Since the biasing current of oscillator stages has a considerable dependency on V_{th} by the temperature variation of V_{th} the current of these stages is changed which leads to oscillator frequency changes. To solve this problem the temperature coefficient of V_{th} can be compensated by adding M_{I1}-M_{I3} transistors. If the threshold voltage is reduced by the increasing of the temperature the current, which passes M_{I2}, is increased. In this situation due to (7) and (8) by reducing the current of M_{I3} the current passing through M_{M1}, M_{M2}, M_{M3} and M_{M4} is reduced because I_{ref} is fixed. Therefore, this current reduction compensates for the current increment resulting from V_{th} reduction and the current is almost fixed [1].

$$I_{ref} = I_{I2} + I_{I3} \tag{7}$$

where I_{I2} and I_{I3} are the currents passing through M_{I2} and M_{I3}, respectively. If the seen resistance from drain and source of M_{I3} is supposed to be almost constant to V_{gs} variations, I_{M2} is calculated as follows:

$$I_{M2} = \frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M1}} \times \frac{V_{gs_{I3}}}{R_{I3}} \tag{8}$$

where $(W/L)_{M2}$ and $(W/L)_{M1}$ are the sizes of M_{M2} and M_{M1}, respectively, and R_{I3} calculated based on Eq. (9) is the resistor of M_{I3} which works in subthreshold region.

$$R_{I3}=\frac{\partial V_{ds_{I3}}}{\partial I_{I3}}=\frac{\partial V_{gs_{I3}}}{\partial I_{I3}}=\left[\frac{1}{\eta V_T}\left((\eta-1)\mu_p C_{ox}\left(\frac{W}{L}\right)_{I3}\right.\right.$$
$$\left.\left.\times V_T{}^2 exp\left(\frac{V_{gs_{I3}}-V_{thN}}{\eta V_T}\right)\right)\left(1-exp\left(-\frac{V_{ds_{I3}}}{V_T}\right)\right)+\frac{1}{V_T}\times\left((\eta-1)\mu_p C_{ox}\left(\frac{W}{L}\right)_{I3}V_T{}^2 exp\left(\frac{V_{gs_{I3}}-V_{thN}}{\eta V_T}\right)\right)\right.$$
$$\left.\times exp\left(-\frac{V_{ds_{I3}}}{V_T}\right)\right]^{-1}=\left[\frac{1}{\eta V_T}I_{I3}+\frac{1}{V_T}\left((\eta-1)\left(\frac{W}{L}\right)_{I3}\times\mu_p C_{ox}V_T{}^2 exp\left(\frac{V_{gs_{I3}}-V_{thN}}{\eta V_T}\right)\right)exp\left(-\frac{V_{ds_{I3}}}{V_T}\right)\right]^{-1} \quad (9)$$

By using Eq. (9) in Eq. (8), I_{M2} is achieved as Eq. (10). Since V_T and I_{I3} have a direct relationship with the temperature, the dependency of I_{M2} on the temperature is decreased based on Eq. (10).

$$I_{M2}=\frac{\left(W/L\right)_{M2}}{\left(W/L\right)_{M1}}\times V_{gs_{I3}}\left[\frac{1}{\eta V_T}I_{I3}+\frac{1}{V_T}\left((\eta-1)\left(\frac{W}{L}\right)_{I3}\times\mu_p C_{ox}V_T{}^2 exp\left(\frac{V_{gs_{I3}}-V_{thN}}{\eta V_T}\right)\right)exp\left(-\frac{V_{ds_{I3}}}{V_T}\right)\right] \quad (10)$$

The generated clock for setting up the processing units and the sensor used in RFID tag should be rail to rail and square wave. By using the designed buffer which is shown in Fig. 2 not only rail to rail and square wave clock is produced, but also the effect of these stages on operation of the oscillator is prohibited. The buffer includes two stages. The first stage is the NMOS amplifier for amplifying the clock amplitude and the second stage is the inverter for producing the clock in square form.

2.1. The Power Dissipation

The dissipated dynamic power of the differential ring oscillator with N nodes is calculated as Eq. (11)

$$W_{ring}=2NC_L V_{DD}^2 f \quad (11)$$

where f is the oscillator central frequency, V_{DD} is the supply voltage and C_L is parasitic capacitor of the inverter output. Also the dissipated dynamic power of the buffer is calculated as:

$$W_{buffer}=C_{LB}V_{DD}^2 f \quad (12)$$

where C_{LB} is the parasitic capacitor of the buffer output. Based on Fig. 4 the load capacitor, C_L, which appears in the inverter output of oscillator's first stage, is calculated as Eq. (13).

$$C_L=C_{out+}=C_{gdD1}\left(\frac{1+A_{vD1}}{A_{vD1}}\right)+C_{dbD1}+C_{gdD3}\left(1+A_{vD3}\right)+C_{gsD3}+\left(\frac{\left(C_{dbN1}+C_{gsN1}\right)\times\left(C_{gdP1}+C_{dbP1}+C_{gsP2}\right)}{\left(C_{dbN1}+C_{gsN1}\right)+\left(C_{gdP1}+C_{dbP1}+C_{gsP2}\right)}\right) \quad (13)$$

where Av_{D1} and Av_{D3} are the differential gain of first and second stages. C_L of the next inverter outputs is similarly calculated. The output frequency of the oscillator is calculated as Eq. (14).

$$f=\frac{2I_D}{NC_L V_{swing}} \quad (14)$$

where I_D is the current of an inverter stage, N is the number of stages, C_L is the load capacitor seen from the output of each inverter and V_{swing} is the output voltage swing. Due to Fig. 5 the output capacitor of the buffer is achieved as Eq. (15).

$$C_{LB}=C_{out}=2\left(C_{gdB3}+C_{gdB4}\right)+C_{dbB3}+C_{dbB4} \quad (15)$$

By adding W_{buffer} and W_{ring} , the total dynamic power can be calculated.

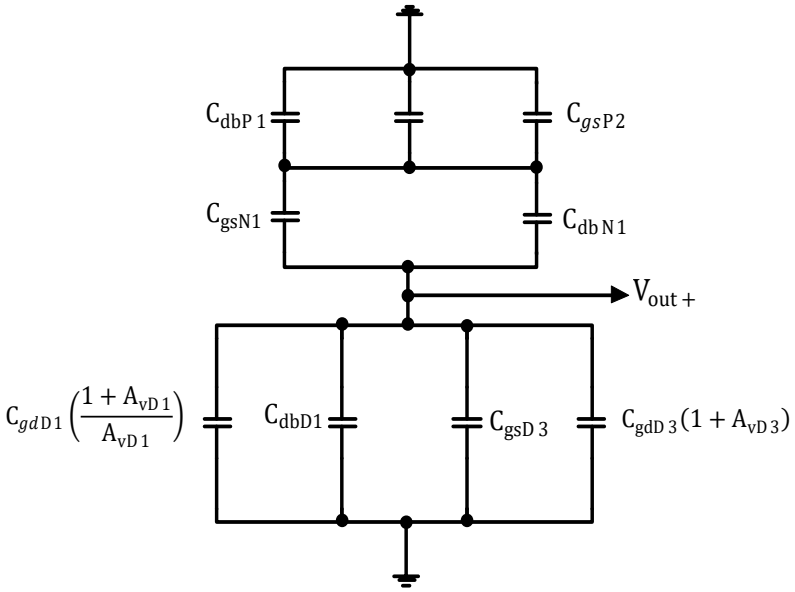

Fig. 4. Capacitor structure of the first inverter output.

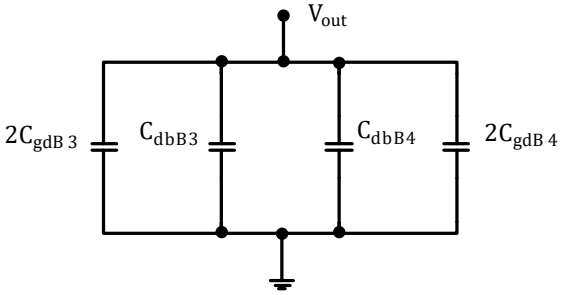

Fig. 5. Capacitor structure of buffer output.

2.2. Phase Noise

Based on Dai's theory the phase noise of the single sideband differential ring oscillator is calculated from Eq. (16) [15, 16].

$$L\{\Delta\omega\} = \begin{cases} \frac{64Fk_BTR}{9V_{pp}^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 & \left(For\ V_{pp} \ll V_{DD}\right) \\ \frac{512Fk_BTRV_{DD}}{27\pi V_{pp}^3}\left(\frac{\omega_0}{\Delta\omega}\right)^2 & \left(For\ V_{pp} \gg V_{DD}\right) \end{cases} \tag{16}$$

$$V_{pp} = \frac{2\left|dv/dt\right|_{max}}{\omega_0} \tag{17}$$

where L{Δω} is the single sideband phase noise, F is the noise factor, R is the equivalent impedance of the inverter output, $|dv/dt|_{max}$ is the maximum slew rate of the output, ω_0 is the central frequency, Δω is the central frequency offset, k_B is the Boltzmann constant, and T is the absolute temperature

3. THE NEURAL NETWORK AND TLBO ALGORITHM

For optimizing the output parameters of the oscillator with the TLBO algorithm, the nonlinear function that represents the behavior of the oscillator due to its input and output should be generated by the neural network. Then by using this function in TLBO algorithm, the

optimized inputs are gained for achieving the desired outputs. Fourteen inputs and three outputs are considered for the proposed oscillator. The inputs include W_P, L_P, W_N and L_N, the sizes of PMOS and NMOS load transistors, W_D and L_D, the size of differential pair transistors, W_M and L_M, the size of current mirror transistors, and W_{I1}, L_{I1}, W_{I2}, L_{I2}, W_{I3} and L_{I3}, the size of transistors which are used for compensating the current of current mirror. The central frequency, power dissipation and frequency deviation parameters of the oscillator are selected as the neural network outputs. The aim of the optimization is to reach the maximum frequency, minimum power dissipation and frequency deviation.

3.1. The Neural Network

The considered Perceptron neural network includes the input layer, hidden layer and output layer. To achieve the function showing the behavior of the proposed oscillator from the neural network, some inputs, and outputs proportional to the oscillator should be introduced to the network for training purposes. In order to obtain the weights of hidden layer and output layer by the achieved samples, three steps as normalizing, training and testing are done. Using the raw data to the network reduces speed and accuracy. Therefore, the input samples of the network are set between 0 and 1 during the normalization process. Logsig(X) function is used to calculate the hidden and output equation in the Perceptron neural network teaching process. If the achieved error between trained function output and simulated output with software is low, the function with the achieved weights can be used for the optimization in TLBO algorithm.

3.2. TLBO Algorithm

TLBO algorithm is one of the optimization techniques based on teaching and learning that is presented by Rao [19]. In this algorithm students are considered as the population and the lessons are the variables and inputs of cost function. The student who has the best result of objective function is considered as the teacher. The teacher tries hard to improve the knowledge of students. Besides the quality of teaching, the students can improve their knowledge by exchanging their views. The student who reaches higher knowledge than that of teacher is considered as the new teacher.

TLBO algorithm is divided into two phases. The first phase is the teacher phase that includes the student learning from the teacher and the second phase is the student phase that shows the learning of students from each other. These two phases are provided after the generation of initial population and evaluation of objective function for the member of population. In the teacher phase, the teacher tries to increase the average learning of students and makes the students' knowledge nearer to his knowledge. This phase is randomly repeated based on Eq. (18) for producing the new member.

$$X_{new,i} = X_{old,i} + r_i \left(X_{tech,i} - T_F M_i \right) \tag{18}$$

where i index is the number of lessons, $X_{old,i}$ is the old member of population, r_i is the random number between 0 and 1, $X_{tech,}$i is the best member, T_F is the teaching factor that can be 1 or 2 and M_i is the student's average grade for each lesson. If $X_{new.i}$ is better than $X_{old,i}$ it can be selected as the new member. In the student phase, the students can improve their level of knowledge by exchanging their views. Therefore, the student can communicate randomly with the other student to improve him or herself. This process can be done based on Eq. (19).

$$X_{new,i} = X_{old,i} + r_i \left(X_j - X_k \right) \tag{19}$$

where i index is the number of members, $X_{old,i}$ is the old member, r_i is the random number between 0 and 1, X_k and X_j are two students who are selected randomly based on $f(X_j) > f(X_k)$ and $j \neq k$ condition. If $X_{new.i}$ is better than $X_{old,i}$ it is accepted.

TLBO algorithm is done by using the trained function of neural network for the proposed oscillator and the maximum and minimum measured data due to Table 1 and Table 2.

In this algorithm the initial population is randomly produced between the maximum and minimum measured sample. In the teacher and student phase the cost function is calculated from Eq. (20) by using the achieved function from the neural network and the value of the cost function is compared with the previous function. If the new cost function is better than the previous one the new member is replaced with the old one, otherwise this procedure continues for better results. Since the aim of the optimization is to reach the maximum frequency and minimum power dissipation and frequency deviation, the cost function is used based on Eq. (20).

$$Cost\ Function = \frac{Frequency}{Power \times TC} \tag{20}$$

The frequency deviation of the oscillator is calculated based on Eq. (21).

$$TC = \frac{\Delta f}{f_0 \times \Delta T} = \frac{f_2 - f_1}{f_0 \times (T_2 - T_1)} \tag{21}$$

Table 1. The maximum and minimum inputs, defined in TLBO algorithm.

Input	W_P	L_P	W_N	L_N	W_D	L_D	W_M	W_M	W_{I1}	L_{I1}	W_{I2}	L_{I2}	W_{I3}	L_{I3}
Min [µm]	0.22	0.18	0.22	0.18	0.22	0.18	0.22	0.18	0.22	1	3	0.18	0.22	0.18
Max [µm]	1	1	1	1	1	1	1	2	1	3	6	1	2	2

Table 2. The maximum and minimum outputs, defined in TLBO algorithm.

Outputs	TC [ppm/◦C]	Power [µw]	Frequency [MHz]
Min	3	0.18	142
Max	14.8	1.2	1082

4. RESULTS AND DISCUSSION

The simulation of the proposed oscillator which is optimized with TLBO algorithm and the one without optimization is done with Cadence software in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 µm Complementary Metal-Oxide Semiconductor (CMOS) technology. Fig. 6 shows the error curve of function trained by the perceptron neural network. The achieved error is less than 0.03, therefore the trained function is appropriate for use in TLBO algorithm.

The average and maximum error of frequency, power dissipation and frequency deviation related to testing process of trained function are presented in Table 3. The worst achieved error is related to the frequency that is equal 0.089 and 0.43 for the average and maximum values, respectively.

In Table 4, the W and L of transistors optimized with TLBO algorithm, W and L of transistors without using optimization and W and L of transistors used in the proposed oscillator are presented.

Based on the achieved results it is obvious that W and L of transistors used in the circuit are almost the same as the ones gained from TLBO algorithm. W and L of transistors used in designed buffer circuit are presented in Table 5.

Fig. 7 shows the frequency versus temperature in the range of 0 to 120°C for the optimized proposed oscillator and the one without temperature compensation. Also, the output waveform of the optimized oscillator is shown in Fig. 8.

Table 3. The average and maximum errors of three outputs related to the testing process.

Error	Frequency [MHz]	Power [nW]	TC [ppm/◦C]
Mean_Error [%]	1.5	1.3	8.9
Max_Error [%]	6	8	43

Table 4. The achieved results from TLBO algorithm, the used values in the proposed circuit and the achieved values without using optimization.

	W_P	L_P	W_N	L_N	W_D	L_D	W_M	L_M	W_{I1}	L_{I1}	W_{I2}	L_{I2}	W_{I3}	L_{I3}
TLBO algorithm output	0.56	0.21	0.22	0.19	0.24	0.18	0.22	0.9	0.22	2.3	4.7	0.18	1	0.7
this paper	0.45	0.18	0.22	0.18	0.22	0.18	0.22	1	0.22	2.6	5	0.18	0.8	0.5
without using TLBO	0.7	0.35	0.25	0.18	0.22	0.18	0.3	2	0.5	1.5	4	0.65	0.5	1

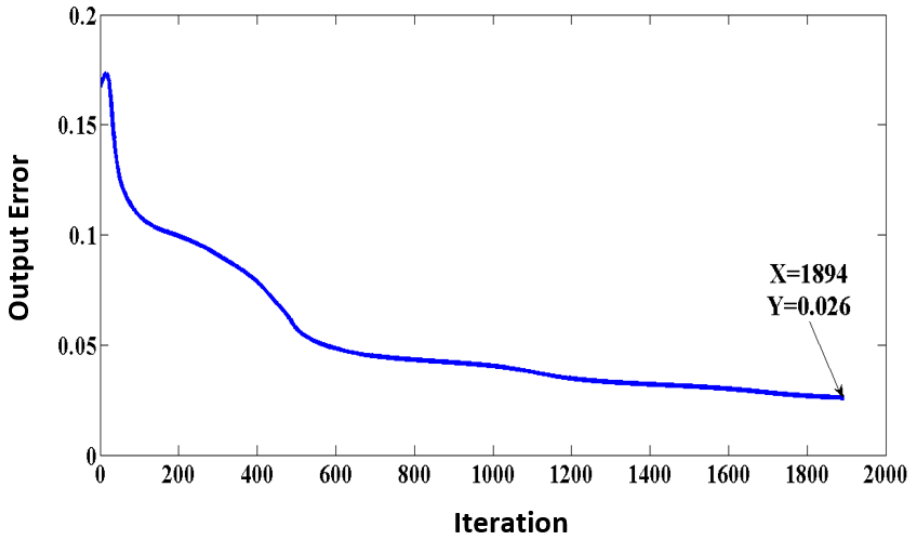

Fig. 6. The error curve achieved from neural network versus the iteration.

Table 5. W and L of output buffer transistors.

W & L	W_{B1}	L_{B1}	W_{B2}	L_{B2}	W_{B3}	L_{B3}	W_{B4}	L_{B4}
Value [µm]	0.28	1.2	0.5	1.2	0.22	0.27	0.36	0.47

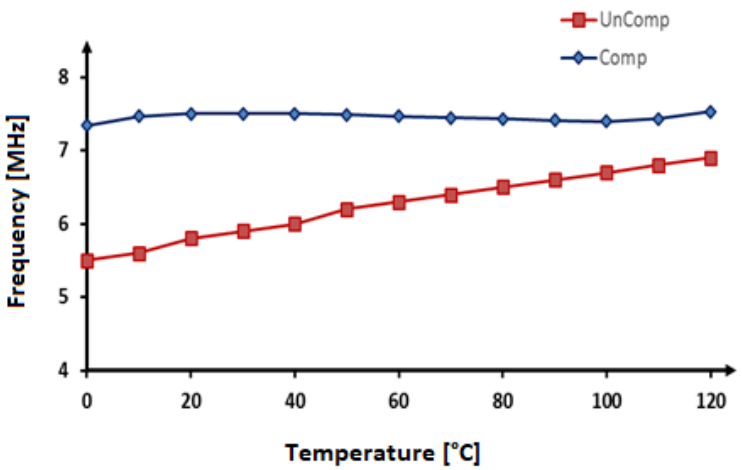

Fig. 7. The frequency curve versus the temperature of the presented oscillator and the oscillator without compensation.

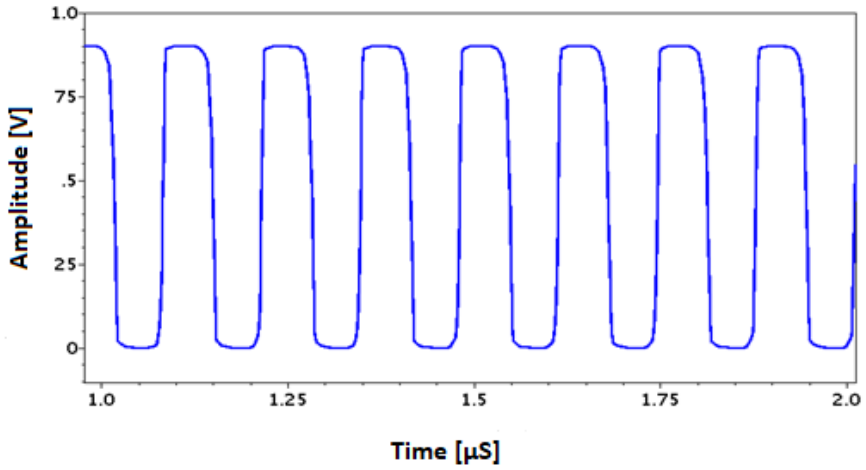

Fig. 8. Output waveform of the proposed oscillator.

Fig. 9 shows the phase noise of the optimized oscillator. The phase noise for two offset frequencies of 1 MHz and 100 KHz is simulated with Cadence software.

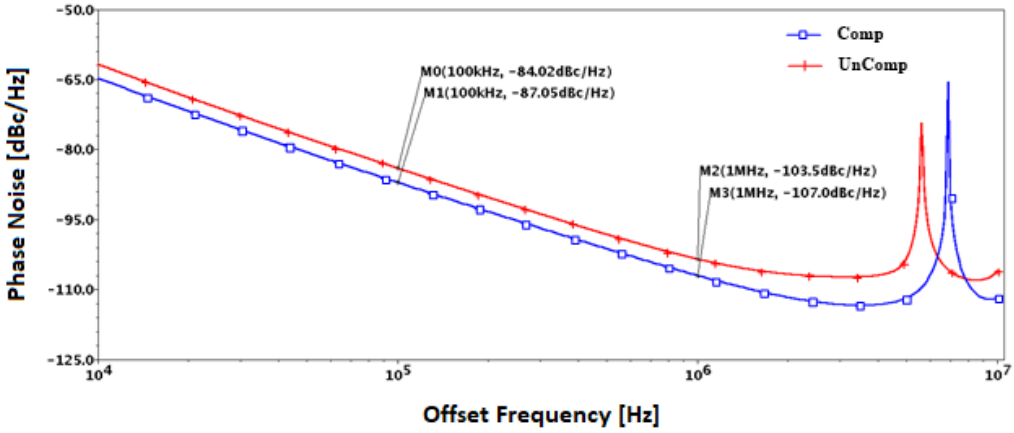

Fig. 9. The phase noise curve of the proposed oscillator.

The proposed oscillator is simulated and optimized under the condition of 0.9 V supply voltage and 150 nA reference current. The power dissipation of the optimized oscillator is 238 nW. The frequency deviation is equal to 210 ppm/°C in the temperature range of 0 to 120°C, that is suitable for RFID tag applications. Table 6 presents the simulation and calculated results

of the proposed oscillator. In addition, the rms period jitter and rms cycle to cycle jitter at 10000 clock cycle are equal to 578 ps and 1786 ps, respectively. The effect of mismatch and process variation on the output frequency of the optimized oscillator are shown in Fig. 10 for 500 runs of Monte Carlo analysis. The average output frequency and standard deviation were obtained as 7.45 MHz and 447.7 KHz, respectively. The layout of the oscillator with the temperature compensation is shown in Fig. 11. The chip area of the oscillator equals to 19×25 μm^2.

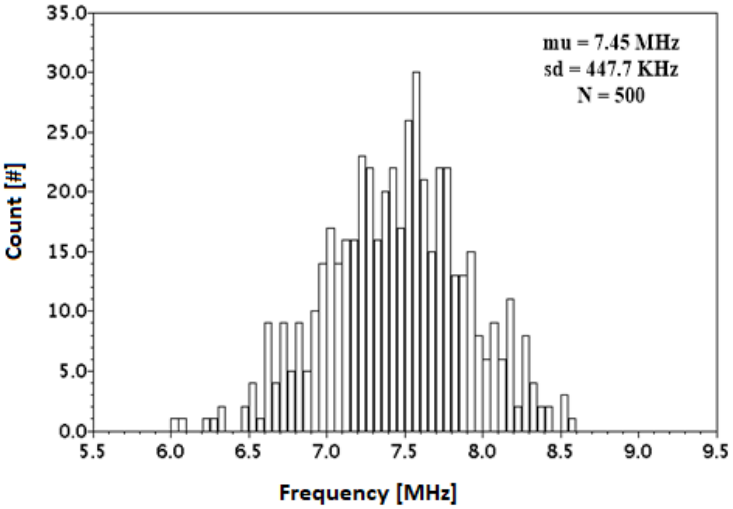

Fig. 10. The Monte Carlo analysis results of the designed oscillator.

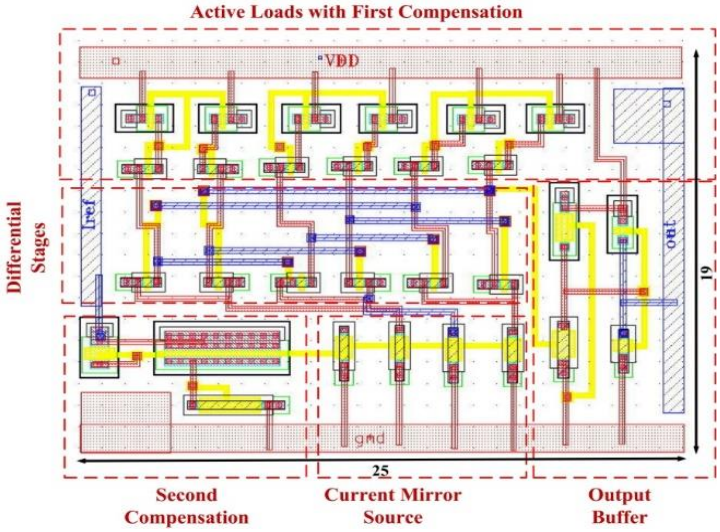

Fig. 11. Layout of the designed oscillator.

Table 6. The simulated and calculated results of the proposed oscillator.

Oscillator	Power Simu. [nw]	Phase noise (offset 1MHz) Simu. [dBc/Hz]	Phase noise (offset 1MHz) Calcu. [dBc/H]	Phase noise (offset 100KHz) Simu. [dBc/Hz]	Phase noise (offset 100KHz) Calcu. [dBc/Hz]	Jitter rms (10K cycle) [ps]	Jitter rms (cycle to cycle) [ps]	TC [ppm /◦C]	Variation [%]
With TLBO	238	-107	-115.3	-87.05	-95.6	578	1786	210 @ 0~120°C	2.52
Without TLBO	433	-103.5	-111.7	-84.02	-89.1	984	3072	521 @ 0~120°C	6.25

Table 7 presents the comparison results of the optimized oscillator with other oscillators. The proposed oscillator has the minimum chip area. Not only its power dissipation and jitter are very low, but also its temperature coefficient is very low in the temperature range of 0 to 120°C. In addition, the phase noise of the proposed oscillator at 100 KHz offset is better than the other compared works.

Table 7. Comparison between the proposed and the reported in literature oscillators.

Ref.	Tech [nm]	Type	VDD [V]	Freq [MHz]	Power [µw]	Phase noise [dBc/Hz]	Rang Temp [◦C]	TC [ppm/◦C]	Variation [%]	Area [µm²]
[1]	180	Single-ended Ring	1	8	0.725	N/A	0~50	250	1.25	551
[6]	180	Differential Ring	1	2.17	1.5	N/A	-40~80	225	2.7	N/A
[7]	180	Single-ended Ring	1	2.56	2	N/A	-15~75	356	3.2	221400
[20]	130	Single-ended Ring	0.7	3	0.24	N/A	0~100	660	6.6	N/A
[21]	90	Differential Ring	1.1	1000	790	-113.3 (10 MHz offset)	N/A	N/A	N/A	1000
[22]	180	Differential Ring	1.8	1860~ 2050	1060	-97.09 (1 MHz offset)	N/A	N/A	N/A	N/A
This work	180	Differential Ring	0.9	7.5	0.238	-87.05 (100 KHz offset)	0~120	210	2.52	475

5. CONCLUSIONS

In this paper the CMOS differential ring oscillator with power dissipation of 238 nW is designed and optimized with TLBO algorithm. By using two temperature compensation techniques, the designed oscillator achieves a temperature coefficient of 210 ppm/°C at 7.5 MHz central frequency in the temperature range of 0 to 120°C. The phase noise at a frequency offset of 100 MHz is -87.05 dBc/Hz, while the period jitter is 0.578 ns (rms) at 10000 clock cycle.

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