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Single Phase Sine-Wave Inverter with High DC Bus Utilization Using Natural Compensation

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Abstract- In this paper, a new fixed frequency single phase sine-wave inverter topology - having high DC bus utilization - is presented. The main inverter uses six IGBT switches operating at low frequency in over-modulation mode to create a five-level voltage waveform; thus, having low switching losses with high DC bus utilization. A series active power filter (SAPF) using power MOSFETs helps to remove the major harmonic voltages. No isolated DC power supply is required across the SAPF that works on a simple feed-forward compensation (instead of feedback), based on the principle of natural compensation. The DC bus voltage needed for the SAPF is about half of the inverter, thus the SAPF has low switching loss even at the designated switching frequency. The switching frequency components of the SAPF remain in the output as they are not compensated, necessitating the use of a small filter at the output to attenuate them, to create a low total harmonic distortion output voltage with higher fundamental compared to the conventional schemes using Sinusoidal Pulse Width Modulation. The proposed inverter is suitable for fixed frequency backup power supply or other applications like renewable energy connection to the power grid.

Keywords— Sine-wave inverter; Series active power filter; DC bus utilization; Natural compensation.

1. INTRODUCTION

Sine wave inverters with fixed frequency are used in several applications as backup power supply to critical equipment or synchronized to the AC grid for power support as distributed generation (DG) from renewable energy sources [1, 2]. To create the desired sinusoidal voltage wave-shape from the DC supply with voltage control, several techniques are used, of which Sinusoidal Pulse Width Modulation (SPWM) techniques are the most popular. The SPWM method is selected to reduce the magnitude of the lower-order harmonics so that the remaining higher-order harmonics can be easily filtered out using small-size low-pass LC filters [3]. However, this process results in the use of high switching frequency in the power semiconductor switches, which causes increased power loss in them. At the same time, the RMS magnitude of AC fundamental voltage obtained from the given DC supply (DC bus utilization) without using a transformer is not very high.

High DC bus utilization has been a matter of research since it yields a higher output sine-wave voltage from a given DC voltage input, which results in the need for lower input DC voltage for a particular AC voltage output. For the same DC bus input & same power output, higher DC bus utilization reduces the current through the semiconductor switches. Several inverter topologies have evolved to improve the DC bus utilization of inverters [4, 5].

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Multilevel voltage source inverters provide high DC bus utilization with low harmonics without the use of transformers or series-connected synchronized switching devices [6, 7]. In multilevel inverters, the harmonics of the output voltage are reduced by increasing the number of levels. However, this also demands large numbers of switching devices in the inverter system and several isolated DC power supplies in different multilevel structures, which is a major concern [8, 9].

Several research carried out using an auxiliary pulse width modulated (PWM) inverter in series with the main inverter in the form of the series active power filter (SAPF) has been effective in removing voltage harmonics from the output of an inverter. One such example of single-phase SAPF uses a transformer coupled PWM bridge (with a separate DC supply) in series with the main inverter to produce good quality voltage but at the cost of limited switching frequency and some higher order harmonics in the load voltage waveform [10]. Another work describes a SAPF using a transformer coupled PWM bridge, but without the use of a separate DC supply [11]. The principle, operation, and control strategy of a SAPF was described to reduce voltage harmonics for linear or non-linear load without using any transformer or DC supply but using a complex control circuit [12]. Another research work has also been presented [13] that developed a single-phase SAPF without using any transformer or DC supply. However, the use of a complex control circuit to maintain the voltage on the DC bus of the SAPF has always been a deterrent. Several techniques have been adopted to overcome the above problem, of which, the principle of natural compensation of harmonics is an interesting area [14, 15]. This technique permits the creation of lesser switching loss in the main inverter and high DC bus utilization [16].

The work presented here combines a low switching frequency multi-level inverter along with a transformer-less SAPF to yield a new combined structure for a single-phase inverter system with advantages of both, such that there is no need for a separate power supply for the SAPF. The combination permits over 20% higher DC bus utilization while maintaining similar efficiency and Total Harmonic Distortion (THD) of voltage when compared to an SPWM inverter of the same power rating, even though using a higher number of switches. In this proposal, a single-phase 5-level main inverter is operated at a low switching frequency with over-modulation to obtain low switching loss along with high DC bus utilization. A 2-level single-phase SAPF using high switching frequency is used for compensation of voltage harmonics but does not require a separate DC bus supply. The SAPF is operated in a simple feed-forward control mode (instead of complex feedback control) to maintain its own DC bus voltage based on the principle of natural compensation. Further, due to the use of a multi-level main inverter, the lower order harmonics are low, hence required DC bus voltage of the SAPF is low, permitting the use of lower voltage devices like power MOSFETs with lower losses at a given switching frequency. A small L-C filter is used at the final output to remove switching frequency components of the auxiliary inverter and create a low total harmonic distortion (THD) sinusoidal output voltage with a magnitude higher than that obtained through a standard PWM inverter.

2. THE PROPOSED SCHEME

The proposed single-phase inverter scheme is depicted in Fig. 1. It comprises of a single-phase 5-level inverter operating from its DC voltage input (V_{dc}), switching only at low frequency, with the desired fundamental frequency output voltage. The output voltage from

this inverter is a stepped waveform without any high-frequency modulation, unlike normal multi-level inverters, thereby creating a high DC bus utilized output waveform (that has a large amount of fundamental AC voltage) with low switching losses. This inverter however has a significant amount of harmonics in its output voltage and a limited range of output voltage adjustment through adjustment in its pulse widths.

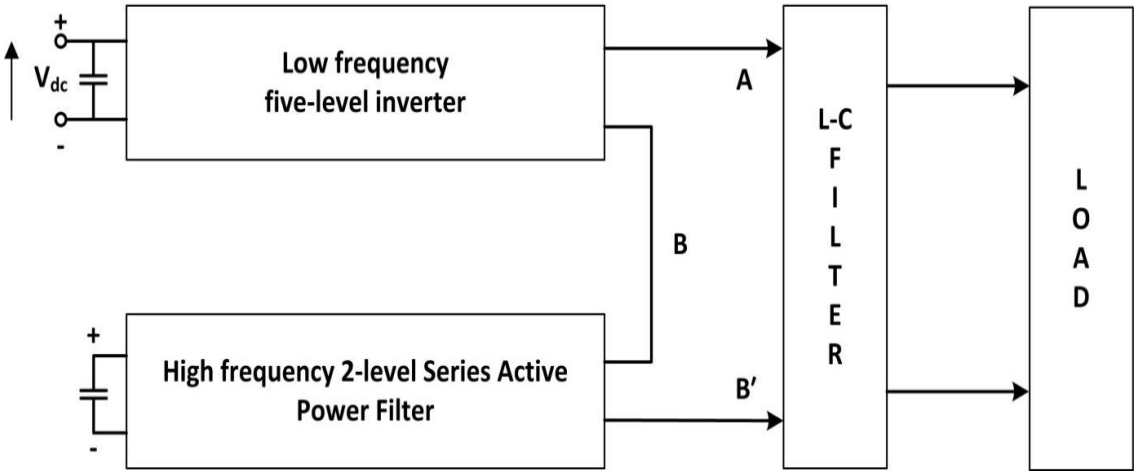

Fig. 1. Scheme of the proposed sine-wave inverter.

A separate single-phase 2-level PWM inverter with only a capacitor bank connected across its DC bus (without a separate power supply) has its output AC terminals connected in series with the 5-level inverter. This is referred to as the SAPF or the compensator. This produces a specially controlled PWM voltage waveform across its output, that has the same order and magnitude of voltage harmonics as what was created by the main inverter, except being out of phase, without any content of the main inverter fundamental voltage. This compensating voltage waveform, when connected in series with the main inverter, as depicted in Fig. 1, results in the cancellation of the harmonic voltages of the main inverter across the total output. Thus, the resultant voltage available across the output is only the fundamental content of the main inverter with added PWM switching frequency component of SAPF. Hence, a small LC filter is sufficient to provide an acceptable sinusoidal voltage waveform across the connected load.

The major contribution of this work is to initially create a stepped voltage waveform with maximum DC bus utilization, without regard to voltage harmonics as they would be removed effectively by the SAPF. For example, a single-phase square wave has a theoretical fundamental root-mean-square (RMS) AC voltage magnitude of 90% of the DC voltage, which provides the maximum possible DC bus utilization but has significant low-order voltage harmonics that would require a large filter for removal. On the other hand, a single-phase SPWM waveform has reduced lower-order harmonics, but the maximum fundamental RMS voltage is only about 70.7% of the DC bus voltage. Thus, the generation of a stepped voltage waveform with two steps in a half cycle (operating in SPWM mode with over-modulation) facilitates high DC bus utilization combined with voltage adjustments while having low switching losses. However, a high number of low-order harmonics in such a voltage waveform created by the main inverter needs large filtering. Elimination of harmonics is accomplished here through a SAPF, based on an auxiliary inverter switching at a higher frequency, but with a lower DC bus voltage, without any separate DC power source, based on a simple feed-forward principle instead of a complex feedback system.

The output voltage generated across the points A & B by switches of the main inverter can be expressed as:

$$v_{AB} = \sum_{k=1,3,5,7,...}^{\infty} V_k \sin k(\omega t - \phi_k) \quad (1)$$

where, ω is the fundamental angular frequency, ϕ_1 is assumed to be zero (as the reference) and V_k is the amplitude of the k-th order voltage harmonic component. This comprises a fundamental amplitude V_1 along with several harmonics of k-th order with magnitude V_k.

The voltage generated by the SAPF across points B & B′, can be expressed as:

$$v_{BB'} = -\sum_{k=3,5,7,..}^{\infty} V_k \sin k(\omega t - \phi_k) \quad (2)$$

Since the magnitude and phase of the harmonics developed in the SAPF is controlled to be equal to that of the main inverter, considering the series connection of the two voltages, the final output voltage across points A & B′ can be expressed as:

$$v_{AB'} = v_{AB} + v_{BB'} = V_1 \sin \omega t \quad (3)$$

Thus, only fundamental voltage will be present, with all other harmonic voltages (including lower-order harmonics) canceled without the use of any LC low-pass filter.

Following effective compensation of voltage harmonics at load terminals, the series current through the inverter and SAPF is predominantly due to the fundamental. However, as the SAPF is not generating any fundamental component of voltage across it, there will be no fundamental active power exchange with the latter. Thus, its DC bus capacitor once charged up through auxiliary paths, can maintain its voltage by natural balance through a simple feed-forward control process, without getting discharged, without the need for a separate energy supply to its DC bus. However, considering system losses, a small amount of energy is required to maintain its DC bus voltage, which is automatically executed.

The above is based on the principle of Natural Harmonic Compensation (NHC) [16] as applied here. During normal operation, if any harmonic voltage generated by the main inverter is not compensated by the same harmonic created by the SAPF, then the resulting harmonic voltage sends a corresponding harmonic current through the load circuit. This harmonic current, along with the corresponding harmonic voltage across the SAPF, transfers energy through the switches of the SAPF, charging up its DC bus capacitor until the compensating harmonic voltage is equal to that of the main inverter when energy flow due to the harmonic stops automatically. Similarly, the reverse action takes place when the harmonic voltage generated by the main inverter is overcompensated by the corresponding harmonic generated by the SAPF. Thus, the average state of charge of the DC bus capacitor of SAPF remains constant, provided that there is a minimum harmonic current path existing through the load such that energy can flow to/from the DC bus capacitor of SAPF at a rate equal to or faster than the internal loss in energy of the SAPF.

It may be noted that the naturally controlled DC bus voltage of the SAPF is automatically adjusted to create the right magnitude of compensating harmonic voltage. Since the output voltage waveform of the main inverter having steps already has a reduced magnitude of lower-order harmonics, the corresponding DC bus voltage of SAPF is lower than that of the main inverter. This aspect is used to advantage in this work by using lower blocking voltage rating devices in the SAPF and thus achieve lower switching losses.

3. THE PROPOSED INVERTER

The complete circuit diagram of the proposed single-phase inverter system is presented in Fig. 2. It consists of a neutral point clamped main inverter generating a five-level voltage output at the fundamental frequency with two steps in each half-cycle, whose width can be modulated to control the fundamental voltage. To compensate for the voltage harmonics of the main inverter, a single-phase high-frequency two-level auxiliary inverter working as a SAPF (based on natural compensation) is connected in series, creating opposing harmonic voltages. Finally, a small L-C filter is used to remove all voltage transients and switching frequency components to create a low THD voltage waveform with high DC bus utilization.

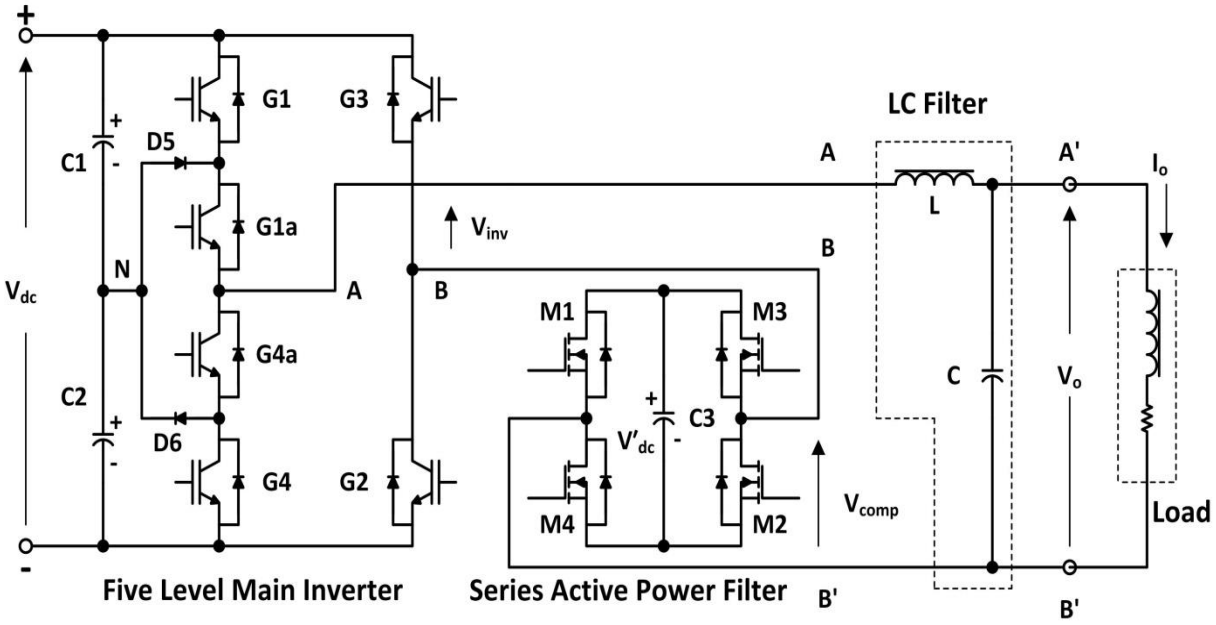

Fig. 2. Power circuit of the proposed single-phase sine-wave inverter.

3.1. Principle of Operation of the Main Inverter

The diode-clamped 5-level main single-phase inverter provides multiple voltage levels from the single DC bus divided into three levels by the series connection of two identical capacitors C1 & C2 that create a DC neutral point N. The first limb has four IGBTs (G1, G1a, G4, G4a) connected in a string across the input DC bus and has two diodes D5 & D6 connecting the string at different symmetrical points to the DC bus neutral. When the switches G1 and G1a are turned on, the output point A is connected to the positive DC bus. When the switches G4 and G4a are turned on, the output point A is connected to the negative DC bus. When the switches G1a or G4a are turned on while all other switches of the same limb are off, the output point A is connected to the mid-point of the DC bus through the diodes D5 or D6 depending on the current polarity. Thus, the first limb creates a 3-level voltage output (V_{AN}) at the desired fundamental frequency at point A concerning the DC bus neutral N, with one pulse per half cycle (without high-frequency modulation) as shown in Fig. 3. The switches G1, G1a, G4, G4a of the first limb creates voltage levels with respect to this mid-point as $\left(+0.5V_{dc}, 0, -0.5V_{dc}\right)$. It is to be noted that the minimum blocking voltage of switches G1, G1a, G4 & G4a is required to be only half that of the DC bus (V_{dc}), hence the switching losses in these devices are also lower than any device that faces full DC bus blocking voltage.

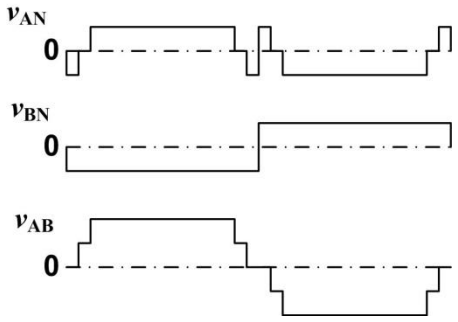

Fig. 3. Schematic of stepped wave voltage generation in proposed inverter.

The second limb has two switches G2 and G3 connected to the input DC bus without any connection to the bus mid-point. When switch G3 is turned on, the output point B is connected to the positive DC bus, and when switch G2 is turned on, the output point B is connected to the negative DC bus. The operation of these two switches produces a 2-level output as V_{BN} at the desired fundamental frequency (as square wave) without any PWM control at point B with respect to the DC bus neutral N. The second limb thus creates voltage levels with respect to the DC bus mid-point as $(+0.5V_{dc}, -0.5V_{dc})$. However, its fundamental is kept displaced from the fundamental at terminal A by 180° as depicted in Fig. 3 to create the highest fundamental voltage (V_{AB}) across the output terminals A and B after taking the difference between the two limb voltages. The minimum blocking voltage of switches G2 and G3 is required to be that of the DC bus (V_{dc}).

Thus, the total output voltage created from the main inverter has the levels $(+V_{dc}, +0.5V_{dc}, 0, -0.5V_{dc}, -V_{dc})$ as the difference between the voltages of the two limbs. Hence, the resultant waveform (V_{AB}) created across the output terminals A and B is 5-level as depicted in Fig. 3. This waveform comprises fundamental voltage as well as harmonics. The operation of the switches is controlled through a low-frequency SPWM strategy in over-modulation mode using two steps per half cycle to control switching losses as well as achieve high DC bus utilization (yield more fundamental output voltage from a given DC bus voltage) combined with a restricted degree of voltage adjustments. The range of Modulation Index m used is:

$$1.5 \leq m \leq 3 \quad (4)$$

3.2. Principle of Operation of SAPF

The series-connected active power filter or compensator uses a single-phase H-bridge comprising of four MOSFETs (M1 to M4) with an isolated DC bus capacitor C3. Assuming that the DC bus capacitor C3 is fully charged, the compensator creates a conventional two-level waveform (which is pulse width modulated at high frequency) between points B and B′. The minimum blocking voltage of switches M1, M2, M3, and M4 is required to be that of the auxiliary inverter DC bus (V'_{dc}).

In order that the SAPF creates an effective compensating waveform, the constituent devices must switch at a frequency higher than that of the main inverter. This justifies the use of MOSFETs to restrict switching loss. On the other hand, the use of MOSFETs restricts the magnitude of its own usable DC bus voltage across C3. In this case, since the output of the main inverter produces a five-level waveform, thereby reducing the height of each step, the DC voltage required across the capacitor C3 is lower than the input DC bus voltage (as explained in section 4), hence permitting easy application of MOSFETs (with lower blocking

voltages) in the compensator circuit. Since no significant real power is drawn from the SAPF, it does not require an active power source on its DC side.

3.3. Principle of Operation of Low Pass L-C Filter

A small LC filter is finally used to remove the switching frequency components of the compensator as well as voltage spikes and smooth the output voltage waveform in order to obtain a low THD voltage output.

4. CONTROL PULSE GENERATION SCHEME

The block schematic of the control pulse generator for the proposed inverter system is shown in Fig. 4. Since the main inverter has a stepped output waveform, a sine wave of variable magnitude (depending on the set value of modulation index) but frequency same as that of the inverter output is compared with a set of four level-shifted triangular waves of constant magnitude but double the frequency.

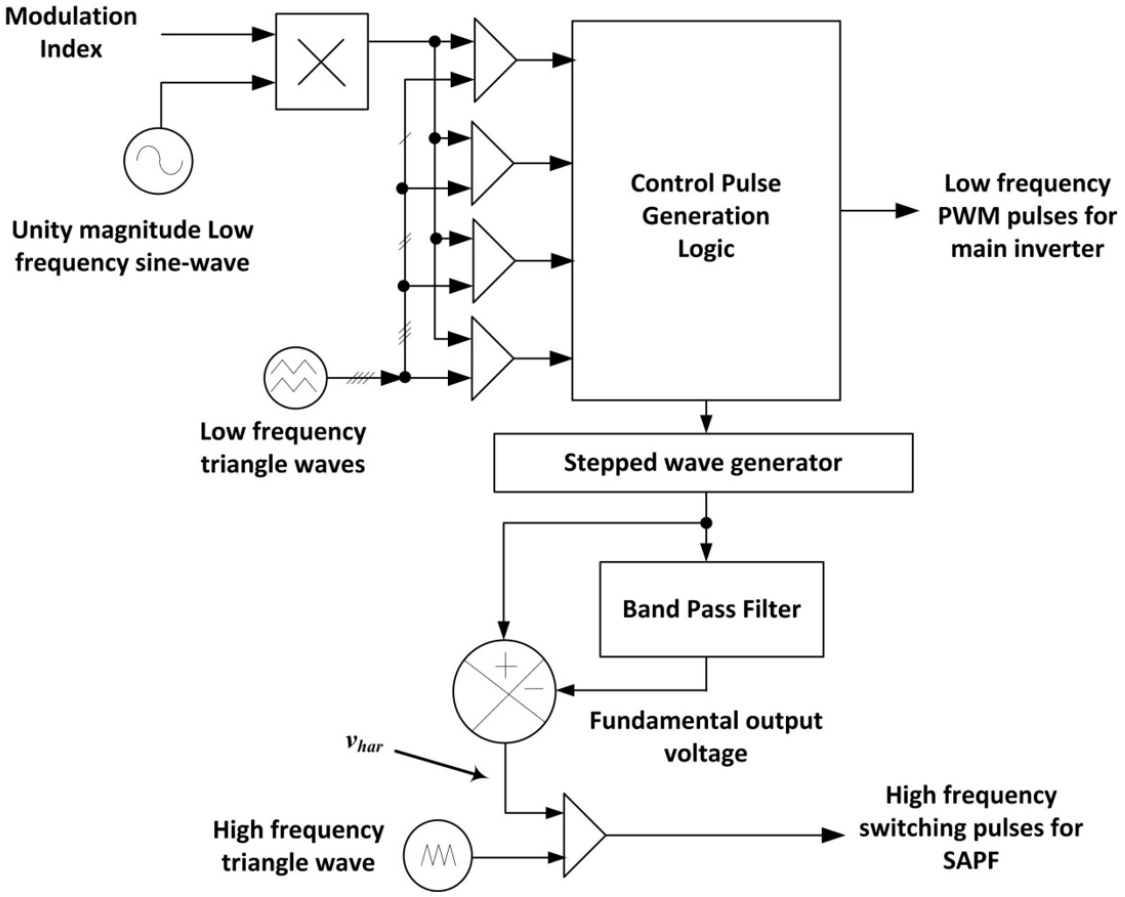

Fig. 4. Block diagram of the scheme for gate pulse generation.

The lowest step per half-cycle is created at the intersection of the sine wave v_{sine} with the triangular wave v_{t2} or v_{t3}, depending on the positive or negative half-cycle respectively concerning Fig. 5(a). The highest step per half-cycle is created at the intersection of the sine wave v_{sine} with the triangular wave v_{t1} and v_{t4} depending on the positive or negative half-cycle respectively. This results in two sets of quasi-square waveforms whose widths are controlled by the magnitude of the sine wave v_{sine}. The control pulses are derived from these using appropriate logic such that the required switching pulses for switches G1, G1a, G4a, and G4

of the main inverter of Fig. 2 are generated to produce the desired voltage between points A and N as shown in Fig. 3. The switching instants of switches G2 & G3 are created by detecting the zero crossings of the sine wave to create two square waves as shown in Fig. 3.

The control of output voltage harmonics is by a feed-forward control strategy of the SAPF. To generate the control pulses of the SAPF, first, the hypothetical 5-level output waveform is synthesized in the control circuit from the pulses generated, as shown in Fig. 5(b). The fundamental component of this waveform v_{fund} is extracted through a band-pass filter and then the same fundamental is subtracted from the synthesized 5-level output waveform to yield the hypothetical harmonic content waveform v_{har} as shown in Fig. 5(b). This resulting waveform is to be synthesized across the output of the SAPF and thus serves as the reference for the SAPF. It is to be noted that after subtraction of the fundamental, the peak-to-peak magnitude of this reference waveform created is about half of that of its original peak-to-peak waveform. This assures the reduced DC bus voltage requirement of the SAPF (V'_{dc}), which is needed to create only the waveform of v_{har} across its output terminals. This is one advantage of the proposed scheme in creating reduced switching losses in the overall system.

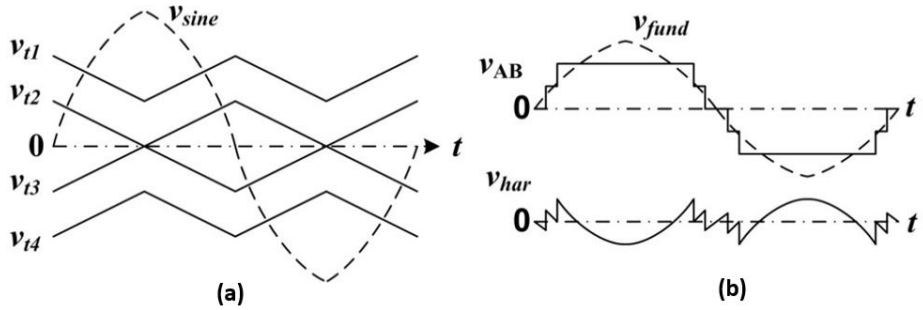

Fig. 5. Principle of: a) over-modulated SPWM pulse generation for the main inverter control; b) reference generation for SAPF (or compensator).

The reference waveform of v_{har} is compared with a separate higher frequency triangular carrier as depicted in Fig. 4 to create the PWM pulses for the SAPF (or compensator). These pulses are to be given to the switches M1, M2, M3 & M4 in sequence to generate v_{comp}, a PWM version of v_{har}, across points BB′ of the inverter in Fig. 2.

5. PERFORMANCE EVALUATION

To evaluate the performance of the proposed inverter, its parameters and components were fixed as given in Table 1.

Table 1. Values of parameters and component ratings of the investigated system.

Parameter	Value	Component	Rating
Input DC voltage (V_{dc})	128 V	IGBTs	20 A, 400V
Main inverter fundamental frequency	50 Hz	DC bus capacitors C1 & C2 (each)	2200 µF
Main inverter switching frequency	100 Hz	MOSFETs	20 A, 150V
DC bus voltage of SAPF (V'_{dc})	64 V	DC bus capacitors C3	2200 µF
SAPF switching frequency	25 kHz	Filter inductor L	350 µH
Load VA	500	Filter capacitor C	2 µF
Load power factor	0.8	Load resistance	19.4 Ω
		Load inductance	46.3 mH

5.1. Simulation Results

The 5-level inverter in series with 2-level SAPF is simulated using MATLAB software. The first limb of the low-frequency inverter is operated with a two-stepped PWM technique at m=3, whereas the second limb is operated with square pulses.

Fig. 6 presents simulated voltage waveforms at different points of the proposed sine wave inverter. Fig. 6(a) depicts the voltages of the main inverter between terminals A & N, while Fig. 6(b) shows the voltage between terminals B & N. Fig. 6(c) presents the resulting 5-level waveform across the output of the main inverter. Fig. 6(d) depicts the waveform of the inverter voltage across terminals A & B' after compensation, where the high-frequency PWM is found to be superimposed. Finally, the filtered sinusoidal output voltage across the load is seen in the waveform of Fig. 6(e). It is observed from Fig. 6(e) that the fundamental RMS value of the output voltage of the proposed inverter at no-load is about 112 volts, which is about 87.5% of the DC bus input, depicting the high DC bus utilization.

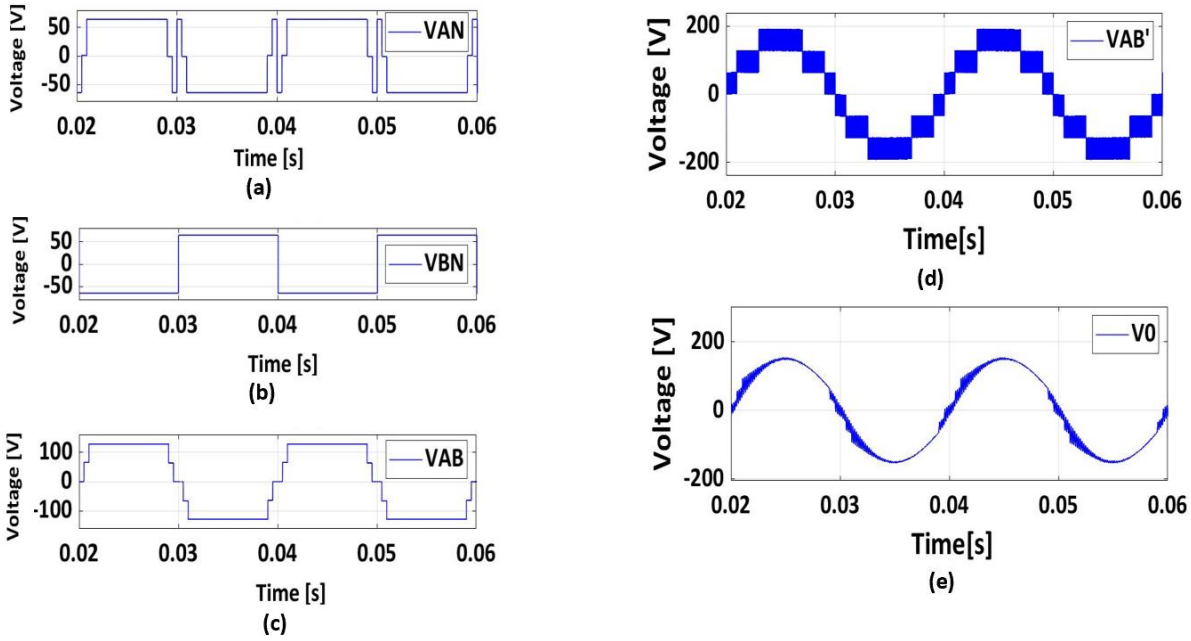

Fig. 6. Simulated waveforms: a) voltage across terminals A and N; b) voltage across terminals B and N; c) voltage across terminals A and B; d) voltage across terminals A and B'; e) output voltage across the load.

5.2. Experimental Results

For the experimental verification, a prototype was built in the laboratory with parameters as close as possible to those under simulation as in Table 1.

Fig. 7 shows the waveforms at different points of the power circuit. Fig. 7(a) depicts the voltages of the main inverter, with the green waveform being between terminals A & N, the red being between terminals B & N and the blue waveform shows the resulting 5-level waveform across the output of the main inverter. The voltage waveform across the terminals of the main inverter (V_{AB}) is found to have a THD of 28.3%. Fig. 7(b) depicts the voltage after compensation, where the blue waveform shows the superimposed high-frequency PWM onto the stepped waveform. The voltage THD across this waveform after compensation ($V_{AB'}$) is found to have a THD of 4.6%, clearly demonstrating the effective removal of voltage harmonics. The red waveform of Fig. 7(b) shows the filtered sinusoidal output voltage across the load with a THD of 4.5%.

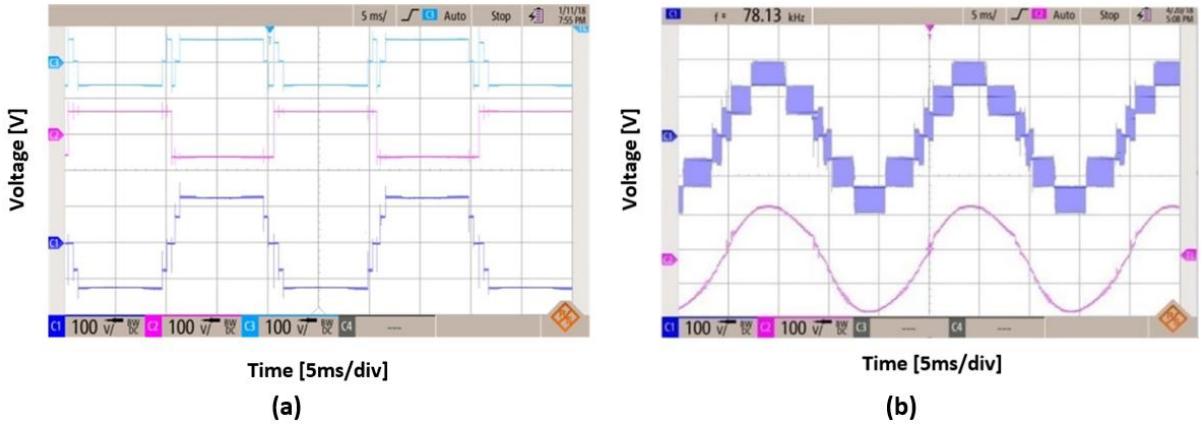

Fig. 7. Experimental waveforms: a) green curve - voltage across terminals A and N, red curve - voltage across terminals B and N, blue curve - voltage across terminals A and B; b) blue curve - voltage across terminals A and B′, red curve - output voltage across the load.

The experimental results are observed to be quite similar to the simulated ones. It is observed that the fundamental value of the output voltage is quite high compared to that of an SPWM inverter. The experimental voltage output has low THD content (4.56%) but has slightly less magnitude than the simulated value due to actual voltage drops in the inverter, compensator, and filter choke. The experimental setup in the laboratory is shown in Fig. 8.

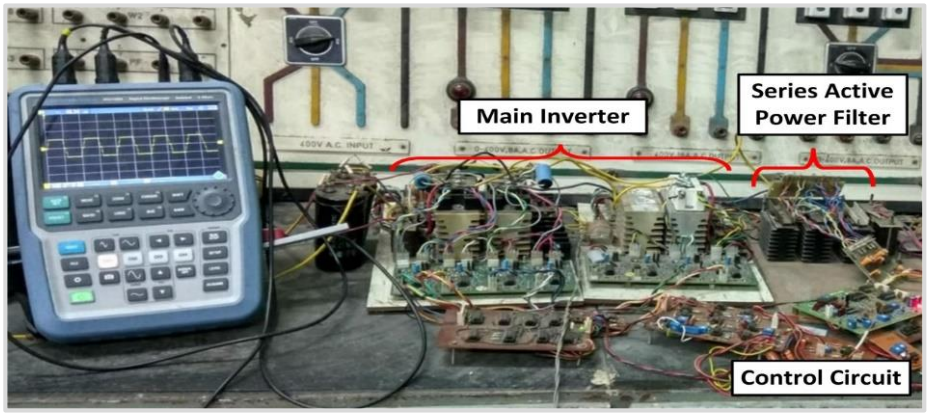

Fig. 8. The experimental setup.

5.3. Comparison of Performance

The simulated results are compared with those from experimentation in Table 2. The results will be observed to be close to each other.

Table 2. Comparison between simulation and experimental results.

Parameter	Simulation Results	Experimental Results
Input DC voltage (V_{dc})	128 V	128 V
Main inverter fundamental voltage	112 V	111 V
SAPF DC bus voltage (V'_{dc})	64 V	64.1 V
Load voltage	111 V	109.5 V
Load current	4.55 A	4.54 A
Output voltage THD	4.51 %	4.56 %

The performance of the proposed inverter is compared with that of a conventional SPWM inverter under simulation. The results are tabulated in Table 3. It will be observed that

the proposed inverter is far superior in terms of DC bus utilization, providing a 123% higher output fundamental voltage than the SPWM inverter from the same DC supply while maintaining almost the same efficiency and same output voltage THD.

Table 3. Comparison between the proposed and the conventional SPWM Inverter.

Parameter	SPWM Inverter	Proposed Inverter
Input DC voltage	128V	128V
Number of switches	4 IGBTs to support 128V	2 IGBTs to support 128V + 4 IGBTs to support 64V + 4 MOSFETs to support 64V
Switching frequency	All switches at 12kHz	2 switches at 50Hz, 4 switches at 100Hz, 4 switches at 25kHz
Output AC RMS voltage (after the filter)	90	111V
Output voltage THD (after the filter)	4.45 %	4.51 %
Load Current	4.55 A	4.55 A
Efficiency	95.1%	94.8%

Even though the proposed inverter has a higher number of switches that increases the total conduction losses, overall total losses are comparable to the SPWM inverter. This is because of all the switches in the proposed inverter scheme, several of them switch at a low frequency only, while several face only an approximate 50% blocking voltage when compared to all the switches in the SPWM inverter, thereby creating lower switching losses.

6. CONCLUSIONS

A new single-phase sine-wave inverter system with high utilization of DC bus is presented along with a SAPF controlled through feed-forward control based on natural harmonic compensation, operating from a single DC source. This inverter can generate higher fundamental voltage than traditional simple inverters due to operation in over modulation mode with voltage THD less than 5% and comparable efficiency, using a simple control strategy. The main inverter uses six IGBT switches with low switching frequency and PWM with only two steps per half cycle to reduce its switching losses. A resulting 5-level output voltage controls the lower order harmonics in output voltage along with high DC bus utilization. The SAPF uses four MOSFET switches at higher switching frequencies to create a composite harmonic voltage across its output to cancel those in the main inverter output when connected in series. Due to the use of the principle of natural compensation, the charge on the compensator capacitor can be maintained naturally using a simple feed-forward control only, without an external DC voltage supply or complex feedback control. The DC bus voltage build-up in the compensator is less than the DC voltage input, which is possible due to the stepped nature of the inverter voltage waveform. The SAPF thus has low switching loss due to its own DC voltage being only about 50% compared to the input DC. A small LC low-pass filter is used to remove components of SAPF PWM switching frequency and residual voltage waveform imperfections due to higher harmonics that are not tackled by the SAPF circuit. The complete inverter system with a higher AC voltage from a given DC voltage input is directly suitable for fixed frequency backup power supply and for other applications like renewable energy connection to the power grid.

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