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A Read-Decoupled Error-Tolerant 10T SRAM Cell in 32nm CMOS Technology

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***Abstract*—** Stability of static random access memory (SRAM) cells has become a growing concern in the nanometer regime. In order to address this issue, this paper proposes a read-decoupled 10 transistor (10T) SRAM cell. The decoupled-read feature of the proposed 10T SRAM cell protects it from the read-disturbance problem, thereby achieving enhanced read stability. Additionally, the bit interleaving capability of the cell provides immunity to soft errors. The simulation is performed on TSPICE software using a 32 nm CMOS predictive technology model. The obtained results reveal that the read static noise margin - at 400 mV - of the proposed design is 4.77x and 1.38x larger compared to that of a 6T cell and the Schmitt-trigger based 10T cell, respectively. Moreover, the write power consumption in the proposed design is found to be 1.86x lesser than that of a 6T cell. Furthermore, the proposed circuit exhibits 3.47x lesser static power consumption compared to a 6T cell.

***Keywords*—** Bit interleaving; Read static noise margin; Leakage power; SRAM; Write static noise margin; CMOS.

1. INTRODUCTION

Static random access memory (SRAM) is commonly used in today's power-aware devices such as wireless sensor nodes (WSN), mobile phones and laptops etc. Important applications of the wireless sensor nodes are in the healthcare, building automation system and in monitoring the environmental conditions [1, 2]. Since a large portion of area of a system-on-chip (SoC) is occupied by the SRAM only, therefore, an SRAM consumes a significant part of the SoC power. Hence, in order to reduce the power consumption of a SoC, it is necessary to reduce the power consumption of the SRAM. The most effective method of reducing the power consumption in SRAM is to scale-down the supply voltage. However, voltage scaling along with technology scaling results in degradation in cell stability [3, 4]. Besides stability degradation, standby power becomes a significant part of total power dissipation in sub-micron regime [5-7]. Fig. 1(a) shows the schematic of a conventional six transistor (conv6T) SRAM cell. It offers a simple circuit, but this cell suffers from stability degradation during read. As shown in Fig. 1(a), during the read operation, an intermediate voltage (ΔV) is developed at '0' storing node QB causing weakly conduction of transistor M2 and the voltage at node Q starts to fall towards ground. Consequently, transistor M3 goes in the ON state which causes a further rise in the voltage at node QB. The process becomes

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cumulative leading to bit alteration in the 6T cell. The above problem (known as read disturbance problem) can be prevented if the driver transistor M4 (and M2) is stronger than the access transistor M6 (and M5). On the other hand, an access transistor M5 (and M6) must be stronger than the pull-up transistor M3 (and M1) for a correct write operation. Thus, a balance on access-transistor size is required in the conv6T cell [8, 9].

Moreover, the conv6T cell does not support the bit-interleaving architecture. A bit-interleaved-architecture with error correcting code is an effective technique of tolerating the soft errors. In a 6T cell based bit-interleaved array, when a cell is selected (for reading or writing) by setting its wordline (WL) to high, the access transistors of other cells connected to the same row also begin to conduct. These unintentionally selected cells (whose row is selected but column is not selected), referred to as Row-half-selected (RHS) cells, experience a pseudo read operation causing the RHS cells may lose stored data; if not tackled properly [10, 11]. Thus, a 6T cell based SRAM is not capable of tolerating the soft-errors.

Researchers have proposed several cell structures to address the issues of the 6T cell. In [12], decoupled read buffer causes an 8T cell prevents read disturb, but this cell also suffers from half-select disturbance because of its 6T-like write operation. A Schmitt-trigger based 10T (ST based 10T) SRAM cell as shown in Fig. 1(b) achieves enhanced read stability but this cell dissipates more leakage power due to the absence of any leakage power reduction scheme [13]. SRAM cells presented in [14] support bit interleaving structure and offer improved write ability by weakening its pull-up network, but this cell requires an additional circuit due to data aware writing. A 12T SRAM cell proposed in [15] also achieves enhanced write margin by employing a data-dependent supply cut-off scheme, but this study does not explain the cell immunity to soft errors. A PMOS-PMOS-NMOS (PPN) based 10T SRAM cell as shown in Fig. 1(c) offers the read stability almost equal to the hold stability [16]. A PMOS-NMOS-NMOS (PNN) based differential 10T cell as shown in Fig. 1(d) offers low standby power [17]. However, this cell employs a stack of two NMOS transistors in its write path resulting in high resistive write path. SRAM cells proposed in [18, 19] provide enhanced read stability, but these cells occupy larger chip-area as they use 12 transistors for their operation. A 9T SRAM cell in [20] provides enhanced read stability, but this cell also needs a data depended write scheme. SRAM cell in [21] employs a tri-state inverter in its latch to improve writeability. However, this work does not address the soft errors issue.

In order to address the issues of the cells mentioned above, we have proposed a 10T SRAM cell which offers enhanced read stability and also supports bit interleaving architecture to tolerate soft errors. Also, the proposed cell employs just one bitline for reading the contents, which reduces switching activities in the proposed cell by approximately half when compared to the differential-read cells. The salient features of the proposed 10T SRAM cell are as follows:

a) No read-disturbance problem due to use of an isolated read buffer in the cell.
b) Low dynamic power consumption during read operation.
c) Ability to tolerate the soft-errors.

The remaining part of the presentation is organized as follows. Section 2 provides the cell-schematic and its operating modes. Section 3 provides results and discussion, and the conclusion is drawn in section 4.

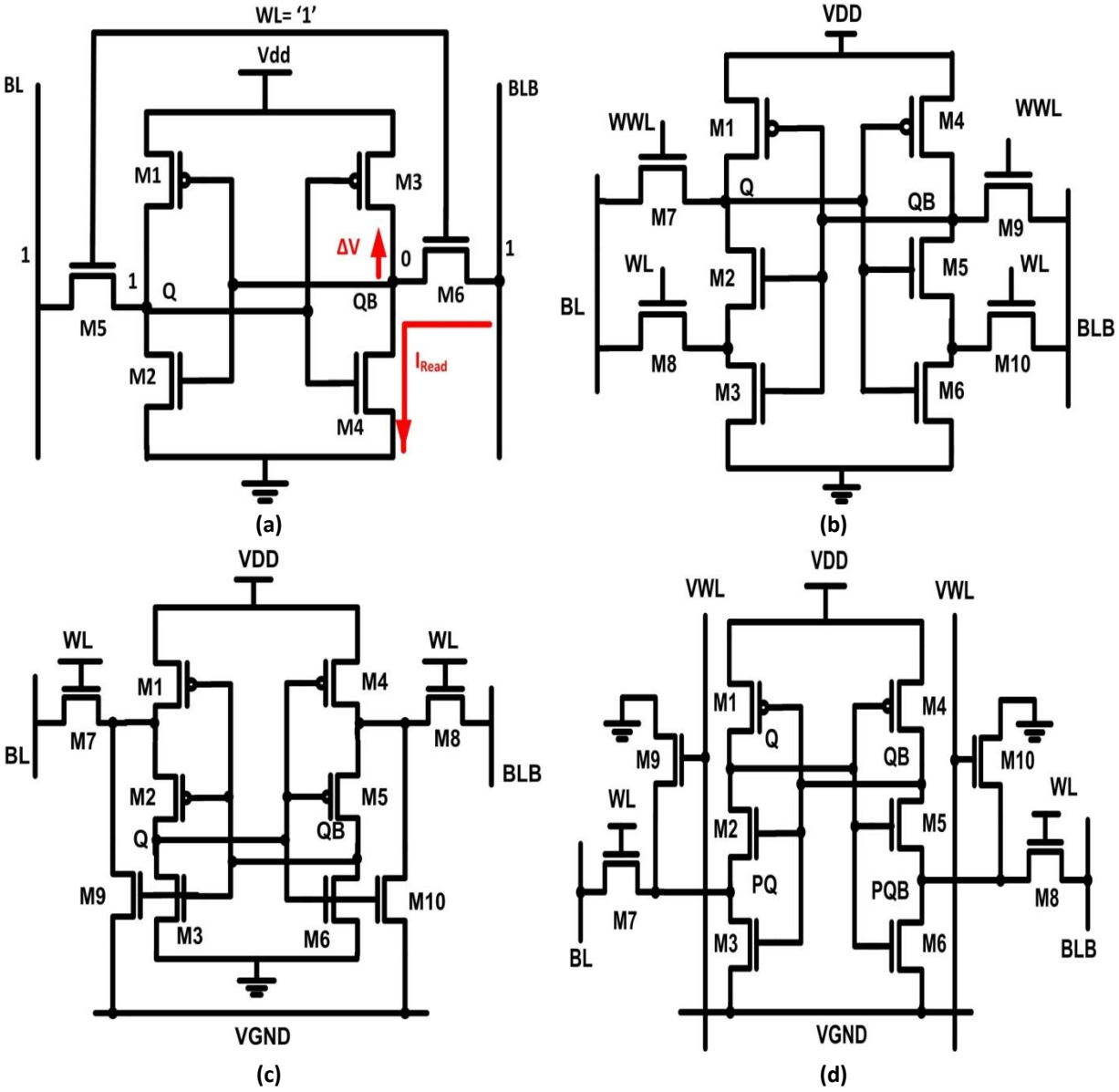


Fig. 1. Schematic of: a) conv6T; b) ST based 10T; c) PPN10T; d) PNN10T cells.

2. THE PROPOSED 10T CELL

Fig. 2 illustrates the schematic of the proposed design. In the circuit, left inverter (M1 to M4) and right inverter (M5 to M6) are connected back to back to form a latch. Transistors M7 and M9 are write access transistors to transfer data between bitline BL (bitline bar BLB) and storage node Q (QB). The read buffer (formed by M9 and M10) is used to access the cell data when the wordline WL (row based) is high and control signal VVSS (row based) is low. Control signals write-wordline WWL (row based) and column-select CS (column based) are the input of transistor M8. Here, M8 performs AND logic operation and activates local wordline LWWL when WWL and CS are both high. To maintain symmetry, the strength ratio of pull-down to pull-up networks of left inverter is the same as that of the right inverter. Table 1 illustrates the control signal status of our cell.

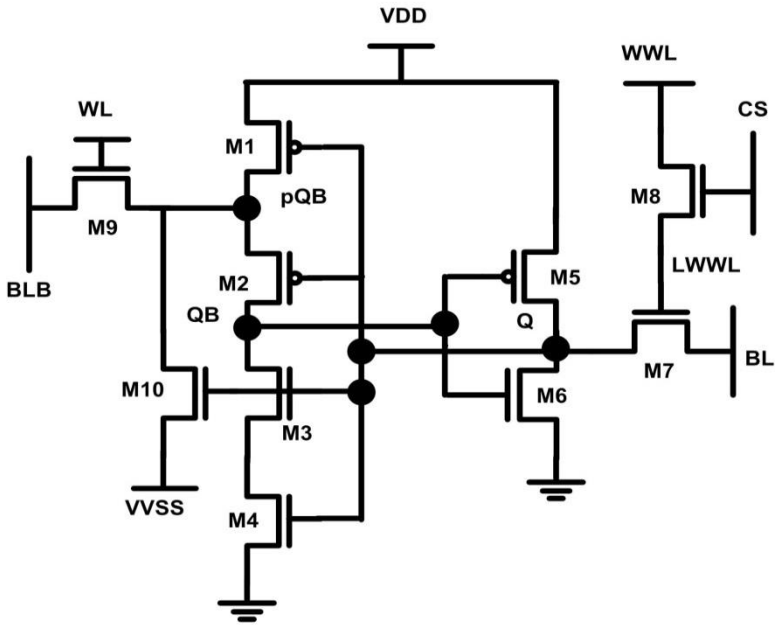


Fig. 2. The proposed 10T SRAM cell.

Table 1. Control signal status of the proposed 10T cell.

Mode of operation	WWL	CS	WL	VVSS	BL	BLB
Read	'0'	'1'	'1'	'0'	'1'	'1'
Write 0	'1'	'1'	'1'	Float	'0'	'1'
Write 1	'1'	'1'	'1'	Float	'1'	'0'
Hold	'0'	'0'	'0'	'1'	'1'	'1'

The read operation, as shown in Fig. 3, is initiated by precharging the bitline BLB to VDD. To begin, WL is raised to VDD while virtual ground (VVSS) is pulled low. Transistor M7 remains OFF by forcing WWL to ground. Consequently, BLB is discharged through M9-M10 (if the cell stores a '1'). Alternatively, BLB is maintained at VDD (if Q = '0').

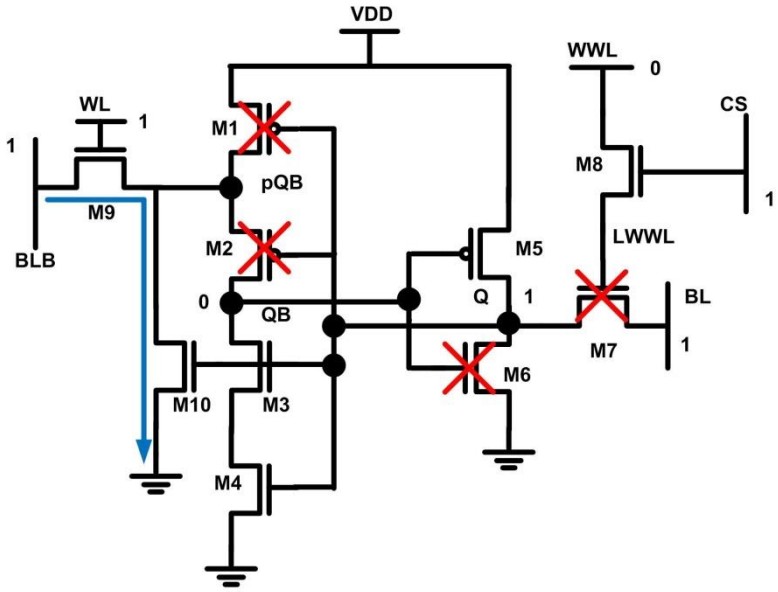


Fig. 3. The proposed 10T cell during read mode.

For writing a '0' in the cell, BL is set to ground while BLB is precharged to VDD. Next, CS, WL and WWL are asserted while VVSS is kept floating. This causes node Q to discharge by BL through M7. This results in weak conduction of M1 and M2 which raises the voltage at node QB. Consequently, M6 transistor's conduction starts getting weaker which further lowers the voltage at node Q. Now, internal feedback starts to work and finally, a '0' is written in the cell. Fig. 4(a) illustrates the write '0' operation. Write '1' operation is initiated by setting BL to VDD while BLB is set to ground. Next, CS, WWL and WL are asserted while VVSS is kept floating. This causes QB to discharge by BL through M2 and M9 as shown in Fig. 4(b) [16, 22]. Now, feedback action starts to work, and Q is set to '1'.

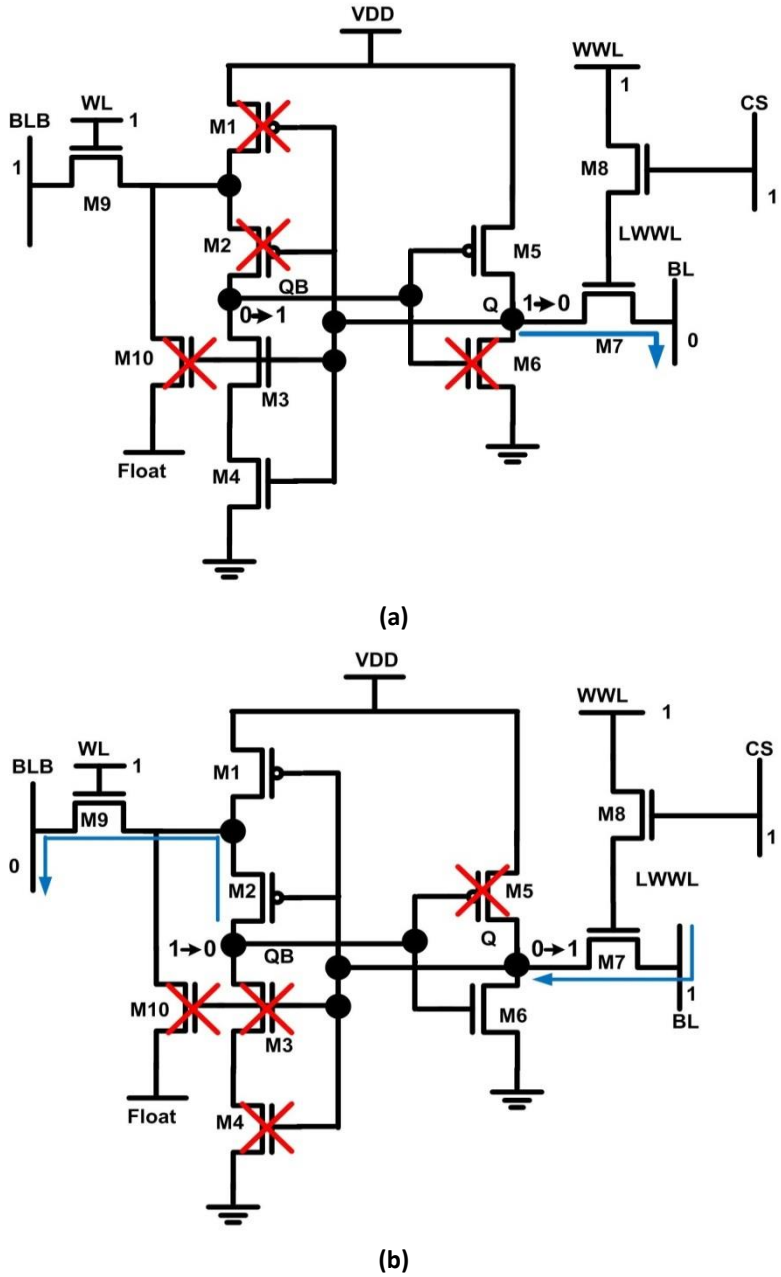


Fig. 4. a) write '0'; b) write '1' modes of the proposed cell.

In the standby mode, CS, WWL, and WL are deactivated while VVSS is set to VDD. The cell holds the data if VDD is kept ON.

3. RESULTS AND DISCUSSION

Characteristics of the proposed 10T cell for important parameters are investigated and compared with a conv6T, a Schmitt-trigger (ST) based 10T cell (now onwards referred to as ST-2 cell) [13], a PPN based 10T cell (referred as PPN10T) [16], and a PNN based 10T cell (referred to as PNN10T) [17]. The TSPICE simulation is carried out on a PTM high performance 32 nm CMOS technology for evaluation purpose [23].

3.1. Read Stability

The term RSNM is used to represent the read stability. RSNM is defined as the maximum value of noise voltage at the storage nodes of the cell without cell upset. Graphically, RSNM is found by embedding the largest square in the read-mode butterfly curve. The side length of this square is equal to the RSNM [24]. Read butterfly curves for the proposed design along with other cells are illustrated in Fig. 5. The proposed design shows a 4.77x (1.38x) larger RSNM compared to the conv6T (ST-2) cell at 0.4 V. Improvement in the RSNM is attributed to the OFF transistor M2 which does not allow charge-sharing between BLB and node QB during the read operation. Fig. 6 shows the variation of the RSNM with the supply voltage. From the graph shown in Fig. 6, it is observed that the proposed cell offers enhanced RSNM for the entire voltage range (from 0.4 V to 0.8 V). At 0.8 V, the proposed cell achieves 3.04x larger RSNM compared to the conv6T cell.

At fast NMOS slow PMOS (FNSP) corner (the worst case for the RSNM), our cell exhibits 4.48x larger RSNM compared to that of the 6T cell as shown in Fig. 7.

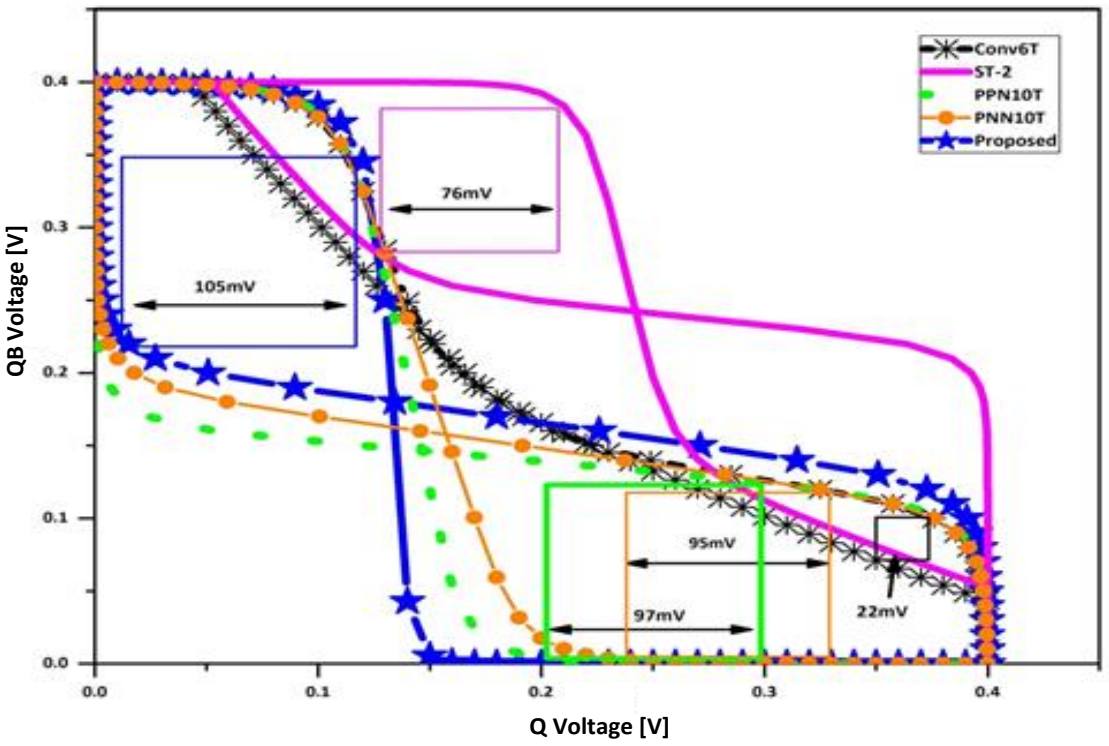


Fig. 5. Read butterfly curves of the proposed and other – reported in literature - cells.

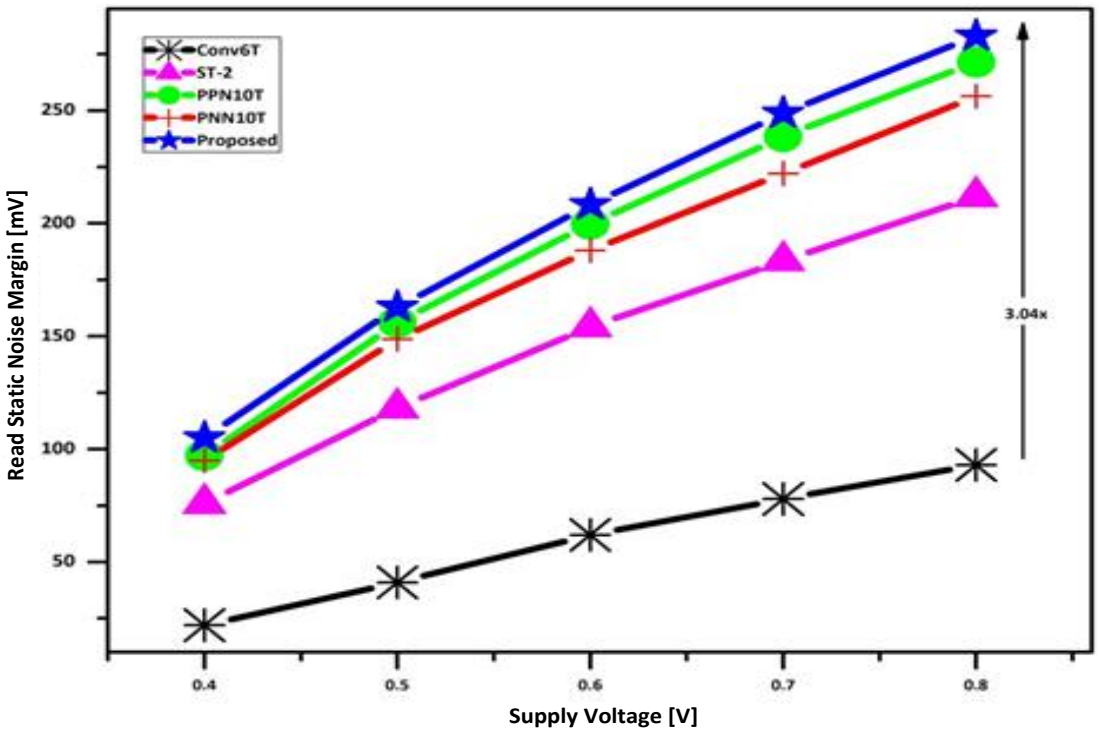


Fig. 6. RSNM versus supply voltage of the proposed and other – reported in literature - cells.

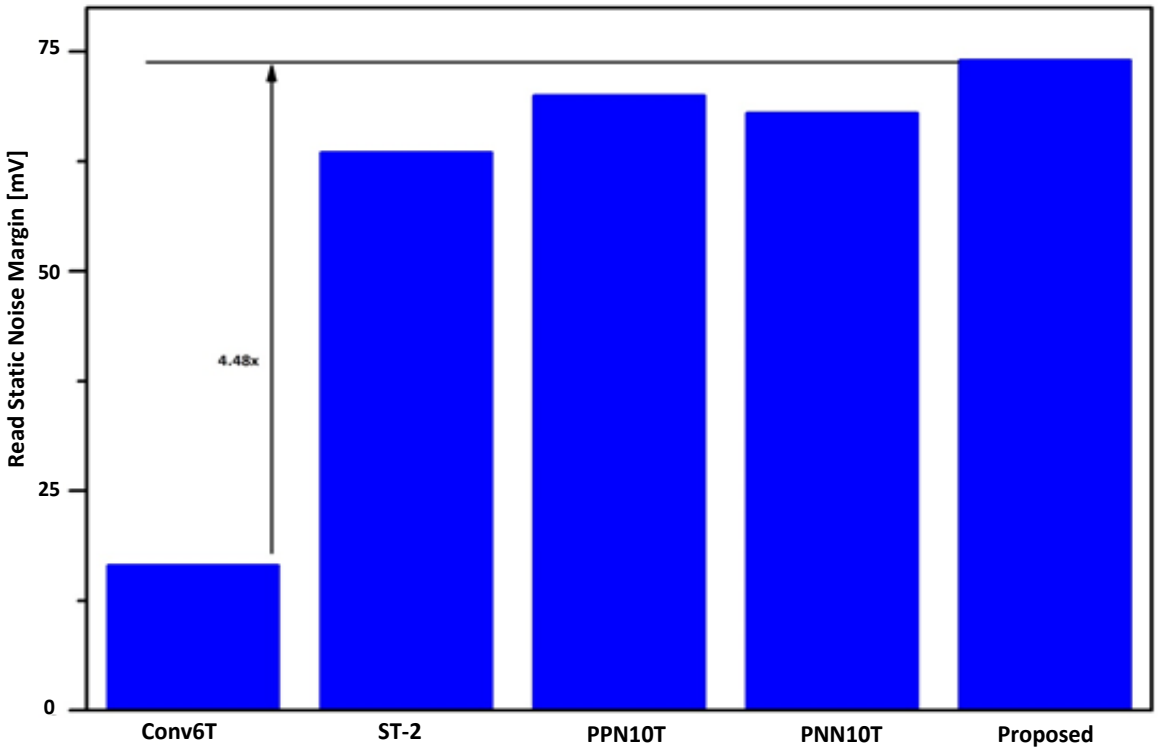


Fig. 7. RSNM at FNSP corner of the proposed and other – reported in literature - cells.

3.2. Write Ability

The write ability of an SRAM cell is represented by the metric write static noise margin (WSNM). The butterfly curve method is used to estimate WSNM.

Write ability of an SRAM cell is estimated by breaking the feedback loop of the cell and applying a voltage source V1 at the input of the right inverter as shown in Fig. 8(a). Now, the voltage source V1 is swept from 0 to VDD and corresponding voltage-transfer curve (VTC) is obtained at node Q. Similarly, a voltage source V2 is applied at the input of left-side inverter to obtain VTC at node QB. A butterfly curve is formed by superimposing VTC of left inverter and inverted VTC (VTC^{-1}) of right inverter as shown in Fig. 8(b). The two VTCs in Fig. 8(b) intersect at only one point means that the cell is in mono-stable state. This implies that the cell performs reliable write operation. To estimate the write-ability, a maximum sized square is embedded inside the lower lobe of the butterfly curve. The length of the leg of the embedded square is estimated as the WSNM [25]. Fig. 8(b) shows the WSNM for write '1' mode. Similarly, WSNM for write '0' can also be estimated.

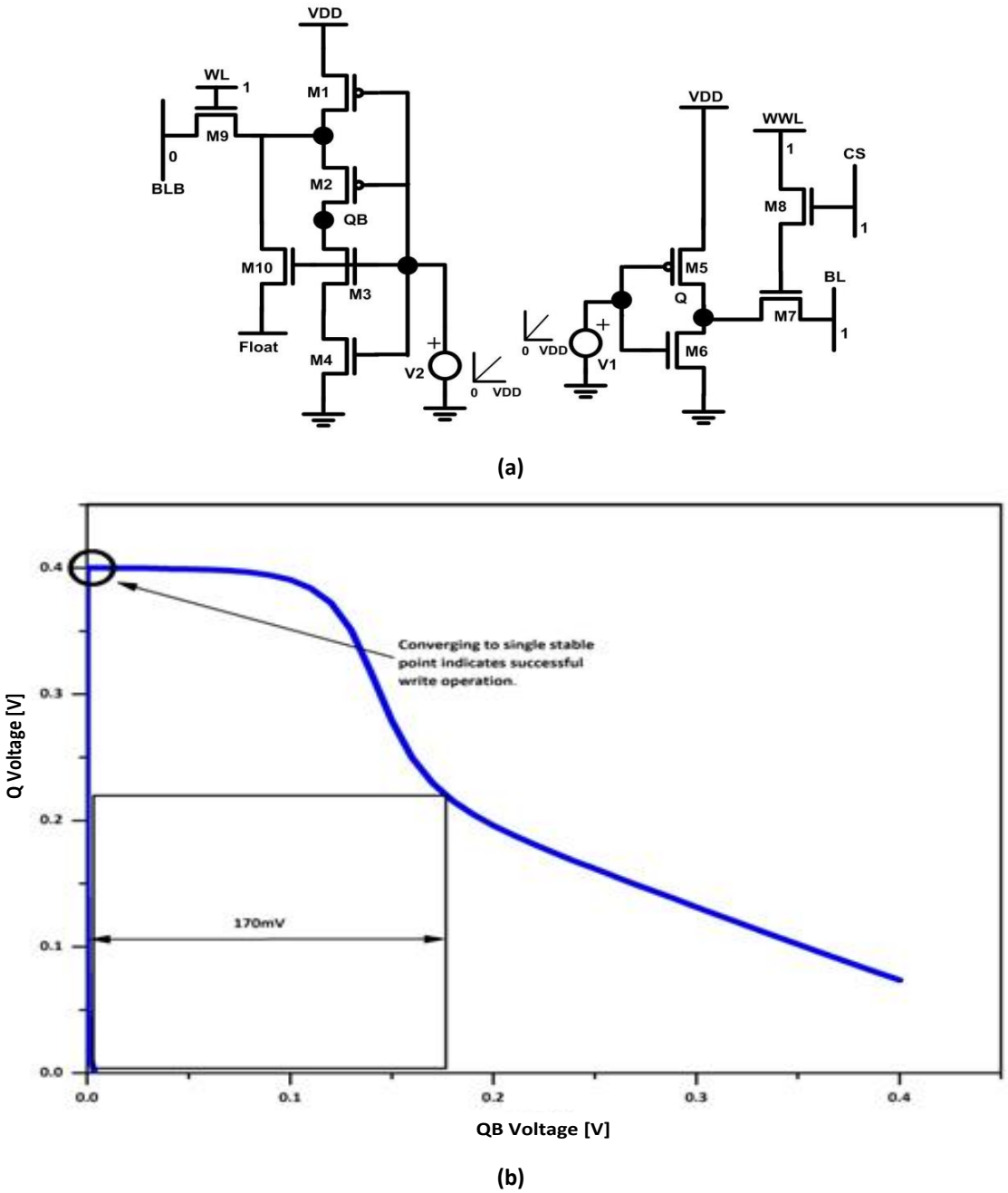


Fig. 8. Estimation of write-ability: a) circuit set-up; b) write butterfly curve.

Fig. 9 shows the write butterfly curve for the proposed design during write '1'. As shown in Fig. 9, the proposed design exhibits 1.18x, 1.25x, and 1.31x larger SNM (during write '1') compared to that of 6T, PPN10T, and PNN10T cells, respectively, at 0.4 V. Larger write '1' SNM of the proposed circuit is due to the fact that unlike PPN10T and PNN10T cells which employ two series transistors in their write paths, the proposed design uses only one transistor (M7) between bit line BL and storage node Q. However, SNM (write '0') of the proposed design is 0.98x of the 6T cell at 0.4 V as shown in Fig. 10.

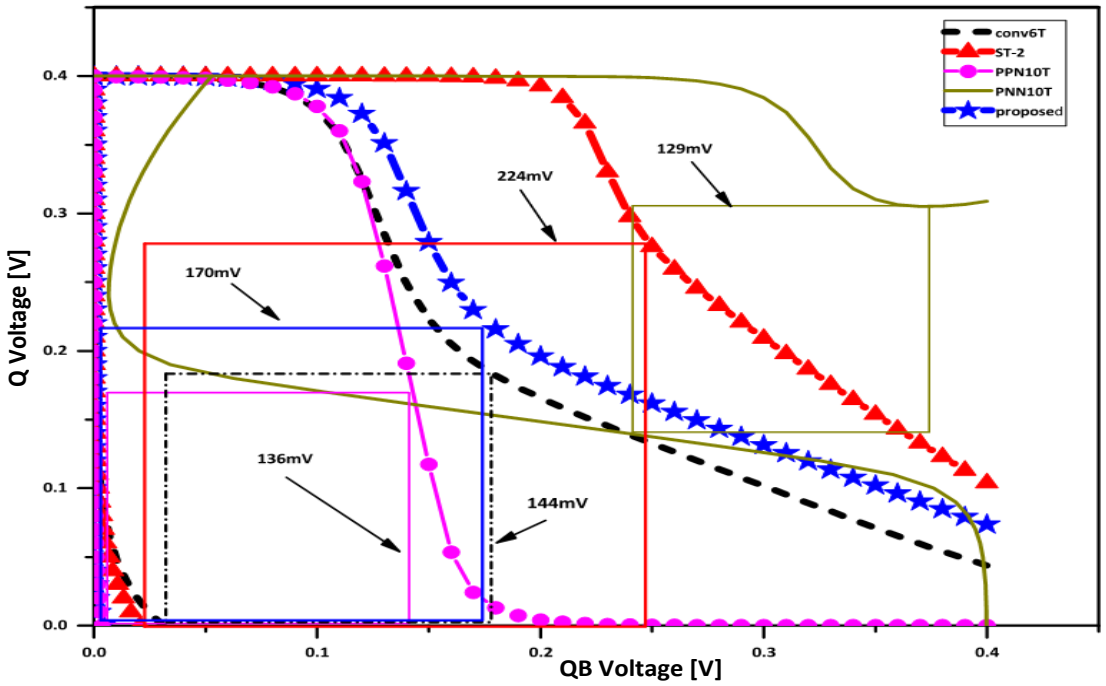


Fig. 9. Butterfly curves during write '1' mode of the proposed and other – reported in literature - cells.

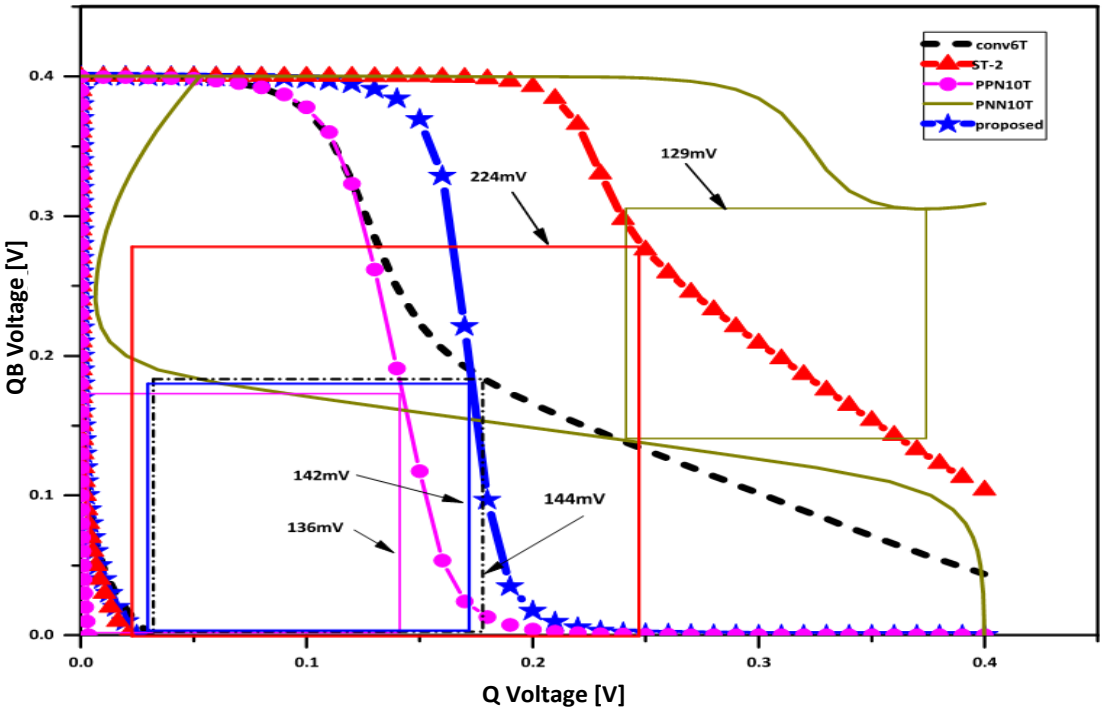


Fig. 10. Butterfly curves during write '0' mode of the proposed and other – reported in literature - cells.

3.3. Write/ Read Delay and Power Dissipation

Table 2 shows the write and read delay of the proposed 10T and other cells under consideration. The proposed design exhibits 3.27x shorter write delay as compared to the PPN10T cell at 0.4 V. This is attributed to the low resistive path (due to use of a single transistor M7) between Q and BL of our cell. On the other hand, the PPN10T cell uses two series transistors in its write path causing high resistance. However, the ST-2 cell offers the lowest write delay followed by the conv6T cell. The read delay of our design is 0.83x of the ST-2 cell as given in Table 2. Our cell and the PPN10T cell offer approximately same read delay as their read buffer consists of equal number of transistors with same strength.

Write power consumption in the proposed design is 1.86x lower compared to that of the conv6T cell at 0.4 V. Since, the conv6T cell offers shorter delay in writing; therefore, it draws larger current from the supply voltage during write. Table 2 also shows read power consumption for different cells. Our cell dissipates 1.4x lesser read power than the 6T cell. This is due to lower switching activities in our cell which employs a single-ended read scheme.

Table 2. Write/read delay and power consumption the proposed and other – reported in literature - cells at 0.4 V.

SRAM cell	Write mode		Read mode	
	Delay [ns]	Power [nW]	Delay [ns]	Power [nW]
Conv6T	1.49	210.44	3.0	210.2
ST-2 [13]	1.64	85.3	4.25	233.8
PPN10T [16]	197.6	75.0	3.54	230.0
PNN10T [17]	26.3	33.7	2.66	161.1
Proposed cell	60.3	112.9	3.55	149.3

3.4. Leakage Power

In a submicron regime, leakage or static power has become a major concern in today's high-density SRAMs. Mostly, a major portion of SRAM remains inactive. Therefore, current through idle cells causes dissipation of static power [7]. Since subthreshold current is the major contributor to the static power dissipation; therefore, reduction in subthreshold current is necessary in order to reduce leakage power. Subthreshold current in an OFF transistor is due to voltage difference between its drain and source terminals [26, 27]. In the proposed cell, leakage current in the left inverter is reduced drastically as it consists of four transistors in series. Bit line leakage current through read buffer (M9-M10) is also reduced as VVSS is set to VDD in hold mode. Note that leakage power in the proposed 10T cell is the average of leakage power during hold '0' and hold '1' modes. Fig. 11 shows leakage power variation with VDD voltage for the cells under consideration. Our cell dissipates 3.21x lesser power than the conv6T cell at 0.4 V.

3.5. Bit Interleaving

As mentioned earlier, bit-interleaved architecture is considered an effective scheme to mitigate the soft errors [3]. However, the conv6T cell does not support bit-interleaved architecture due to half-select disturbance. Fig. 12 shows a 2 × 2 bit-interleaved architecture of the proposed 10T cell. Suppose a logic '1' is to write in the row-0, column-0 cell. For this,

WWL_0, WL_0 and CS_0 are set to logic '1'. Bitlines BL_0 and BLB_0 are loaded with logic '1' and logic '0', respectively. This results in a '1' is written in the selected cell as shown in Fig. 12. However, a Row-half selected (RHS) cell does not undergo half-select disturbance as BLB_1 = '1' (therefore, no charge transfer from QB to BL) and CS_1 = '0' (M7 is OFF). Similarly, a column half-select cell does not undergo half-select disturbance as WWL_1 and WL_1 are low.

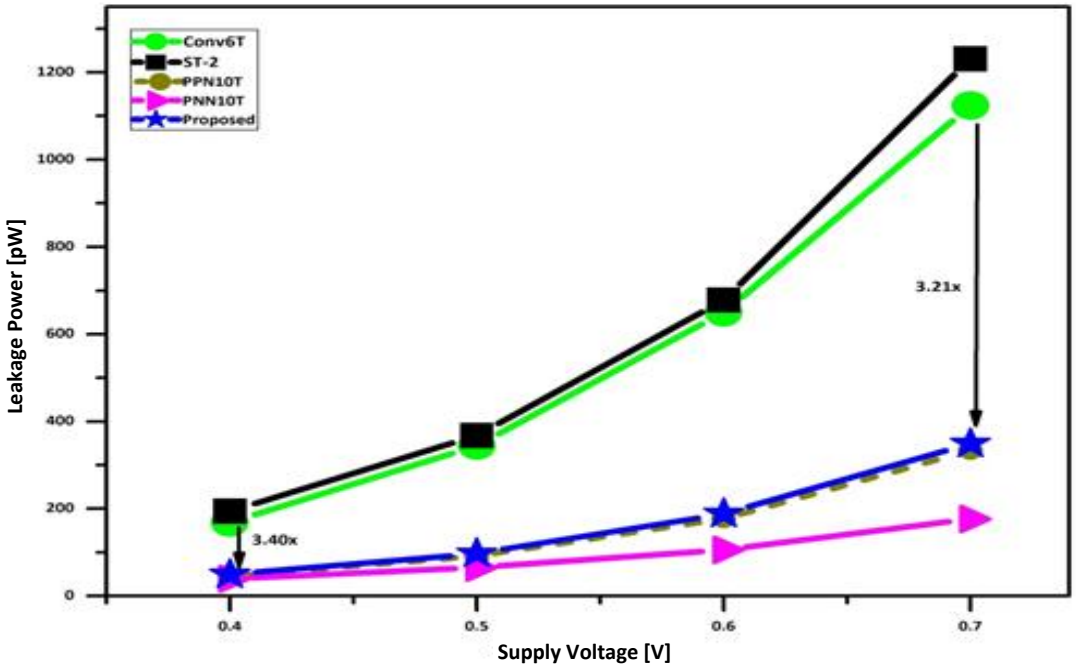


Fig. 11. Leakage power versus supply voltage of the proposed and other – reported in literature - cells.

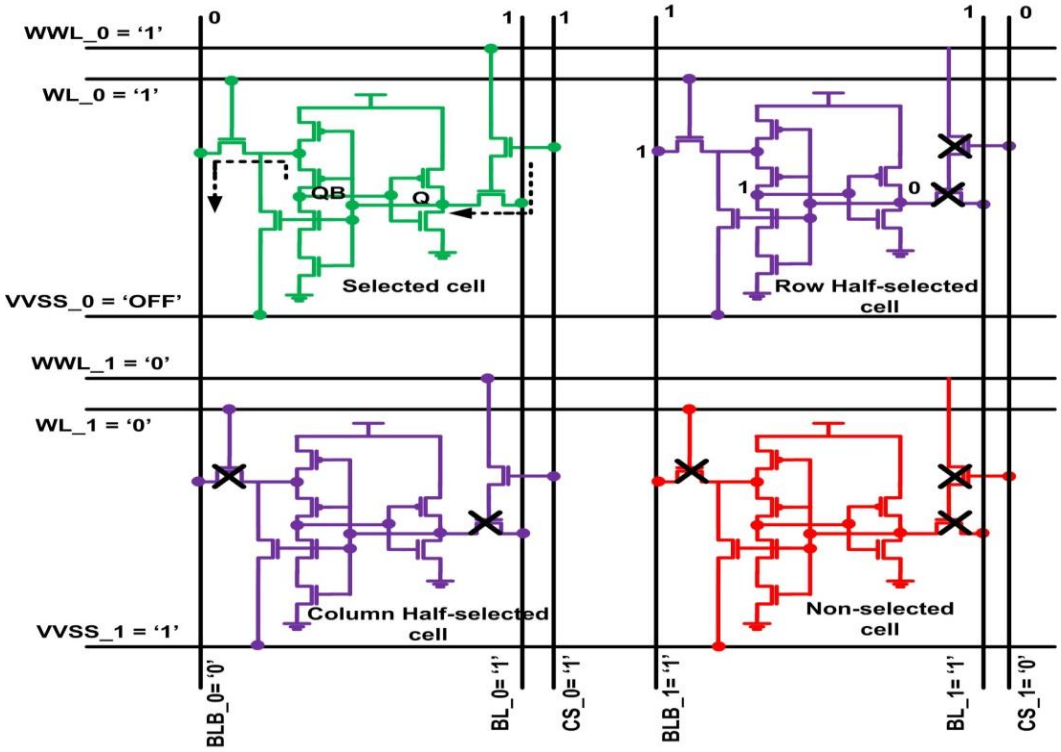
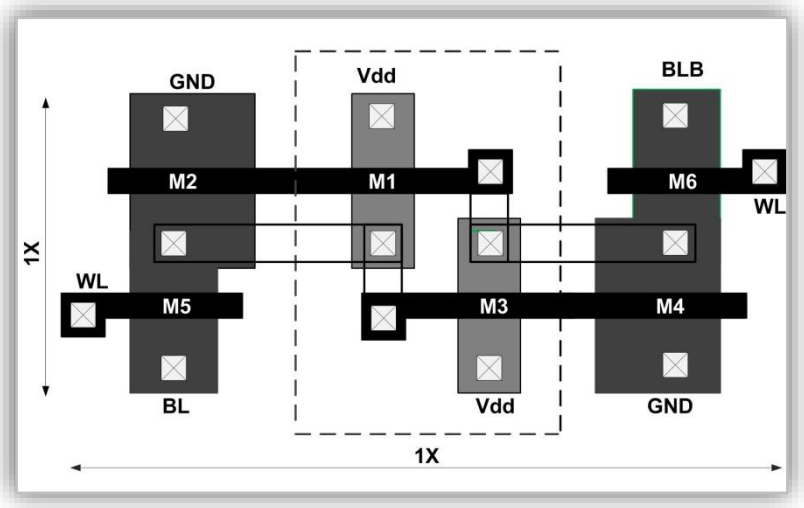


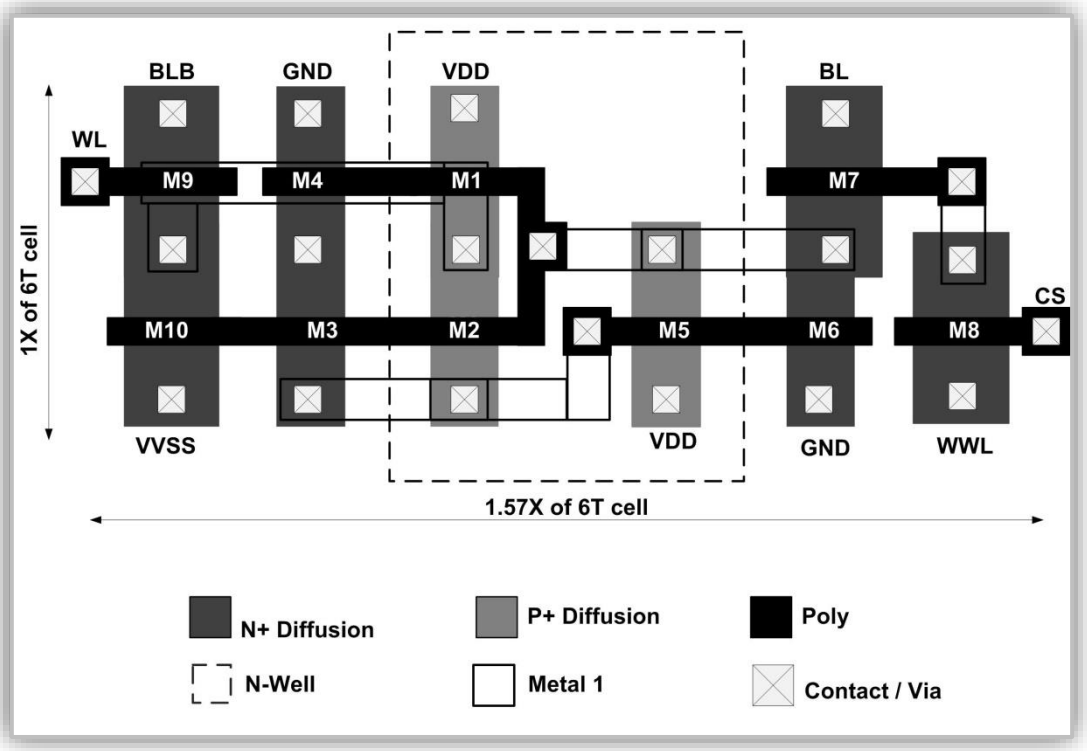
Fig. 12. 2 × 2 Bit-interleaved architecture of the proposed 10T cell.

3.6. Area Layout

Fig. 13 shows the layouts of conv6T and the proposed 10T cells using 32 nm CMOS process technology rules [28]. As shown in Fig. 13, vertical dimensions of the proposed 10T and that of the 6T cells are equal (two poly pitches). In the horizontal direction, six columns of active regions are used in our cell whereas only four in the conv6T cell. Therefore, layout of the proposed circuit is 1.57× longer than the conv6T cell in horizontal direction. Thus, the chip area of our design is 1.57x of the 6T cell.



(a)



(b)

Fig. 13. Layout of the: a) conv6T; b) proposed 10T cells.

3.7. Comparison of the Proposed Cell with Other – Reported in Literature - Cells

Table 3 provides a comparison of the suggested 10T cell with other cells under consideration. As can be observed from Table 3, our cell shows the largest RSNM (105 mV) among all the cells under consideration. At 0.4 V, WSNM (during write '1') of the proposed cell is 1.18x larger compared to the conv6T cell. The leakage power of our cell is 0.29x of the conv6T cell, at 0.4 V. However, the proposed cell consumes 1.57x more area compare to the conv6T cell. Our cell supports bit-interleaving architecture; therefore, it can tolerate the soft errors. Besides, single-ended read scheme in the proposed cell results in low power consumption during a read operation. Thus, the proposed cell is useful in battery operated portable devices.

Table 3. Comparison of the proposed and other – reported in literature - cells at 0.4 V.

SRAM cell	Conv6T	ST-2 [13]	PPN10T [16]	PNN10T [17]	Proposed
No. of Transistors	6	10	10	10	10
Read operation	Differential	Differential	Differential	Differential	Single-ended
Read-disturb free	No	Yes	Yes	Yes	Yes
RSNM [mV]	22	76	97	95	105
WSNM [mV] During write '1'	144	224	136	129	170
WSNM [mV] During write '0'	144	224	136	129	142
Bit-interleaving	No	----	Yes	Yes	Yes
Leakage power [pW]	168.3	194.3	45.4	39.6	49.4
Layout Area (Normalized)	1x	1.92x	1.64x	---	1.57x

4. CONCLUSIONS

A read-decoupled 10T SRAM cell was proposed in this paper. The single ended read feature of the cell leads to lower read power consumption. The proposed cell offers 4.77x (1.38x) larger RSNM compared to a conv6T (ST-2) cell at 400 mV. Moreover, it exhibits 3.27x shorter write-delay than that of a PPN10T cell. Write power consumption in the proposed design is 1.86x lesser than that of a conv6T cell, and its static power dissipation is 3.47x lesser compared to a conv6T cell. However, the proposed cell requires 1.57x more area compared to a conv6T cell at 32 nm CMOS technology.

REFERENCES

[1] Adikpe, M. Iyobhebhe, C. Amlabu, I. Botson, B. Omojola, J. Bashayi, C. Ezugwu, "A review on wireless fidelity co-location technology adopted indoors for technology-based contact tracing," *Jordan Journal of Electrical Engineering*, vol. 8, no. 2, pp. 133-150, 2022.

[2] A. Miyim, M. Ismail, "Dynamic routing protocol for QoS enhancement in wireless mobile ad-hoc networks," *Jordan Journal of Electrical Engineering*, vol. 7, no. 1, pp. 29-42, 2021.

[3] J. Sun, H. Guo, G. Li, H. Jiao, "An ultra-low-voltage bit-interleaved synthesizable 13T SRAM circuit," *IEEE Journal of Solid State Circuits*, vol. 57, no. 11, pp. 3477-3489, 2022.

[4] A. Do, S. Zeinolabedin, T. Kim, "Energy-efficient data-aware SRAM design utilizing column-based data encoding," *IEEE Transactions on Circuits and Systems II: Express Brief*, vol. 67, no. 10, pp. 2154-2158, 2020.

[5] N. Yadav, A. Shah, S. Vishvakarma, "Stable, reliable, and bit-interleaving 12T SRAM for space applications: a device circuit co-design," *IEEE Transaction on Semiconductor Manufacturing*, vol. 30, no. 3, pp. 276–284, 2017.

[6] S. Mansore, R. Gamad, "A data-aware write-assist 10T SRAM cell with bit-interleaving capability," *Turkish Journal of Electrical Engineering and Computer Sciences,* vol. 26, no. 5, pp. 2361–2373, 2018.

[7] A. Calimera, A. Macii, E. Macii, M. Poncino, "Design techniques and architectures for low-leakage SRAMs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 9, pp. 1992-2007, 2012.

[8] J. Rabaey, *Digital Integrated Circuits: A Design Perspective*, New Delhi: PHI, 2000.

[9] R. El Senousy, S. Ibrahim, W. Anis, "Stability analysis and design methodology of near-threshold 6T SRAM cells," *28th International Conference on Microelectronics*, pp. 225-228, 2016.

[10] R. Joshi, R. Kanj, V. Ramadurai, "A novel column-decoupled 8T cell for low-power differential and domino-based SRAM design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 19, no. 5, pp. 869-882, 2010.

[11] R. Baumann, "Soft errors in commercial integrated circuits," *International Journal of High Speed Electronics and Systems,* vol. 14, no. 2, pp. 299-309, 2004.

[12] L. Chang, R. Montoye, Y. Nakamura, K. Batson, R. Eickemeyer, R. Dennard, W. Haensch, D. Jamsek, "An 8T SRAM for variability tolerance and low-voltage operation in high performance caches," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 956-962, 2008.

[13] J. Kulkarni, K. Roy, "Ultralow-voltage process-variation-tolerant Schmitt-trigger-based SRAM design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 2, pp. 319-332, 2011.

[14] Y. Chiu, Y. Hu, M. Tu, J. Zhao, Y. Chu, S. Jou, C. Chuang, "40 nm bit-interleaving 12T subthreshold SRAM with data-aware write-assist," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 9, pp. 2578-2585, 2014.

[15] J. Kim, P. Mazumder, "A robust 12T SRAM cell with improved write margin for ultra-low power applications in 40 nm CMOS," *Integration,* vol. 57, pp. 1-10, 2017.

[16] C. Lo, S. Huang, "PPN based 10T SRAM cell for low-leakage and resilient subthreshold operation," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 3, pp. 695-704, 2011.

[17] Y. Chien, J. Wang, "A 0.2 V 32-Kb 10T SRAM with 41 nW standby power for IoT applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 8, pp. 2443-2454, 2018.

[18] N. Yadav, Y. Kim, S. Li, K. Choi, "Stable, low power and bit-interleaving aware SRAM memory for multi-core processing elements," *Electronics,* vol. 10, pp. 2724, 2021.

[19] S. Pal, D. Divya Sri, W. Ki, A. Islam, "Soft-error resilient read decoupled SRAM with multi-node upset recovery for space applications," *IEEE Transactions on Electron Devices*, vol. 68, no. 5, pp. 2246–2254, 2021.

[20] S. Mansore, R. Gamad, D. Mishra, "A single-ended read disturb-free ppn based 9T SRAM cell," *Revue Roumaine Des Sciences Techniques-Serie Electrotechnique Et Energetique,* vol. 63, no. 3, pp. 295-299, 2018.

[21] E. Abbasian, "A highly stable low-energy 10T SRAM for near-threshold operation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 12, pp. 5195-5205, 2022.

[22] S. Mansore, R. Gamad, D. Mishra, "A 32 nm read disturb-free 11T SRAM cell with improved write ability," *Journal of Circuits, Systems and Computers*, vol. 29, no. 5, pp. 2050067, 2020.

[23] *Predictive Technology Model (PTM),* 2008. < http://ptm.asu.edu>

[24] E. Seevinck, F. List, J. Lohstroh, "Static noise margin analysis of MOS SRAM cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748-754, 1987.

[25] A. Islam, M. Hasan, "Leakage characterization of 10T SRAM cell," *IEEE Transactions on Electron Devices*, vol. 59, no. 3, pp. 631–638, 2012.

[26] G. Pasandi, S. Fakhraie, "An 8T low voltage and low-leakage half selection disturb-free SRAM using bulk-CMOS and FinFETs," *IEEE Transactions on Electron Devices*, vol. 61, no. 7, pp. 2357-2363, 2014.

[27] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, M. BohR, "SRAM design on 65-nm CMOS technology with dynamic sleep transistor for leakage reduction," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 895-901, 2005.

[28] S. Gupta, K. Gupta, N. Pandey, "A 32-nm subthreshold 7T SRAM bit cell with read assist," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 12, pp. 3473-3483, 2017.