JJEE
Volume 9 | Number 2 | June 2023 | Pages 189-208

Jordan Journal of Electrical Engineering

ISSN (print): 2409-9600, ISSN (online): 2409-9619

Homepage: jjee.ttu.edu.jo

A New Positive Output High Gain Quadratic Buck-Boost Converter: Analysis, Design and Control

Majid Hosseinpour[1*], Armineh Dastgiri[2]

[1, 2] Department of Electrical Engineering, University of Mohaghegh Ardabili, Ardabil, Iran
E-mail: hoseinpour.majid@uma.ac.ir

Received: December 08, 2022 *Revised: January 18, 2023* *Accepted: January 25, 2023*

***Abstract*—** In this paper, a non-isolated quadratic and buck-boost converter based on the Zeta structure is proposed, and its operating principle and analysis of its steady-state is discussed. Also, the parameter design is presented, and on-idealities are considered in the power circuit to analyze - in detail - the real voltage gain and efficiency of the proposed converter. Moreover, a simulation prototype is implemented to validate the theoretical analysis, and a comparison of the proposed converter with other similar topologies and small-signal models is conducted. The results show that - unlike the classic buck-boost converters - the proposed converter has a positive output voltage and a quadratic voltage gain that is higher than the traditional Zeta converters. Also, it has advantages such as common ground characteristics between output/input voltage terminals, continuous input current, simple structure and high efficiency. Additionally, the voltage stresses across the power switches of the proposed converter are less than half of the output voltage or equal to the sum of the input and output voltages. Therefore, the low on-resistance power switches are employed to reduce power losses and improve efficiency. On top of that, the high quadratic voltage gain and positive output polarity features present the superiority of the proposed converter against other similar converters.

***Keywords*—** Buck-boost converter; Zeta converter; Positive output voltage; Quadratic voltage gain.

1. INTRODUCTION

In the present era, renewable energy sources, including photovoltaic (PV) systems, wind turbines (WTs), fuel cells (FCs), and other energies, have experienced dramatic growth because of fossil fuel shortages and severe environmental problems such as air pollution, global warming, etc. [1, 2]. Therefore, the research in the field of DC/DC converters to achieve high voltage is increasing day by day [3, 4]. However, the conventional boost converter is not a proper solution due to limited voltage gain with an increment in the duty cycle, high power losses, and high voltage stress across the power switches [5]. Thus, DC/DC converters can be explained as isolated and non-isolated converters. Isolated DC/DC converters can achieve high voltage gain through using high-frequency transformers [6]. However, this solution leads to voltage spikes. So, snubber circuits and clamping techniques are needed to decrease the voltage spike, which increases the volume and cost of the converters [7, 8]. Hence, the non-isolated converters have become more attractive due to their low cost, size, and simple structure [9, 10]. Also, non-isolated converters can be classified into two categories; coupled inductors and non-coupled inductor converters. In coupled inductor-based converters, high voltage gain can be obtained by adjusting the turns ratio of the coupled inductor. However, these converters have drawbacks

* Corresponding author
Article's DOI: 10.5455/jjee.204-1670524690

such as voltage spikes, leakage inductances, complex systems, etc. [11, 12]. Non-coupled inductor converter includes switched inductor (SI) circuit [13], switched capacitor (SC) circuit [14, 15], voltage lift (VL) circuit [16], interleaved circuit [17], voltage multiplier cell (VMC) [18] and quadratic converter [19].

Each of the converters as mentioned earlier is derived from the conventional boost converter [20]. Hence, these converters can only increase the voltage without the ability to decrease the voltage, which causes difficulties in applications with both step-up and step-down capabilities. Therefore, buck-boost-based DC/DC converters are the proper choice for such applications. The conventional buck-boost converter can either increase or decrease the input voltage to the desired value [21]. However, negative output voltage, discontinuous input current, high inductor current stress, and low efficiency are the main drawbacks of this converter, which limits its application [22]. SEPIC, CUK, and Zeta are other primary buck-boost converters. Although these converters are effective in some options, the voltage gain is the same as the conventional buck-boost converter [23]. A large duty cycle is thus required to get a high voltage gain, which reduced converter efficiency. To overcome these drawbacks, various buck-boost topologies with improved techniques are discussed in different works of literature.

High voltage gain buck-boost converters with a single switch are proposed in [24, 25]. A non-isolated cascaded converter is presented in [26]. Although the presented converter has the square voltage gain of the conventional buck-boost converter, it suffers from high voltage stress across the semiconductors. In [27], a buck-boost converter is proposed to obtain high voltage gain with low voltage stress on the elements by using voltage multipliers. Reference [28] reported a converter with continuous input current that achieves a three times greater voltage gain in comparison to the conventional buck-boost converter. A high voltage gain quadratic converter is reported in [29]. However, this converter's primary shortcomings are the discontinuous input current and the negative output polarity. A positive output polarity converter is reported in [30], in which the floating ground is a serious problem. A family of buck-boost converters is presented in [31]. These converters have an expendable conversion ratio. However, utilizing a high amount of semiconductors leads to an increase in total cost.

According to recent papers, it can be deduced that having a quadratic structure [32] is a useful feature for new structures. For this purpose, cascading the structures leads to the quadratic type converter. Also, cascading conventional buck-boost converters such as ZETA converters with different structures make a good solution in which the useful features for new structures can be obtained [26]. A quadratic buck-boost converter is reported in [33] with zero output voltage ripple at a selectable operating point. However, the drawbacks of this structure include negative output polarity and high voltage stress across the output diode. A positive output polarity converter is reported in [34], which has continuous current in the input and output terminals. Nevertheless, it cannot achieve a high voltage gain ratio. New transformer-less quadratic and semi-quadratic buck-boost converters are proposed in [35, 36], respectively. Both proposed converters can achieve high voltage gain, but they have negative output polarity. A zeta-based converter with common ground characteristics is reported in [37], in which the discontinuous input current is the main disadvantage. The inverted high step-down (IHSD) converter introduced in [38] has low stress across the components.

Based on the merits and demerits of the aforementioned buck-boost converters, providing continuous input current, positive output voltage, common ground, and high voltage gain are essential to discover a new buck-boost converter. Consequently, a non-isolated quadratic and buck-boost converter based on the Zeta structure is proposed in this paper. As mentioned, the proposed converter benefits from the advantages such as common ground characteristics between output/input voltage terminals, continuous input current, simple structure, and quadratic voltage gain. Moreover, the low voltage stresses across the power switches of the proposed converter or identical compared to the sum of the input and output voltages leads to low power conduction losses and high efficiency.

The rest of the paper is organized as follows: The proposed converter configuration and operating principle are described in section 2. Section 3 presents the steady-state analysis of the proposed converter. In section 4, the parameter design process of the proposed converter is examined. Section 5 discusses the real voltage gain and efficiency calculations by considering the impact of non-ideals on the converter performance. The comparison is also provided in section 6. The small-signal modeling is covered in section 7. Section 8 displays the simulation outcomes used to confirm the theoretical relations. Finally, section 9 concludes the paper.

2. PROPOSED TOPOLOGY AND OPERATING MODES

As demonstrated in Fig. 1, the configuration of the proposed converter is derived by combining the quadratic buck-boost converter with a ZETA converter in a way that it has merits over the cascaded converters. Improved efficiency is one of the mentioned merits. The power circuit of the proposed converter comprises two simultaneously controlled power switches, S_1 and S_2, two inductors L_1 and L_2, diode D_1, and capacitor C_1 as a quadratic structure, a Zeta structure consists of common power switch S_2 and inductor L_2 with quadratic structure, diode D_2, and capacitor C_2, an output LC filter consist of inductor L_3 and capacitor C_o, and load R. Based on the ON and OFF control of the power switches, the proposed converter has two states whose equivalent circuits and key waveforms are depicted in Figs. 2 and 3, respectively. To facilitate the analysis of the proposed converter, the following assumptions are assumed:

- The converter operates in continuous conduction mode (CCM).
- All the components are ideal.
- All the capacitors are large enough that the voltage across them is considered constant.

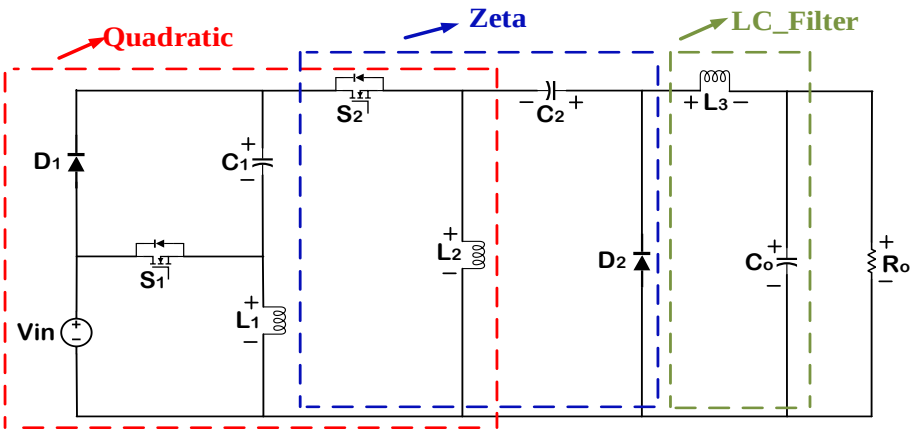


Fig. 1. Configuration of the proposed quadratic buck-boost converter based on the Zeta structure.

First state: according to Fig. 2(a), both switches S_1 and S_2 are turned on in the first state. The diodes D_1 and D_2 are reversed-biased. Inductor L_1 charges in parallel through S_1 by voltage source V_{in}. Simultaneously, inductor L_2 is charged by voltage source V_{in} and capacitor C_1 via switches S_1 and S_2. Also, inductor L_3 charges by the voltage source, the capacitors C_1 and C_2, and load. Moreover, capacitors C_1 and C_2 are discharged, and the capacitor C_o supplies power to the load R. The steady-state equations are as follows:

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_{in} \\ v_{L2} = L_2 \dfrac{di_{L2}}{dt} = V_{in} + v_{C1} \\ v_{L3} = L_3 \dfrac{di_{L3}}{dt} = V_{in} + v_{C1} + v_{C2} - V_o \end{cases}, \begin{cases} i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = -i_{L2} - i_{L3} \\ i_{C2} = C_2 \dfrac{dv_{C2}}{dt} = -i_{L3} \\ i_{Co} = C_o \dfrac{dv_{Co}}{dt} = i_{L3} - I_o \end{cases} \quad (1)$$

Second state: the equivalent circuit of the second state is displayed in Fig. 2(b). Switches S_1 and S_2 are both turned off during this state. The diodes D_1 and D_2 are forward-biased. Inductor L_1 is discharged by voltage source V_{in} and capacitor C_1 via diode D_1. Simultaneously, inductor L_2 and inductor L_3 release energy by capacitor C_1 and capacitor C_o via diode D_2, respectively. Moreover, capacitor C_1 is charged, and capacitor C_2 receives energy from inductor L_2. The capacitor C_o supplies power to the load R. The equations of the steady-state condition can be obtained as Eq. (2).

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_{in} - v_{C1} \\ v_{L2} = L_2 \dfrac{di_{L2}}{dt} = -v_{C2} \\ v_{L3} = L_3 \dfrac{di_{L3}}{dt} = -V_{Co} \end{cases}, \begin{cases} i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = i_{L1} \\ i_{C2} = C_2 \dfrac{dv_{C2}}{dt} = i_{L2} \\ i_{Co} = C_o \dfrac{dv_{Co}}{dt} = i_{L3} - I_o \end{cases} \quad (2)$$

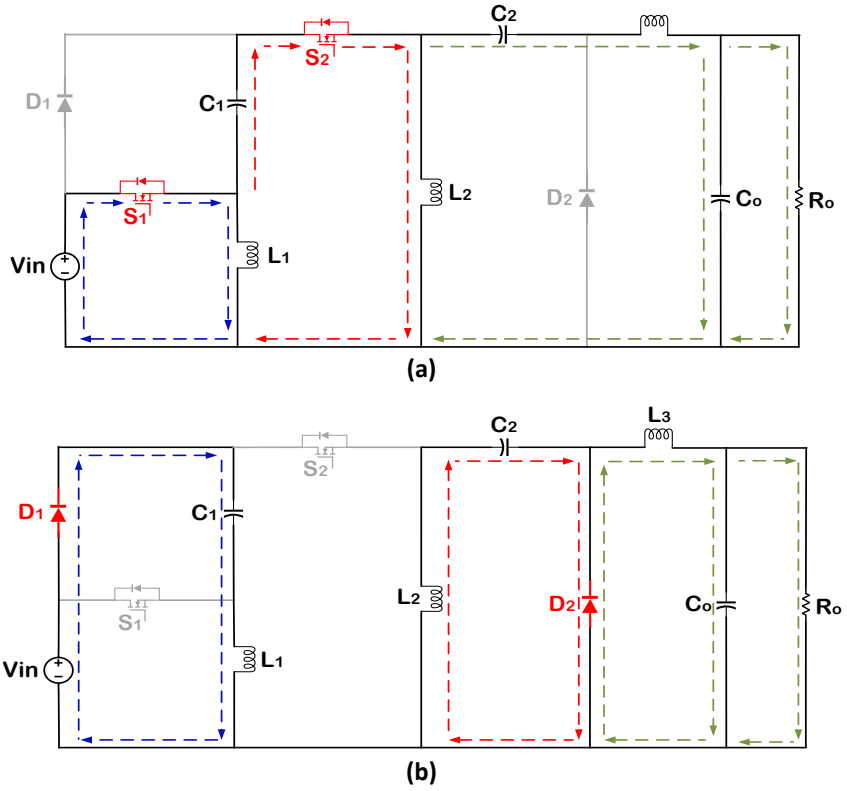


Fig. 2. Operation modes of the proposed structure: a) first mode; b) second mode.

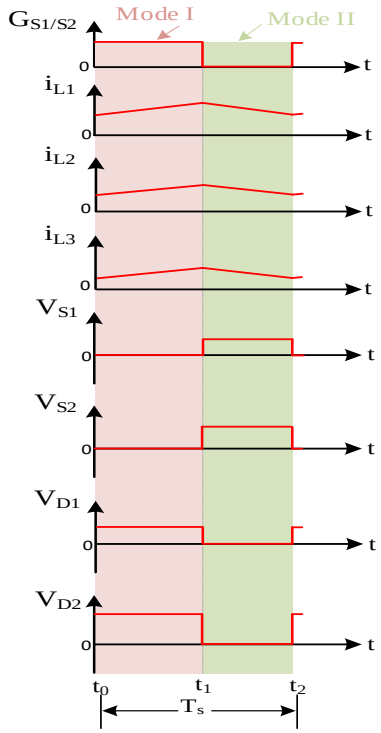


Fig. 3. Key waveforms of the proposed structure.

3. STEADY STATE ANALYSIS

3.1. Analysis of Voltage Gain

Applying the average voltage over a period across the inductors L_1, L_2, and L_3 results in the following equations:

$$\begin{aligned} &(a)\ DV_{in}+(1-D)(V_{in}-v_{C1})=0 \\ &(b)\ D(V_{in}+v_{C1})+(1-D)(-v_{C2})=0 \\ &(c)\ D(V_{in}+v_{C1}+v_{C2}-V_o)+(1-D)(-V_o)=0 \end{aligned} \tag{3}$$

By using Eq. (3.a), the voltage across capacitor C_1 can be obtained as:

$$v_{C1}=\frac{V_{in}}{1-D} \tag{4}$$

where D is the duty cycle of switches S_1 and S_2.

From Eqs. (3.b) and (4), the voltage across capacitor C_2 can be derived as:

$$v_{C2}=\left(\frac{2D-D^2}{(1-D)^2}\right)V_{in} \tag{5}$$

By using Eq. (3.c) and substituting the voltage across capacitors C_1 and C_2, the output voltage can be calculated as:

$$V_o=\left(\frac{2D-D^2}{(1-D)^2}\right)V_{in} \tag{6}$$

Finally, the steady-state voltage gain equation of the proposed converter can be obtained as follows:

$$M_{ideal}=\frac{V_o}{V_{in}}=\frac{2D-D^2}{(1-D)^2} \tag{7}$$

The proposed converter operates in boost mode for $D > 0.292$, whereas it operates in buck mode for $D < 0.292$.

3.2. Analysis of Voltage Stress

By turning off the semiconductors in their equivalent circuits, the voltage stress on them can be explained. As can be seen in Fig. 2(a), the diodes D_1 and D_2 are turned off in the first state. Therefore, the voltage stress across them can be calculated as follows:

$$\begin{aligned} V_{D1} &= v_{C1} = \frac{V_{in}}{1-D} \\ V_{D2} &= V_{in} + v_{C1} + v_{C2} = \left(\frac{2-D}{(1-D)^2} \right) V_{in} \end{aligned} \tag{8}$$

According to Fig. 2(b), the voltage across switches S_1 and S_2 swings between (0, V_{C1}) and (0, V_{in} + V_{C2}), respectively. Thus, the voltage stress across them can be derived as:

$$\begin{aligned} V_{S1} &= v_{C1} = \frac{V_{in}}{1-D} \\ V_{S2} &= V_{in} + v_{C2} = \frac{V_{in}}{(1-D)^2} \end{aligned} \tag{9}$$

4. PARAMETER DESIGN CONSIDERATION

4.1. Inductor Design

CCM operation of the proposed converter is the main aim of inductor design. So, the average current of the inductor is supposed to be higher than half of its current ripple for this aim. During the first operation state, the inductors' current i_{L1}, i_{L2}, and i_{L3} increased linearly. By knowing the ripple currents $\Delta i_{L1}, \Delta i_{L2}$, and Δi_{L3} and using Eqs. (1) and (2), the minimum inductance values can be calculated as:

$$\begin{cases} L_1 \geq \dfrac{V_{in}}{\Delta i_{L1} f_s} D \\ L_2 \geq \dfrac{V_{in}}{\Delta i_{L2} f_s} (1-D) \\ L_3 \geq \dfrac{V_{in}}{\Delta i_{L3} f_s} D \end{cases} \tag{10}$$

where f_S is the switching frequency.

4.2. Capacitor Design

Calculating the average current in the inductors is essential to design capacitors based on the current flowing through them. The average currents of inductors are calculated as follows by applying the ampere second balance across the capacitors C_1, C_2, and C_o and using Eqs. (1) and (2),

$$\begin{cases} I_{L1} = \dfrac{D}{(1-D)^2} I_o \\ I_{L2} = \dfrac{D}{1-D} I_o \\ I_{L3} = I_o \end{cases} \tag{11}$$

Therefore, the capacitance values C_1, C_2, and C_o can be calculated as follows:

$$\begin{cases} C_1 \geq \dfrac{I_o}{\Delta v_{C1} f_s} \\ C_2 \geq \dfrac{I_o}{\Delta v_{C2} f_s} \\ C_o \geq \dfrac{I_o}{\Delta v_{Co} f_s}(1-D) \end{cases} \tag{12}$$

By knowing the allowable ripple ΔV_{C1}, ΔV_{C2}, and ΔV_{Co} and using Eqs. (2) and (12), the required capacitors can be selected.

5. NON-IDEAL VOLTAGE GAIN AND EFFICIENCY CALCULATIONS

Based on the non-idealities effect on the converter behavior, the real voltage gain and efficiency of the proposed converter can be deduced. Fig. 4 demonstrates the proposed converter with parasitic components. Here r_{S1} and r_{S2} are the series resistance of the switches S_1 and S_2. r_{D1} and r_{D2} are the internal resistances of the diodes D_1 and D_2, and V_{D1} and V_{D2} are the voltage drops. Moreover, r_{L1}, r_{L2}, and r_{L3} are the inductor windings resistance, and r_{C1}, r_{C2}, and r_{Co} are the equivalent series resistance of C_1, C_2, and C_o.

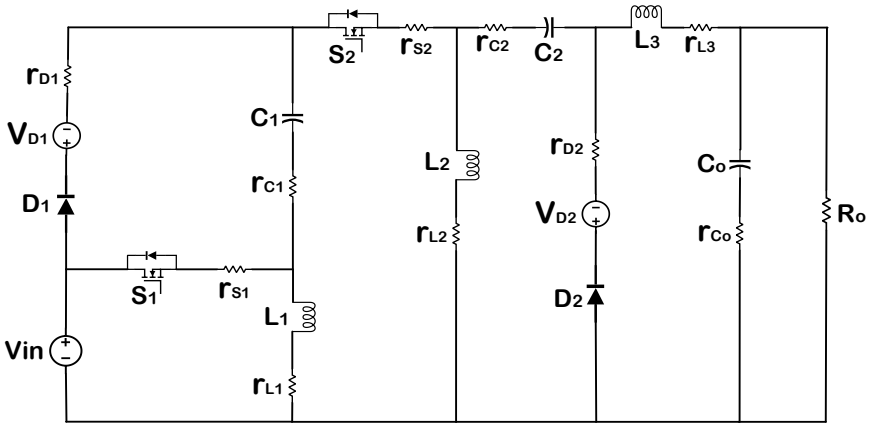


Fig. 4. Equivalent circuit of the proposed converter with parasitic elements.

5.1. Non-Ideal Voltage Gain

By applying the volt-second balance law across the inductors according to the operating principle of the proposed structure, the voltage relationships of v_{L1}, v_{L2}, and v_{L3} during time interval DT_S can be obtained as:

$$\begin{aligned} v_{L1} &= V_{in} - (r_{S1} + r_{L1}) i_{L1} - (i_{L2} + i_{L3}) r_{S1} \\ v_{L2} &= V_{in} + V_{C1} - r_{S1} i_{L1} - (r_{S1} + r_{S2} + r_{L2} - r_{C1}) i_{L2} - (r_{S1} + r_{S2} - r_{C1}) i_{L3} \\ v_{L3} &= V_{in} + V_{C1} + V_{C2} - V_o - r_{S1} i_{L1} - (r_{S1} + r_{S2} - r_{C1}) i_{L2} - (r_{S1} + r_{S2} + r_{L3} - r_{C1} - r_{C2}) i_{L3} \end{aligned} \tag{13}$$

Moreover, the voltage relationships of inductors during time interval *(1-D)* T_S can be written as:

$$\begin{aligned} v_{L1} &= V_{in} - V_{C1} - V_{D1} - (r_{D1} + r_{L1} + r_{C1}) i_{L1} \\ v_{L2} &= -V_{C2} - V_{D2} - (r_{D2} + r_{L2} + r_{C2}) i_{L2} - r_{D2} i_{L3} \\ v_{L3} &= -V_o - V_{D2} - r_{D2} i_{L2} - (r_{D2} + r_{L3}) i_{L3} \end{aligned} \tag{14}$$

Based on Eqs. (11), (13) and (14), the real voltage gain considering the non-idealities effect can be derived as:

$$M_{real}=\frac{\left(\frac{2D-D^2}{(1-D)^2}\right)-\left(\frac{D}{1-D}\right)\left(\frac{V_{D1}}{V_{in}}\right)-\left(\frac{V_{D2}}{V_{in}}\right)}{ar_{L1}+br_{L2}+r_{L3}+cr_{C1}+dr_{C2}+er_{S1}+fr_{S2}+gr_{D1}+hr_{D2}} \quad (15)$$

where the coefficients are explained as Eq. (16) in next sub-section.

The non-ideal and ideal voltage gain curves of the proposed converter are illustrated in Fig. 5. According to Fig. 5, the ideal voltage gain increases to limitless values by increasing the duty cycle from zero to one. Also, the maximum non-ideal voltage gain is attained at 13.64 at the 81 percent duty cycle. It is noticeable that the non-ideal and ideal voltage gain are approximately the same up to duty cycles, around 62 percent.

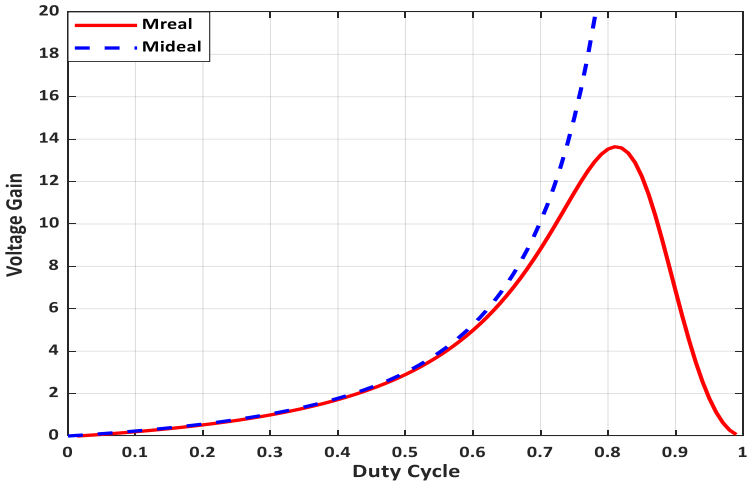


Fig. 5. Real and ideal voltage gain versus duty cycle.

5.2. Efficiency Calculation

The efficiency calculation based on the power loss of the proposed converter is analyzed in this part. The power losses include power losses of inductors, capacitors, power switches, and diodes.

$$\begin{cases} a=\dfrac{D^2}{(1-D)^4} \\ b=\dfrac{D^2}{(1-D)^2} \\ c=\dfrac{2D^2-D}{(1-D)^3} \\ d=\dfrac{2D^2-D}{1-D} \\ e=\dfrac{D}{(1-D)^4} \\ f=\dfrac{2D^2-D}{(1-D)^2} \\ g=\dfrac{D^2}{(1-D)^3} \\ h=\dfrac{1}{1-D} \end{cases} \quad (16)$$

Inductor loss: The winding resistance r_L leads to copper loss of the inductor, which can be calculated as:

$$P_{Loss}^{Inductor} = r_{L1}I_{L1,rms}^2 + r_{L2}I_{L2,rms}^2 + r_{L3}I_{L3,rms}^2 \quad (17)$$

where $I_{L1,rms}$, $I_{L2,rms}$, and $I_{L3,rms}$ are the RMS values of currents through inductors.

Capacitor loss: The parasitic resistance r_C leads to capacitor loss which can be calculated as:

$$P_{Loss}^{Capacitor} = r_{C1}I_{C1,rms}^2 + r_{C2}I_{C2,rms}^2 + r_{Co}I_{Co,rms}^2 \quad (18)$$

where $I_{C1,rms}$, $I_{C2,rms}$, and $I_{Co,rms}$ are the RMS values of currents through capacitors.

Power switch loss: The power switch loss includes the turned-on interval loss by ON resistance $R_{DS\text{-}on}$, named conduction loss, and the rise time t_r and fall time t_f duration loss, named switching loss as:

$$P_{Loss}^{Switch} = P_{Conduction}^{Switch} + P_{Switching}^{Switch} \quad (19)$$

These two losses can be explained as:

$$P_{Conduction}^{Switch} = R_{DS-on}I_{Switch,rms}^2, \quad P_{Switching}^{Switch} = \frac{1}{2}V_{DS-on}I_{Switch,avg}\left(t_r + t_f\right)f_s \quad (20)$$

where $I_{Switch,rms}$ denotes the RMS of current through the switch. Also, V_{DS_on} is the standing voltage on the switch, $I_{Switch,avg}$ is the average of current through the switch, and f_s is the frequency of the switch.

Diode loss: The series resistance r_D and forward voltage drop V_D lead to diode loss which can be derived as:

$$P_{Loss}^{Diode} = r_D I_{D,rms}^2 + V_D I_{D,avg} \quad (21)$$

where $I_{D,avg}$ and $I_{D,rms}$ are the average and RMS of current passing through the diode, respectively.

Thus, the efficiency can be derived as:

$$\eta = \frac{P_o}{P_o + P_{Loss}^{Total}} \times 100\% \quad (22)$$

where $P_{Loss}^{Total} = \sum\left(P_{Loss}^{Inductor} + P_{Loss}^{Capacitor} + P_{Loss}^{Switch} + P_{Loss}^{Diode}\right)$ and $P_o = V_o^2/R_o$.

The calculated efficiencies in boost and buck modes based on the power loss analysis mentioned above are shown in Fig. 6. As can be seen, the efficiency in boost mode is approximately around 96 percent. Also, the efficiency in buck mode changes by around 91 percent.

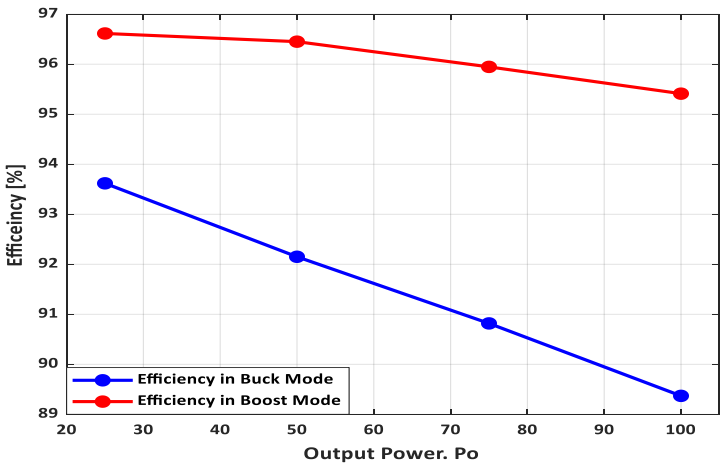


Fig. 6. Efficiency versus output power (Buck and Boost modes).

6. COMPARISON STUDY

The comparison of some main features such as the total number of elements, ideal voltage gain, voltage stresses of the switch and diodes, and the output polarity of the proposed converter against other converters such as quadratic buck-boost converters [22, 26], enhanced gain buck-boost converter [34], buck-boost converter based on ZETA structure [37], and inverted high step-down converter [38] are summarized in Table 1. The proposed converter and converters in [34, 37] have the same number of elements. Additionally, the converter in [26] has 20% more components than the proposed converter, whereas the converters in [22, 38] have one less inductor and capacitor.

Table 1. Comparison of the proposed converter with other similar converters.

	Ref [22]	Ref [26]	Ref [34]	Ref [37]	Ref [38]	Proposed converter
Switches	2	1	2	1	2	2
Diodes	2	5	2	2	2	2
Inductors	2	3	3	3	2	3
Capacitors	2	3	3	4	2	3
Total number of elements	8	12	10	10	8	10
Voltage gain (M)	$\left(\frac{D}{1-D}\right)^2$	$\left(\frac{D}{1-D}\right)^2$	$\left(\frac{D}{1-D}\right)^2$	$\frac{2D}{1-D}$	$\frac{D^2}{1-D}$	$\frac{2D-D^2}{(1-D)^2}$
Voltage stress on the switches	$\frac{V_{S1}}{V_{in}}=\frac{1}{(1-D)}$ $\frac{V_{S2}}{V_{in}}=\frac{D}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{V_{S1}}{V_{in}}=\frac{1}{(1-D)}$ $\frac{V_{S2}}{V_{in}}=\frac{1}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{D}{(1-D)}$	$\frac{V_{S1}}{V_{in}}=\frac{1}{(1-D)}$ $\frac{V_{S2}}{V_{in}}=\frac{1}{(1-D)^2}$
Voltage stress on the diodes	$\frac{V_{D1}}{V_{in}}=\frac{1}{(1-D)}$ $\frac{V_{D2}}{V_{in}}=\frac{D}{(1-D)^2}$	$\frac{V_{D1/D4}}{V_{in}}=\frac{1}{(1-D)}$ $\frac{V_{D2/D5}}{V_{in}}=\frac{D}{(1-D)^2}$ $\frac{V_{D3}}{V_{in}}=\frac{1}{(1-D)^2}$	$\frac{V_{D1}}{V_{in}}=\frac{1}{(1-D)}$ $\frac{V_{D2}}{V_{in}}=\frac{D}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{D}{(1-D)}$	$\frac{V_{D1}}{V_{in}}=\frac{1}{1-D}$ $\frac{V_{D2}}{V_{in}}=\frac{2-D}{(1-D)^2}$
Output polarity	Positive	Negative	Positive	Positive	Negative	Positive

Fig. 7 displays the ideal voltage gain comparison of the converters above versus the duty cycle. Compared to other converters, the proposed converter has a quick rise due to a high quadratic voltage gain. Also, it is noticeable that the proposed converter operates in buck mode for duty cycles less than 0.292.

The voltage stress across the power switches against the duty cycle is represented in Fig. 8. The voltage stress across the power switch S_1 is equal to switch S_1 of the converters [22, 34] and the switch of the converter [37]. Moreover, it tolerates lower voltage stress in comparison to switch S_2 of the converter [22] for duty cycles of more than 50%. Also, it has lower voltage stress than the other mentioned switches except for the switches of the converter [38] for duty cycles of less than 95%.

The voltage stress across the switch S_2 is the same as the voltage across the power switch of the converter [26] and the switch S_2 of the converter [34]. In comparison to the

other mentioned switches, it tolerates high voltage stress, which is acceptable according to achieving high voltage gain.

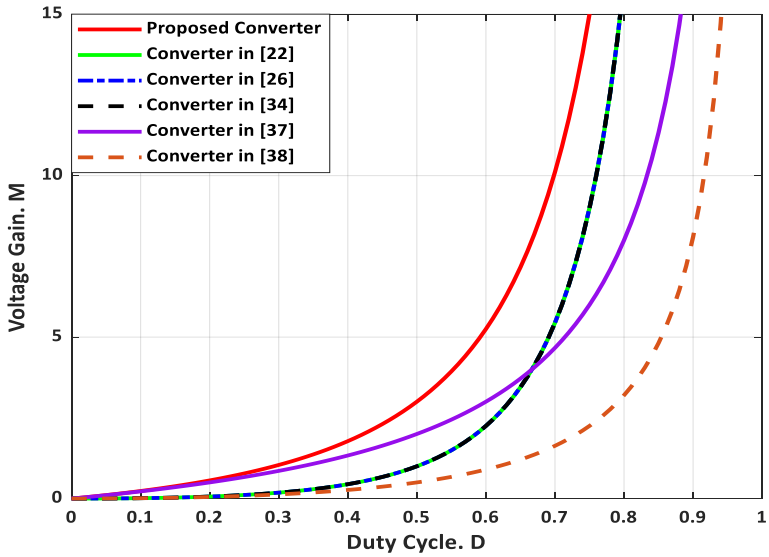


Fig. 7. Voltage gain versus duty cycle.

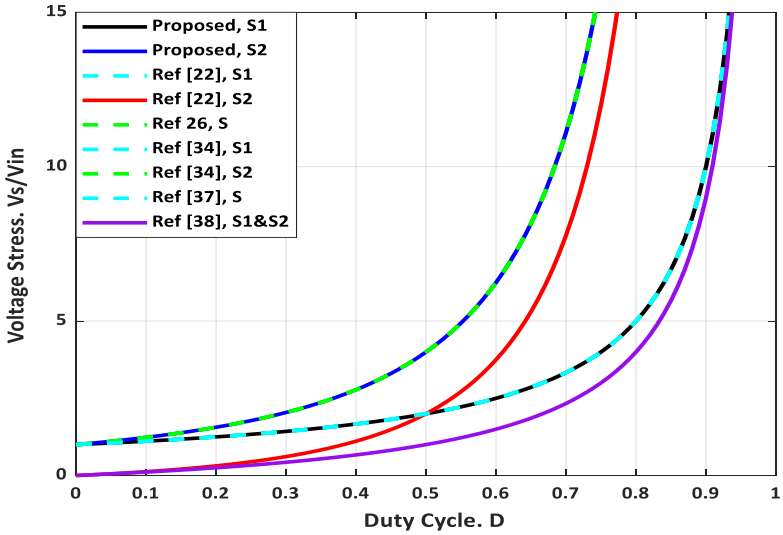


Fig. 8. Voltage stress of the switches versus duty cycle.

The voltage stress across the diodes against the duty cycle is represented in Fig. 9. The voltage stress across the diode D_1 is equal to diode D_1 of the converters [22, 34], diodes D_1 and D_4 of the converter [26], and diodes D_1 and D_2 of the converter [37]. Moreover, it has lower voltage stress in comparison to diode D_2 of the converters [22, 34] and diodes D_2 and D_5 of the converter [26] for duty cycles of more than 50%. Also, it can be observed that diode D_2 has high voltage stress than other suggested converters. As a result, the voltage stress across the power switch S_1 and the diode D_1 is less than half of the output voltage. Also, the voltage stress across switch S_2 equals the sum of the output and input voltages. Hence, just the diode D_2 tolerates high voltage stress than the output voltage.

The last main feature to compare the mentioned converters is the output polarity. As seen in Table. 1, the proposed converter and converters [22, 34, 37] have positive output polarity, which makes them superior to the two negative output polarity topologies.

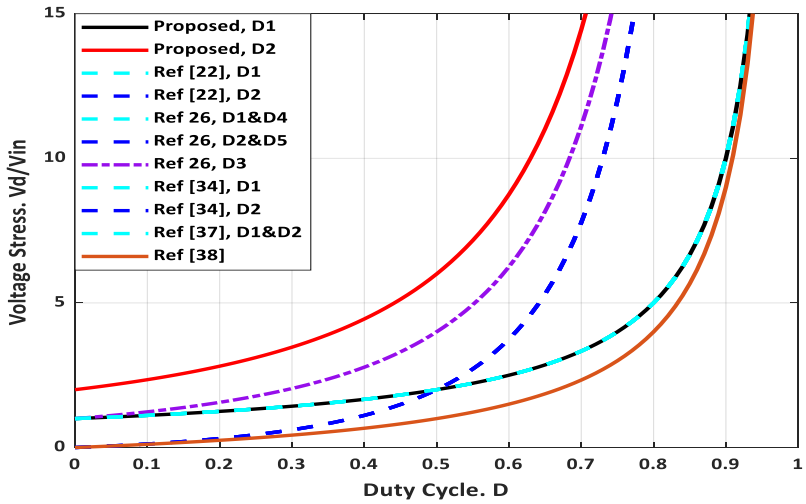


Fig. 9. Voltage stress of the diodes versus duty cycle.

7. SMALL SIGNAL MODEL OF THE PROPOSED CONVERTER

To obtain an open loop transfer function for dynamic behavior analysis and control design, the small signal model is utilized. Based on this model, each averaged parameter, such as the input voltage, the duty cycle, the currents through inductors, and the voltage across capacitors, comprise a DC value and an AC perturbation which can be written as:

$$\begin{cases} \langle v_{in} \rangle = V_{in} + \tilde{v}_{in} \\ \langle d \rangle = D + \tilde{d} \\ \langle i_{L1} \rangle = I_{L1} + \tilde{i}_{L1} \\ \langle i_{L2} \rangle = I_{L2} + \tilde{i}_{L2} \\ \langle i_{L3} \rangle = I_{L3} + \tilde{i}_{L3} \\ \langle v_{C1} \rangle = V_{C1} + \tilde{v}_{C1} \\ \langle v_{C2} \rangle = V_{C2} + \tilde{v}_{C2} \\ \langle v_{Co} \rangle = V_{C0} + \tilde{v}_{C0} \end{cases} \quad with \quad \begin{cases} |\tilde{v}_{in}| \ll |V_{in}| \\ |\tilde{d}| \ll |D| \\ |\tilde{i}_{L1}| \ll |I_{L1}| \\ |\tilde{i}_{L2}| \ll |I_{L2}| \\ |\tilde{i}_{L3}| \ll |I_{L3}| \\ |\tilde{v}_{C1}| \ll |V_{C1}| \\ |\tilde{v}_{C2}| \ll |V_{C2}| \\ |\tilde{v}_{Co}| \ll |V_{Co}| \end{cases} \tag{23}$$

By substituting Eq. (23) into Eqs. (1) and (2), and neglecting the second AC terms due to their small values, the small signal state equations can be obtained as:

$$\begin{cases} L_1 \dfrac{d\tilde{i}_{L1}}{dt} = \tilde{v}_{in} - (1-D)\tilde{v}_{C1} + \dfrac{V_{in}}{1-D}\tilde{d} \\ L_2 \dfrac{d\tilde{i}_{L2}}{dt} = D\tilde{v}_{in} + D\tilde{v}_{C1} - (1-D)\tilde{v}_{C2} + \dfrac{(2-D)V_{in}}{(1-D)^2}\tilde{d} \\ L_3 \dfrac{d\tilde{i}_{L3}}{dt} = D\tilde{v}_{in} + D\tilde{v}_{C1} + D\tilde{v}_{C2} - \tilde{v}_{Co} + \dfrac{(2-D)V_i}{(1-D)^2}\tilde{d} \\ C_1 \dfrac{d\tilde{v}_{C1}}{dt} = (1-D)\tilde{i}_{L1} - D\tilde{i}_{L2} - D\tilde{i}_{L3} - \dfrac{I_o}{(1-D)^2}\tilde{d} \\ C_2 \dfrac{d\tilde{v}_{C2}}{dt} = (1-D)\tilde{i}_{L2} - D\tilde{i}_{L3} - \dfrac{I_o}{1-D}\tilde{d} \\ C_o \dfrac{d\tilde{v}_{Co}}{dt} = \tilde{i}_{L3} - \left(\dfrac{1}{R_o}\right)\tilde{v}_{Co} \end{cases} \tag{24}$$

Hence, the state-space model derives as Eq. (25).

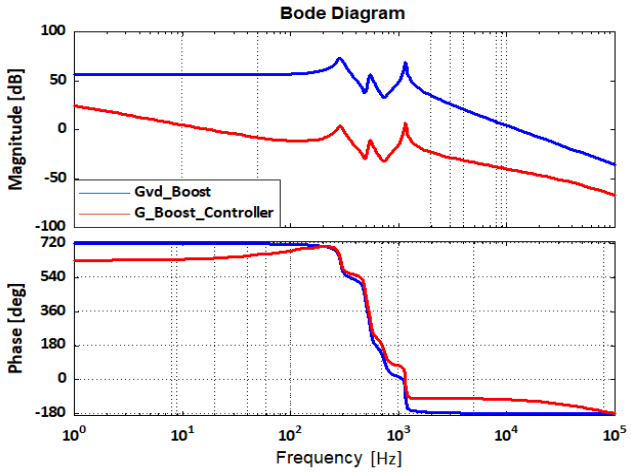
By applying Laplace transform on Eq. (24), the control-to-output transfer functions for boost and buck modes can be obtained as Eqs. (26) and (27), respectively. The bode diagrams based on the theoretical calculations without compensator and with compensator are illustrated in Fig. 10.

$$\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{i}_{L3}}{dt} \\ \frac{d\hat{v}_{C1}}{dt} \\ \frac{d\hat{v}_{C2}}{dt} \\ \frac{d\hat{v}_{Co}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\left(\frac{1-D}{L_1}\right) & 0 & 0 \\ 0 & 0 & 0 & \frac{D}{L_2} & -\left(\frac{1-D}{L_2}\right) & 0 \\ 0 & 0 & 0 & \frac{D}{L_3} & \frac{D}{L_3} & -\frac{1}{L_3} \\ \left(\frac{1-D}{C_1}\right) & -\frac{D}{C_1} & -\frac{D}{C_1} & 0 & 0 & 0 \\ 0 & \left(\frac{1-D}{C_2}\right) & -\frac{D}{C_2} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \\ \hat{v}_{Co} \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{L_1(1-D)} & \frac{1}{L_1} \\ \frac{V_{in}(2-D)}{L_2(1-D)^2} & \frac{D}{L_2} \\ \frac{V_{in}(2-D)}{L_3(1-D)^2} & \frac{D}{L_3} \\ -\frac{I_o}{C_1(1-D)^2} & 0 \\ -\frac{I_o}{C_2(1-D)} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{d} \\ \hat{v}_{in} \end{bmatrix} \quad (25)$$

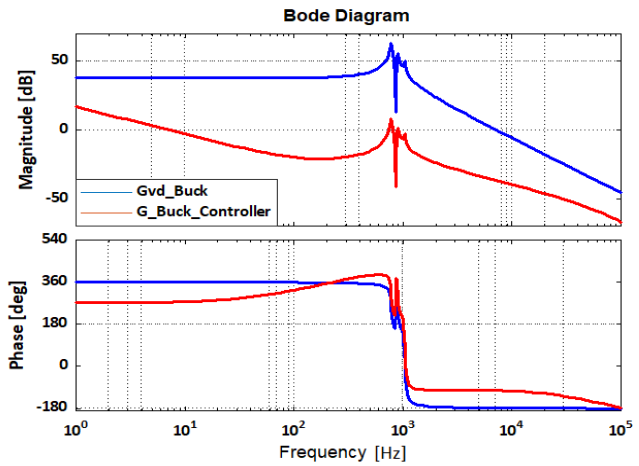
$$[\hat{v}_{Co}] = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1] \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \\ \hat{v}_{Co} \end{bmatrix} + [0] \begin{bmatrix} \hat{d} \\ \hat{v}_{in} \end{bmatrix}$$

$$G_{vd-Boost}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{6.316e9s^4 - 5.845e12s^3 + 1.949e17s^2 - 7.075e19s + 1.265e24}{s^6 + 600s^5 + 6.761e7s^4 + 2.7e10s^3 + 8.31e14s^2 + 1.657e17s + 2.029e21} \quad (26)$$

$$G_{vd-Buck}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{2.029e9s^4 - 1.024e12s^3 + 1.461e17s^2 - 2.954e19s + 2.53e24}{s^6 + 600s^5 + 9.844e7s^4 + 3.934e10s^3 + 3.134e15s^2 + 6.26e17s + 3.232e22} \quad (27)$$



(a)



(b)

Fig. 10. Bode diagrams of Gvd(s): a) boost mode; b) buck mode.

Fig. 10(a) represents the diagram for boost mode with *D=0.6* and the load *R=55.125Ω*. Also, Fig. 10(b) represents the diagram for buck mode with *D=0.2* and the load *R=5.06Ω*. It is evident from the bode plots of both boost and buck modes without compensator that the gain margin (GM) and phase margin (PM) are not in practical limitations. So, the proposed system became unstable. Utilizing SISOTOOL of MATLAB software and considering the practical limitations of gain margin (at least 5 dB) and phase margin (between 40 to 80 degrees), the proper controller can be obtained as:

$$G_C = \frac{K(s+a_1)(s+a_2)}{s(s+b_1)(s+b_2)} \tag{28}$$

By applying the controller, the GM and PM in boost mode are equal to 23.5 dB and 47.8°, respectively. Also, these margins are equal to 6.55 dB and 59.7° for buck mode. Thus, the proposed system became stable. Fig. 11 depicts the control system block diagram for the proposed converter, where the defined controller is responsible for ensuring the buck-boost voltage feature.

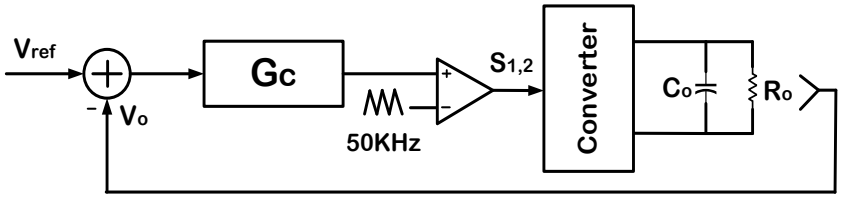


Fig. 11. Block diagram of the control system for the proposed converter.

8. SIMULATION RESULTS

The aforementioned features of the proposed quadratic buck-boost-based ZETA converter are verified by using a simulation prototype in the PSIM environment. Table 2 shows the simulation parameters of the prototype. As can be seen, the tested output power for boost and buck modes are 100W and 25W, respectively. Moreover, the power switches are controlled simultaneously in which their turn-on duty cycle is 60% for boost mode and 20% for buck mode. It is noticeable that the results are obtained in real condition by considering the parasitic elements. Thus, a little difference between theoretical and simulation results is acceptable.

Table 2. Simulation parameters in real condition

Parameters	Boost mode	Buck mode
Rated power (P_o)	200W	25W
Output voltage (V_o)	99.9V	10.8V
Input voltage (V_{in})	20V	
Switching frequency (f_s)	50kHz	
Duty cycle (D)	60%	20%
Inductor (L_1)	112µH	
Inductor (L_2)	842µH	
Inductor (L_3)	1.26mH	
Capacitor (C_1)	220 µF	
Capacitor (C_2)	22 µF	
Capacitor (C_o)	22 µF	

Figs. 12 and 13 indicate the outcomes for boost mode. The output and input voltages are shown in Fig. 12(a). As expected, the 20 V input voltage is boosted to 100 V by a 60% duty cycle. The voltage across capacitors C_1 and C_2 is represented in Fig. 12(b). The voltage of the capacitors is approximately 50 V and 100 V, in which the agreement between calculation and simulation results is visible. Fig. 12(c) depicts the continuous input current and output current. The average value of the output current is about 2 A. The current of inductors L_1, L_2, and L_3 are shown in Fig. 12(d), where the average currents of inductors are near 7.1 A, 2.8 A, and 2 A, respectively. The obtained results of average currents are the same as that derived from Eq. (11). The voltage across the power switches S_1 and S_2 are depicted in Fig. 13(a,b). As expected, the voltage stress across the power switch S_1 is less than half of the output voltage. Also, the voltage stress across switch S_2 equals the sum of the input and output voltages. Moreover, the voltage across the diodes D_1 and D_2 are depicted in Fig. 13(c,d), consistent with Eq. (8).

Figs. 14 and 15 indicate the outcomes for buck mode. The output and input voltages are shown in Fig. 14(a). The output voltage is equal to 10.3 V with a duty cycle of 20 %. This little difference originated from the presence of the resistance. The voltage across capacitors C_1 and C_2 are represented in Fig. 14(b), which are about 24.9 V and 10.2 V.

Fig. 14(c) represents the input current and output current. The average value of output current is equal to 2.5 A. Fig. 14(d) represents the current of inductors L_1, L_2, and L_3 equal to 0.78 A, 0.28 A, and 2.5 A, respectively. The voltage stress across the power switches S_1 and S_2 are depicted in Fig. 15(a,b), which overlap the relations obtained in Eq. (9). Finally, the voltage across the diodes D_1 and D_2 are shown in Fig. 15(c,d), equal to 25 V and 56 V, respectively. As can be seen, all the simulation results in both boost and buck modes are in good accordance with theoretical calculations. However, the little difference is ignorable due to the non-idealities effect.

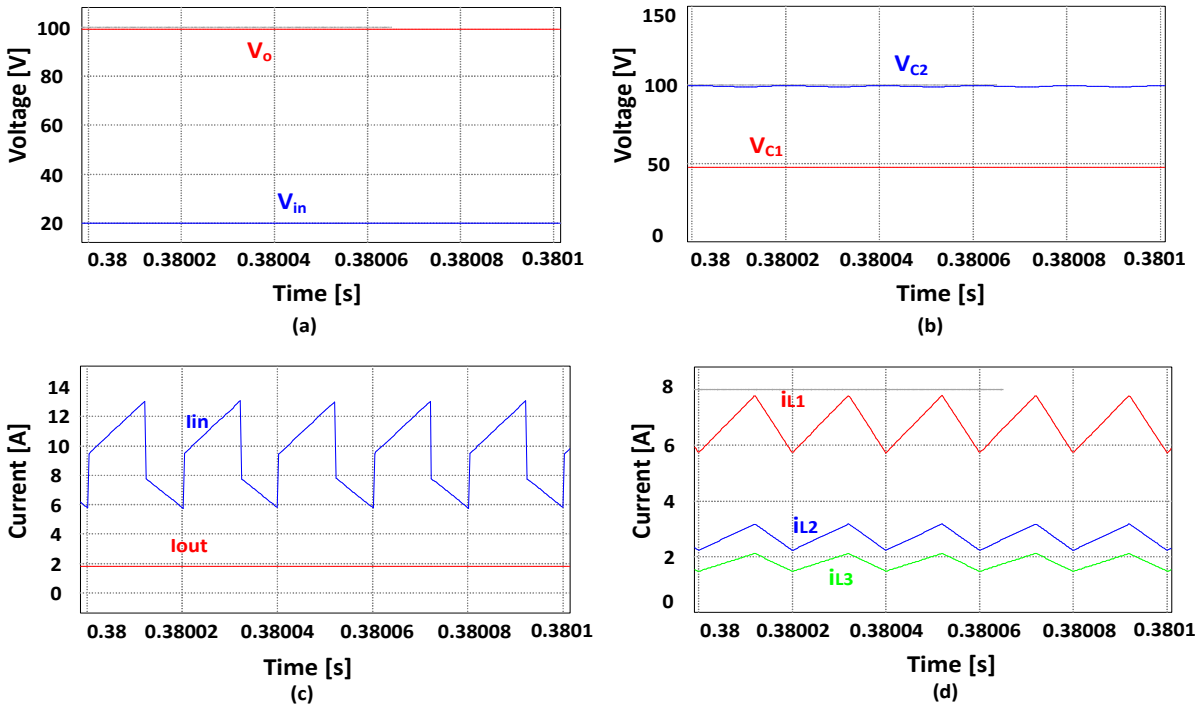


Fig. 12. Boost mode: a) output and input voltages (V_o, V_{in}); b) voltage across capacitors (V_{C1}, V_{C2}); c) output and input currents (I_o, I_{in}); d) inductor currents (i_{L1}, i_{L2}, i_{L3}).

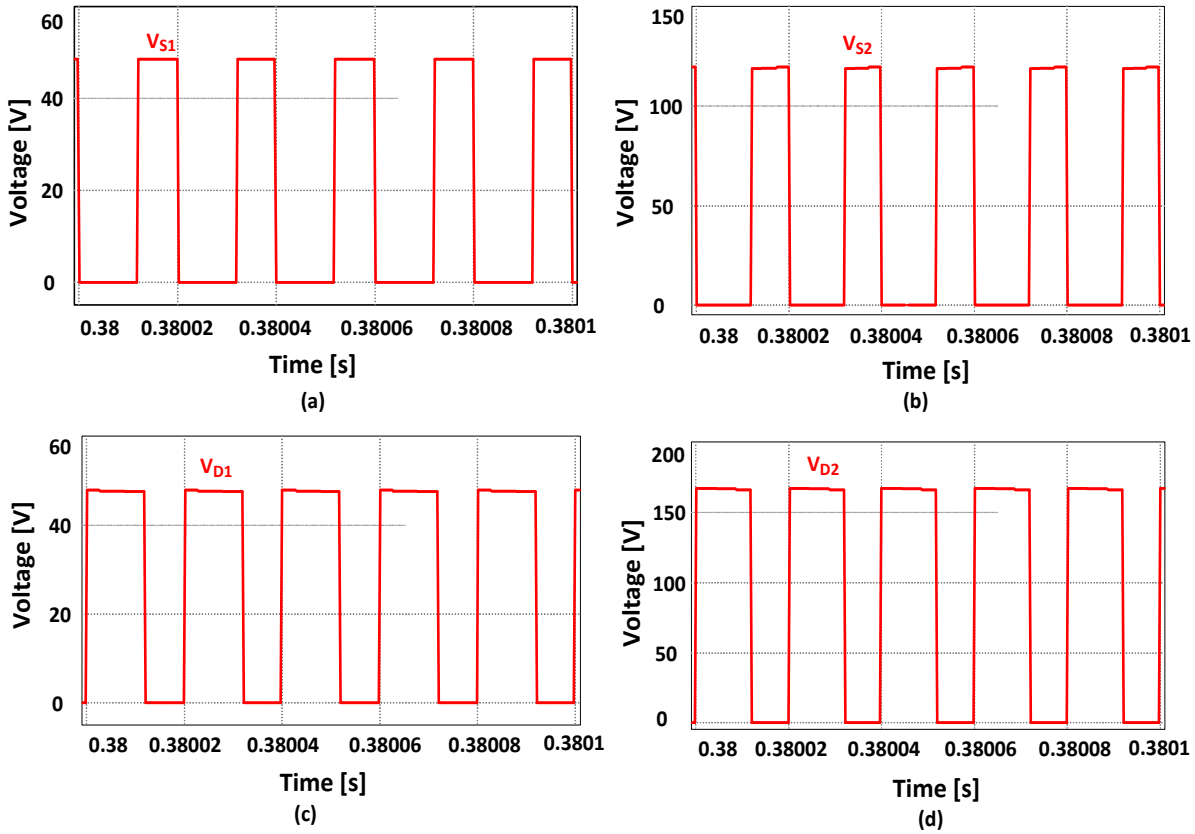


Fig. 13. Boost mode: a) voltage stress across the switch (V_{S1}); b) voltage stress across the switch (V_{S2}); c) voltage stress across the diode (V_{D1}); d) voltage stress across the diode (V_{D2}).

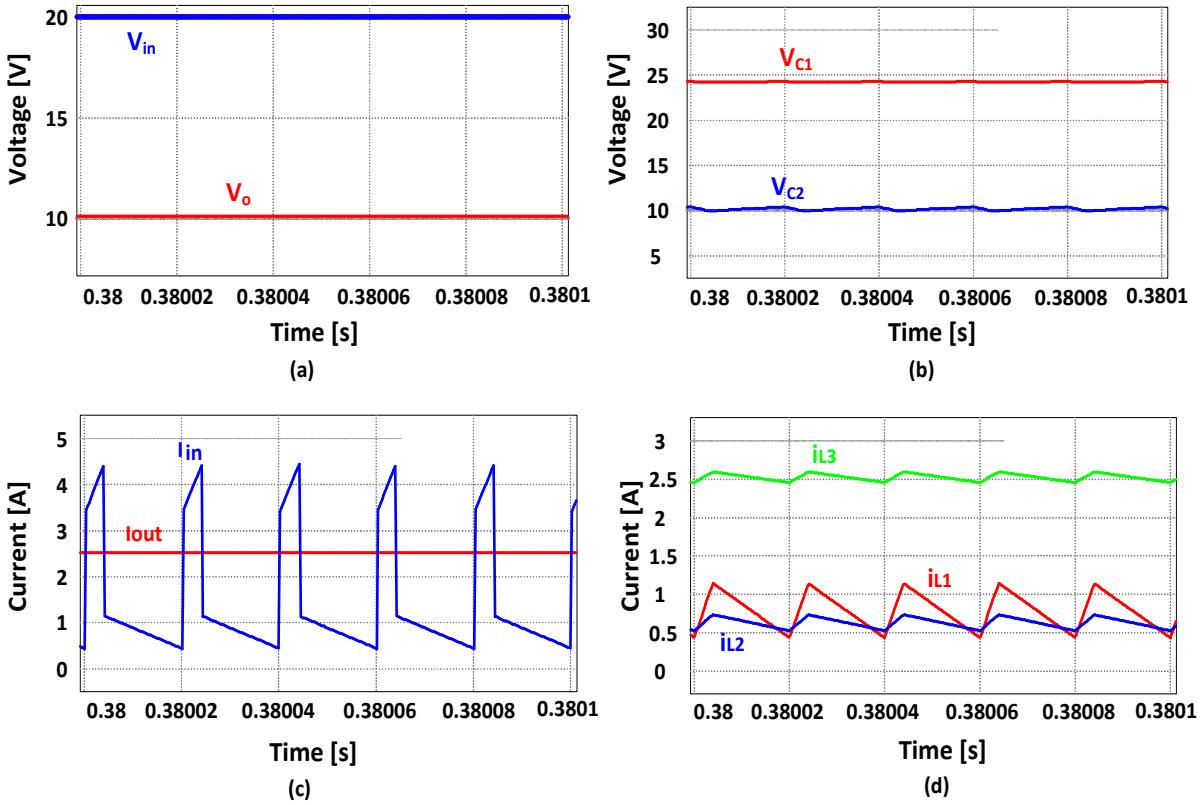


Fig. 14. Buck mode: a) output and input voltages (V_o, V_{in}); b) voltage across capacitors (V_{C1}, V_{C2}); c) output and input currents (I_o, I_{in}); d) inductor currents (i_{L1}, i_{L2}, i_{L3}).

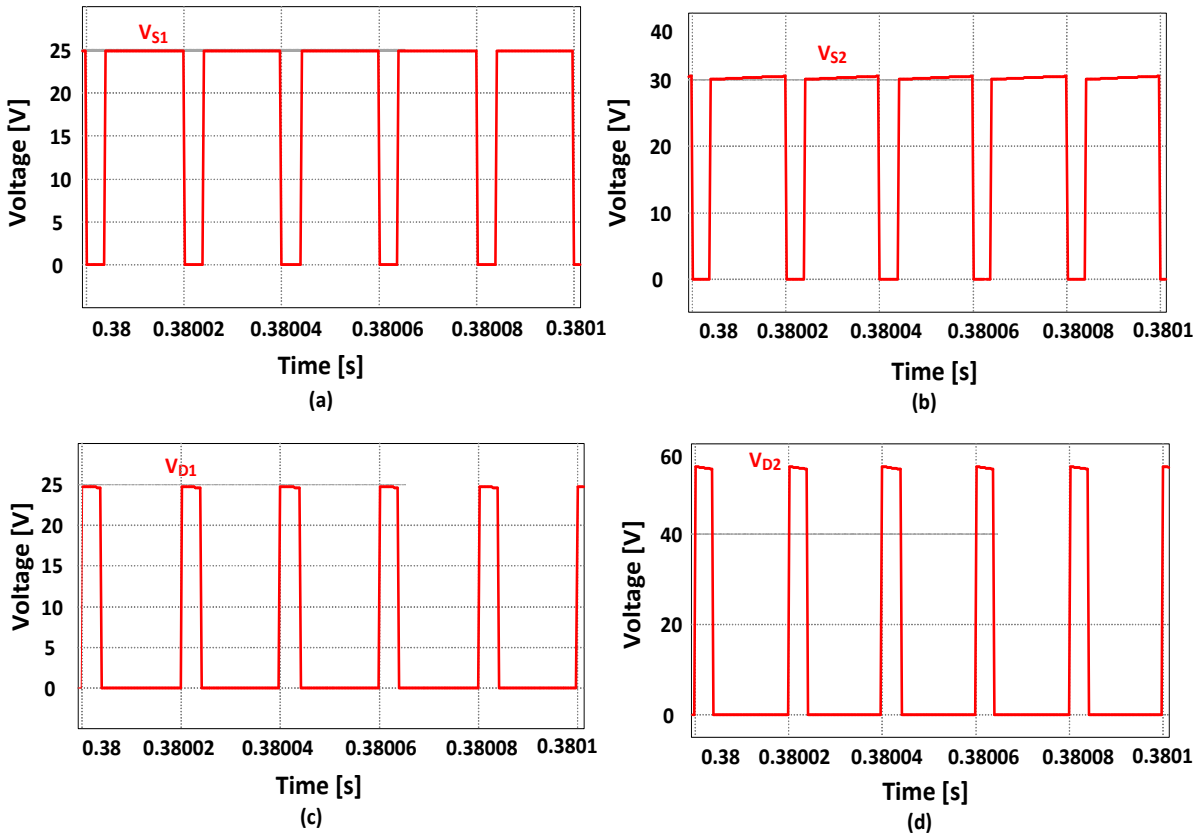


Fig. 15. Buck mode: a) voltage stress across the switch (V_{S1}); b) voltage stress across the switch (V_{S2}); c) voltage stress across the diode (V_{D1}); d) voltage stress across the diode (V_{D2}).

9. CONCLUSIONS

A new quadratic buck-boost converter based on the ZETA structure is proposed in this paper. The simplicity, continuous input current, common ground characteristics between the output/input voltage terminals and quadratic voltage gain are the main merits of the proposed structure. Moreover, the low or equal voltage stress across the power switches compared to the sum of the input and output voltages leads to the utilization of the low-rating elements besides the reduced cost, low conduction losses and improved efficiency. Also, the high quadratic voltage gain and positive output polarity features present the superiority of the proposed converter against other similar converters. Hence, this converter is a proper choice for utilization in renewable energy applications, such as fuel cells and PV cells due to its operation. Therefore, the analysis of the utilization of the proposed converter in renewable energies can be taken in future works. The steady-state analysis, parameter design, non-idealities effect on the real voltage gain and efficiency, comparison with other similar converters, and small signal model analysis are explained in detail. Finally, the correctness of the proposed converter is verified through PSIM simulation software.

REFERENCES

[1] S. Desingu, A. Mouttou, "Control of improved non-isolated high gain DC-DC converter," *Jordan Journal of Electrical Engineering*, vol. 7, no. 1, pp. 43-58, 2021.

[2] L. Schmitz, D. Martins, R. Coelho, "Comprehensive conception of high step-up DC–DC converters with coupled inductor and voltage multipliers techniques," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 67, no. 6, pp. 2140-2151, 2020.

[3] B. Zhu, Z. Wei, Y. Chen, H. Wang, D. Vilathgamuwa, "Multiple input-terminal voltage multiplier circuit," *IEEE Transactions on Industry Applications,* vol. 56, no. 5, pp. 5075-5082, 2020.

[4] N. Radaydeh, M. Al-Mothafar, "Extended research on small-signal modelling of current-mode controlled parallel-input/series-output buck-based converters," *Jordan Journal of Electrical Engineering,* vol. 5, no. 2, pp. 91-108, 2019.

[5] M. Bhaskar, M. Meraj, A. Iqbal, S. Padmanaban, P. Maroti, R. Alammari, "High gain transformer-less double-duty-triple-mode DC/DC converter for DC microgrid," *IEEE Access,* vol. 7, pp. 36353-36370, 2019.

[6] R. Li, F. Shi, "Control and optimization of residential photovoltaic power generation system with high efficiency isolated bidirectional DC–DC converter," *IEEE Access,* vol. 7, pp. 116107-116122, 2019.

[7] M. Ahmadi, M. Hosseinpour, S. Mousavi-Aghdam, F. Sedaghati, "A high conversion ratio transformerless buck-boost converter with continuous input current," *In 2021 12th Power Electronics, Drive Systems, and Technologies Conference,* pp. 1-7, 2021.

[8] K. Yari, S. Shahalami, H. Mojallali, "A novel nonisolated buck–boost converter with continuous input current and semiquadratic voltage gain," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 9, no. 5, pp. 6124-6138, 2021.

[9] A. Sarikhani, B. Allahverdinejad, M. Hamzeh, "A nonisolated buck–boost DC–DC converter with continuous input current for photovoltaic applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 9, no. 1, pp. 804-811, 2020.

[10] A. Dastgiri, M. Hosseinpour, F. Sedaghati, S. Mousavi-Aghdam, "A high step-up DC-DC converter with active switched LC-network and voltage-lift circuit," *In IEEE 2020 11th Power Electronics, Drive Systems, and Technologies Conference*, pp. 1-7, 2020.

[11] X. Fan, H. Sun, Z. Yuan, Z. Li, R. Shi, N. Ghadimi, "High voltage gain DC/DC converter using coupled inductor and VM techniques," *IEEE Access,* vol. 8, pp. 131975-131987, 2020.

[12] Q. Pan, H. Liu, P. Wheeler, F. Wu, "High step-up cascaded DC–DC converter integrating coupled inductor and passive snubber," *IET power electronics,* vol. 12, no. 9, pp. 2414-2423, 2019.

[13] A. Dastgiri, M. Hosseinpour, A. Poulad, "A high step-up non-isolated DC-DC converter with active switched-inductor and switched-capacitor networks," *International Journal of Modelling and Simulation,* pp. 1-12, 2022.

[14] H. Xie, R. Li, "A novel switched-capacitor converter with high voltage gain," *IEEE Access,* vol. 7, pp. 107831-107844, 2019.

[15] M. Salvador, J. De Andrade, T. Lazzarin, R. Coelho, "Nonisolated high-step-up DC–DC converter derived from switched-inductors and switched-capacitors," *IEEE Transactions on Industrial Electronics,* vol. 67, no. 10, pp. 8506-8516, 2019.

[16] A. Dastgiri, M. Hosseinpour, F. Sedaghati, S. Mousavi-Aghdam, "A high step-up DC–DC converter with active switched LC-network and voltage-lift circuit: topology, operating principle, and implementation," *International Journal of Circuit Theory and Applications,* vol. 50, no. 1, pp. 226-248, 2022.

[17] V. Bussa, R. Singh, R. Mahanty, V. Lal, "Design and analysis of step-up interleaved DC–DC converter for different duty regions," *IEEE Transactions on Industry Applications,* vol. 56, no. 2, pp. 2031-2047, 2020.

[18] S. Park, J. Yang, J. Rivas-Davila, "A hybrid Cockcroft–Walton/Dickson multiplier for high voltage generation," *IEEE Transactions on Power Electronics,* vol. 35, no. 3, pp. 2714-2723, 2019.

[19] J. Valdez-Resendiz, J. Rosas-Caro, J. Mayo-Maldonado, A. Llamas-Terres, "Quadratic boost converter based on stackable switching stages," *IET Power Electronics,* vol. 11, no. 8, pp. 1373-1381, 2018.

[20] B. Zhu, G. Liu, Y. Zhang, Y. Huang, S. Hu, "Single-switch high step-up zeta converter based on coat circuit," *IEEE Access,* vol. 9, pp. 5166-5176, 2020.

[21] S. Hasanpour, A. Mostaan, A. Baghramian, H. Mojallali, "Analysis, modeling, and implementation of a new transformerless semi-quadratic buck–boost DC/DC converter," *International Journal of Circuit Theory and Applications,* vol. 47, no. 6, pp. 862-883, 2019.

[22] J. Rosas-Caro, J. Valdez-Resendiz, J. Mayo-Maldonado, A. Alejo-Reyes, A. Valderrabano-Gonzalez, "Quadratic buck–boost converter with positive output voltage and minimum ripple point design," *IET Power Electronics,* vol. 11, no. 7, pp. 1306-1313, 2018.

[23] M. Veerachary, V. Khubchandani, "Analysis, design, and control of switching capacitor based buck–boost converter," *IEEE Transactions on Industry Applications,* vol. 55, no. 3, pp. 2845-2857, 2018.

[24] S. Gorji, A. Mostaan, H. Tran, M. Ektesabi, "Non-isolated buck–boost dc–dc converter with quadratic voltage gain ratio," *IET Power Electronics,* vol. 12, no. 6, pp. 1425-1433, 2019.

[25] H. Shayeghi, S. Pourjafar, F. Sedaghati, "Presented a transformer-less buck-boost DC–DC structure with vast voltage range," *IET Power Electronics,* vol. 15, no. 7, pp. 659-674, 2022.

[26] N. Zhang, G. Zhang, K. See, B. Zhang, "A single-switch quadratic buck–boost converter with continuous input port current and continuous output port current," *IEEE Transactions on Power Electronics,* vol. 33, no. 5, pp. 4157-4166, 2017.

[27] B. Zhu, S. Hu, G. Liu, Y. Huang, X. She, "Low-voltage stress buck-boost converter with a high-voltage conversion gain," *IEEE Access,* vol. 8, pp. 95188-95196, 2020.

[28] M. Banaei, S. Sani, "Analysis and implementation of a new SEPIC-based single-switch buck–boost DC–DC converter with continuous input current," *IEEE Transactions on Power Electronics,* vol. 33, no. 12, pp. 10317-10325, 2018.

[29] S. Gorji, A. Mostaan, H. Tran, M. Ektesabi, "Non-isolated buck–boost dc–dc converter with quadratic voltage gain ratio," *IET Power Electronics,* vol. 12, no. 6, pp. 1425-1433, 2019.

[30] P. García-Vite, J. Rosas-Caro, A. Martínez-Salazar, J. Chavez, A. Valderrábano-González, V. Sánchez-Huerta, "Quadratic buck–boost converter with reduced input current ripple and wide conversion range," *IET Power Electronics,* vol. 12, no. 15, pp. 3977-3986, 2019.

[31] M. Abbasi, E. Abbasi, B. Tousi, G. Gharehpetian, "New family of expandable step-up/-down DC-DC converters with increased voltage gain and decreased voltage stress on capacitors," *International Transactions on Electrical Energy Systems,* vol. 30, no. 3, pp. e12252, 2020.

[32] J. Rosas-Caro, V. Sanchez, J. Valdez-Resendiz, J. Mayo-Maldonado, F. Beltran-Carbajal, A. Valderrabano-Gonzalez, "Quadratic buck–boost converter with positive output voltage and continuous input current for PEMFC systems," *International Journal of Hydrogen Energy,* vol. 42, no. 51, pp. 30400-30406, 2017.

[33] J. Mayo-Maldonado, J. Valdez-Resendiz, P. Garcia-Vite, J. Rosas-Caro, M. Del Rosario Rivera-Espinosa, A. Valderrabano-Gonzalez, "Quadratic buck–boost converter with zero output voltage ripple at a selectable operating point," *IEEE Transactions on Industry Applications,* vol. 55, no. 3, pp. 2813-2822, 2018.

[34] M. Veerachary, M. Khuntia, "Design and analysis of two-switch-based enhanced gain buck–boost converters," *IEEE Transactions on Industrial Electronics,* vol. 69, no. 4, pp. 3577-3587, 2021.

[35] M. Okati, M. Eslami, M. Jafari Shahbazzadeh, H. Shareef, "A new transformerless quadratic buck–boost converter with high-voltage gain ratio and continuous input/output current port," *IET Power Electronics,* pp. 1280-1294, 2022.

[36] M. Hosseinpour, M. Ahmadi, A. Seifi, S. Mousavi-Aghdam, "A new transformerless semi-quadratic buck–boost converter based on combination of Cuk and traditional buck–boost converters," *International Journal of Circuit Theory and Applications,* pp. 3926-3948, 2022.

[37] M. Banaei, H. Bonab, "A high efficiency nonisolated buck–boost converter based on ZETA converter," *IEEE Transactions on Industrial Electronics,* vol. 67, no. 3, pp. 1991-1998, 2019.

[38] S. Naresh, S. Peddapati, "New family of transformer-less quadratic buck-boost converters with wide conversion ratio," *International Transactions on Electrical Energy Systems,* vol. 31, no. 11, pp. e13061, 2021.