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On Metastability Resilience of Multi-Gate MOSFETs

Ziyad A. Al-Tarawneh

Department of Electrical Engineering, Mu'tah University, Al-Karak, Jordan
e-mail: zdtarawneh@yahoo.com

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Abstract— With rapid technology scaling, Flip Flops have become more susceptible to metastability errors due to higher clock frequency and the well-known effects of process, temperature, and voltage fluctuations that can result in persistent setup and hold time violations. However, it is accepted that scaling cannot continue indefinitely; and approaches involving new materials and device structures have to be devised to circumvent the unavoidable barriers due to the reduction in device dimensions. A potential candidate to meet the criteria of low static power dissipation while maintaining high-speed operation is multiple gate MOSFETs (MuGFETs). This is due to its high current drive capability attained through its superior gate control over the channel and excellent suppression of short-channels. In this paper, the influence of key design parameters of multiple gate MOSFETs on the metastability robustness of Power PC Flip Flops is investigated. It was found that the resolution time constant (τ) can be reduced by increasing the effective width of the devices to enhance the device transconductance. For instance, this can be done by increasing the number of fins and fingers as well as fin widths of the devices. Furthermore, the impact of technology scaling on the metastability behavior of Flip Flops is considered. It is shown that using smaller technology nodes provides better metastability resilience.

Keywords— Metastability, MuGFETs, MTBF, reliability, resolution time constant.

I. INTRODUCTION

With continuous CMOS technology scaling, bistable circuits are becoming more vulnerable to metastability due to tighter timing budgets and the effects of process, temperature, and voltage variations that frequently contribute to setup and hold time violations which might result in metastable errors. However, it has been accepted that device scaling cannot continue indefinitely; and other approaches involving new materials and device structures are needed to avoid the inevitable barriers as a result of the reduction in device dimensions. In this regard, a possible candidate to meet the criteria of low static power dissipation while keeping high-speed and reliable operation is the multi-gate MOSFET (MuGFET) which results from its high drive current capability attained through its superior gate control over the channel and excellent suppressing of short-channel effects and better short-channel characteristics [1]. In general, metastability is a phenomenon that can take place in the event that the setup or hold time of a Flip Flop (FF) is violated. This can occur if there are either asynchronous signals within the design or multiple phase clocks which must be synchronised. Since phase clocks have no fixed phase relationship, no static timing analysis constraints can be created for data transfer between these clocks. Whenever the setup or hold relationship between the source and the destination register is violated, the output of the register might potentially become metastable, a condition where the output voltage is neither high nor low, but hovers at some transitional voltage for an indefinite period of time. Ultimately, the metastable value will resolve to a state of logic (0) or logic (1) [2], [3]. This situation is illustrated graphically in Fig. 1, which shows that the input signal of the Flip Flop changes during the window defined by t_{su} (FF setup time) and t_h (FF hold time) where no transitions should occur for typical behaviour. In this situation, the output value may become metastable and eventually resolve to its new logic value (FF Output (*a*)) or regress to its previous logic value (FF Output (*b*)). The resolution time occurs sometime after the technically specified t_{cq} (clock-transition to

Corresponding author's e-mail: zdtarawneh@yahoo.com

output delay) of the Flip Flop. If this additional time is not accounted for with additional timing slack, then system failures may occur [4].

While metastability has been present in digital VLSI systems for many years, the amount of research is considerably less prevalent when compared to other research areas. This is evident in the number of publications referring to metastability during the past fifty years or so. Previous works on metastability have primarily focused on theoretical modeling, experimental measurements and effects of several circuit parameters on a given latch or flip-flop. Works from two decades ago [5], [6], have shaped the basis for metastability analysis by solving small-signal equations for the time-resolving constant (τ) in the cross-coupled inverter pair. The work introduced in [2], [7] and [8] identifies the challenges and techniques associated with on-chip metastability measurement of a specific synchronizer, jamb-latch flip-flop. Several approaches have already been proposed in [9] to further improve metastability in the jamb-latch flip-flop under process variations as well as in sub-threshold operations. In [10], metastability parameters are extracted from simulation results in addition to delay and power analysis of different transmission-gate based flip-flops. Previously, metastability typically exists when flip-flops are synchronizing two unrelated signals in asynchronous systems.

As CMOS technology continues to scale, tighter timing budgets which arise from elevated clock rates and smaller intrinsic gate delays along with process, voltage and temperature (PVT) variations have all contributed to the escalating susceptibility of the flip-flops to enter metastability in the synchronous systems. Consequently, the number of research work relating to error-resilient design and metastability correction circuits has shown a gradual increase in the past few years [11], [12]. Generally, the potential to investigate metastability-related research topics is rapidly growing. With recent developments in processing technologies proposed in today's VLSI systems in order to accomplish different design objectives, a thorough analysis and design optimization on the flip-flop metastability based on the advanced process technologies have immensely remained missing.

This paper examines the impact of modern technology process parameters of MOSFETs on the metastability time-resolving constant (τ) of advanced technologies below the 65nm regime, in particular, multiple gate MOSFETs (MuGFETs). In sub- 100nm regime, MOSFETs with multi- gate structures are promising for high-performance and low-power CMOS applications owing to their superior gate control over the channel, excellent suppressing of short-channel effects and better short-channel characteristics [1].

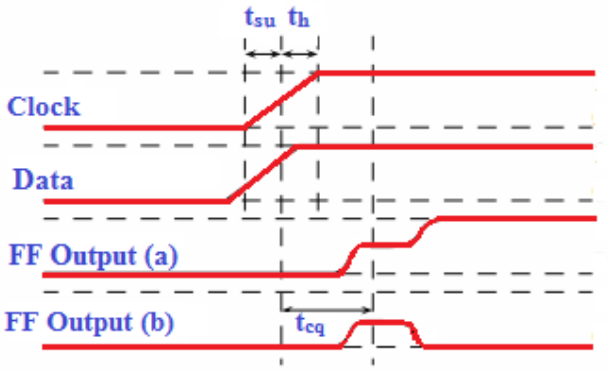

Fig. 1. Metastable flip flop behavior

In general, flip-flop is an imperative component to obtain high-performance and reliable deep-pipelined systems in modern digital microprocessors. Many different flip-flop

architectures have already been suggested during the past to effectively facilitate diverse design objectives such as performance, power, and area constraints. The foremost prominent design techniques involve transmission-gate based, tri-state inverter based, pulse-triggered, conditional capturing, and single-clocked phase. Transmission-gate flip-flops prove high-performance and low-power characteristics due to their low-impedance paths. Among them, the PowerPC shown in Fig. 2 is a conventional single-ended master-slave structure with short direct path and low-power consumption. The excellent overall performance of the PowerPC in comparison with various other transmission gate based flip-flops arises from the use of complementary pass-gates and low-power feedback. Nonetheless, the application of both CLK and CLK' signals increases the susceptibility to race through in the period of one gate delay in which the two phases overlap [10], [13]. In this paper, the influence of the key design parameters of multiple gate MOSFETs on the robustness of PowerPC Flip Flops towards metastability errors will be surveyed. It exhibits high-performance and low-power characteristics, especially when compared with other transmission gate based flip flops.

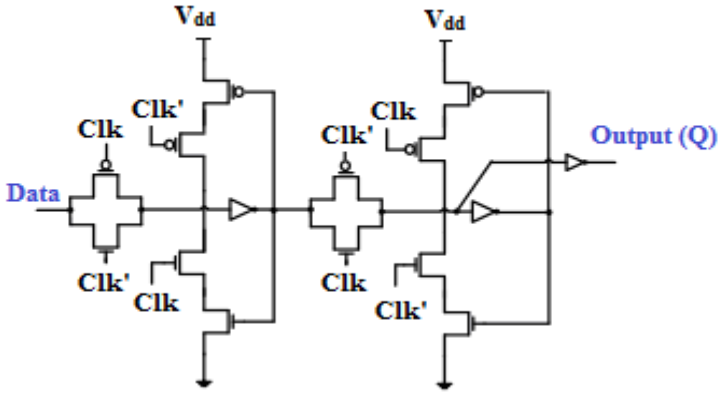

Fig. 2. Schematic view of a PowerPC flip-flop

II. CHARACTERIZATION OF METASTABILITY

Past research studies have demonstrated that the Flip Flop delay in the metastable region is exponential in nature, as shown in Fig. 3, where the delay behavior in the metastable region can be modeled and analyzed using two parameters (τ and T_0) [7]. In addition, the metastability window δ is a collective metric used to quantify metastability and is given in (1) [14]:

$$\delta = T_0 e^{-t_s/\tau} \tag{1}$$

where T_0 is the asymptotic width of the metastability window with no settling time, and (τ) is the resolution time constant that represents the inverse of the gain-bandwidth product of feedback inverters in the flip flop. Intuitively, it is possible to consider T_0 as the normalized time aperture when metastability can occur. Hence T_0 is closely related to the aperture window t_s. On the other hand, the resolution time constant (τ) determines how long the metastable state will last if the flip flop enters a metastable state. In general, metastability window (δ) can be defined as the time period where data transitions cannot be resolved within a given settling time (t_s), and as such, it should be kept as small as possible. Moreover, since δ

is exponentially proportional to τ, a slight improvement in τ can cause a sizeable reduction in δ. For this reason, a significant design effort is focused on minimizing the value of τ.

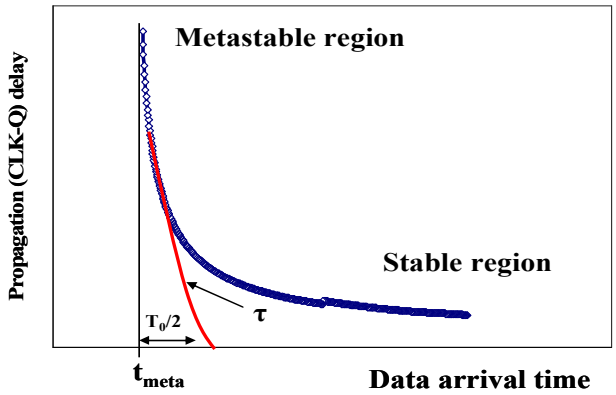

Fig. 3. Ideal plot of the C-Q delay vs. data arrival time for a typical flip flop

To obtain τ and T_0 for metastability analysis, HSPICE simulations were undertaken. The propagation (CLK-Q) delay vs. displacement between the input data and the clock signal is firstly plotted for the Flip Flop under investigation. The data arrival time varied at a time interval of 0.01ps to generate the corresponding propagation delay in order to obtain precise results in the metastable region. Thereafter, from the plot, the metastable point t_{meta} at which the flip flop fails to capture the correct data is determined. The next step is to obtain a theoretical linear curve from the propagation (CLK-Q) delay vs. the time displacement between the input data; and t_{meta} plot on a semi log scale. The slope of this line is the time resolving constant τ and the X-intercept is $\log(T_0/2)$ as shown in Fig. 4 [10], [15]-[17]. To make a conservative analysis of metastability, the largest slope value and the corresponding X intercept in the linear curve were taken when extracting τ and T_0 [2], [17].

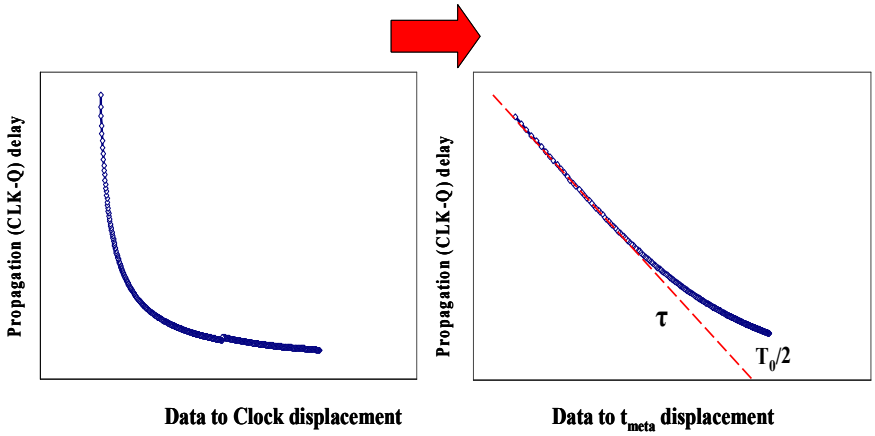

Fig. 4. Illustration for extracting metastability parameters [17]

III. RESULTS AND DISCUSSION

In this section, the effects of key device and circuit parameters such as process and voltage on the resolution time constant (τ) of the PowerPC flip flop are illustrated using results obtained from Spice simulations for different technology nodes ranging from 10 to 20nm. The simulations were performed using BPTM model cards [18] with nominal operating voltage V_{dd}=0.9V. To obtain precise results in the metastable region under a variety of operating

conditions, the data arrival time varied at a time interval of 0.01ps in order to generate the corresponding propagation delay of the FF under investigation.

In this work, we focus on the analysis of τ exclusively as it has the greatest impact on the metastability window δ and the Mean Time Between Failure (MTBF), which represents the average time between the failures of a system as shown in (2) [19]-[21].

$$MTBF = \frac{1}{f_D f_{clk} \; T_0 e^{-t_s/\tau}} \tag{2}$$

where f_D and f_{CLK} are the data transition frequency and clock frequency, respectively. In general, the MTBF indicates the average time interval between two successive failures in a system. Hence, a higher MTBF value increases the overall reliability of the system.

Fig. 5 illustrates the influence supply voltage V_{dd} on the circuit robustness to metastability. Clearly, as the supply voltage V_{dd} of the circuit increases, the time resolving constant τ decreases, leading to a substantial improvement in the circuit's robustness to the metastability phenomenon. Moreover, it can be concluded from Fig. 3 that using smaller device geometries can ensure significant changes in the resilience of the circuit to metastability. This might be explained by the fact that the current strength of the devices noticeably increases as the device size is reduced; and hence the total transconductance increases. In addition, the reduction incurred in node capacitance, as a consequence of device scaling, results in a significant reduction in the likelihood of the metastability state.

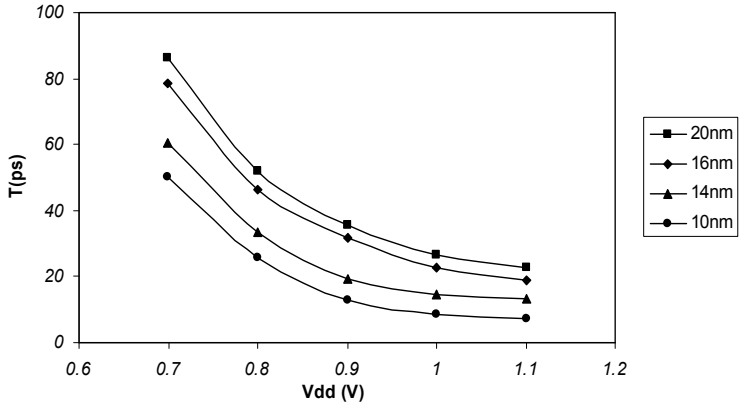

Fig. 5. The impact of power supply voltage on resolution time constant for different technology nodes

Fig. 6 demonstrates the influence of temperature upon the time resolving constant. It can be seen that as the temperature of the circuit increases, the time resolving constant τ increases, leading to a degradation in the circuit robustness to the metastability phenomenon. This is mainly because of the fact that the electron and hole mobilities tend to be degraded as the temperature increases, and are directly reflected on the drive current of the devices. Hence, the decrease of total transconductance can elevate the probability of metastability errors.

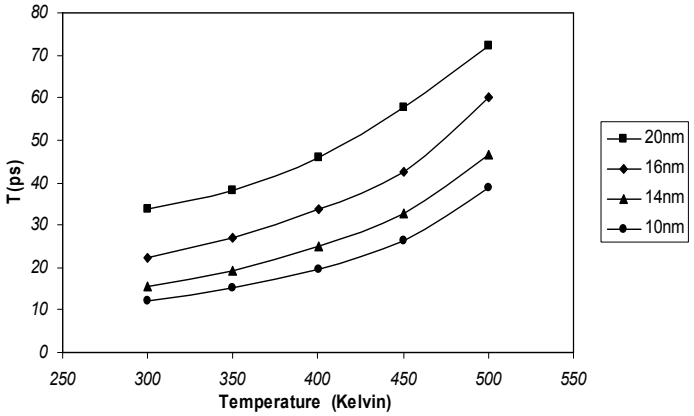

Fig. 6. The impact of temperature variations on resolution time constant for different technology nodes

Fig. 7 shows that as the number of fins of the transistor increases, the time resolving constant τ reduces, leading to an improvement in the circuit's robustness to a metastable event. This might be explained by the fact that increasing these device parameters will significantly increase the total effective width of the devices. Similar effects can possibly be noticed from Fig. 8 and 9, when the number of fingers and the fin width of the devices increase. Additionally, it can be noticed from Fig. 7-9 that using smaller device geometries can promote significant changes in the resilience of the circuit to the metastability phenomenon.

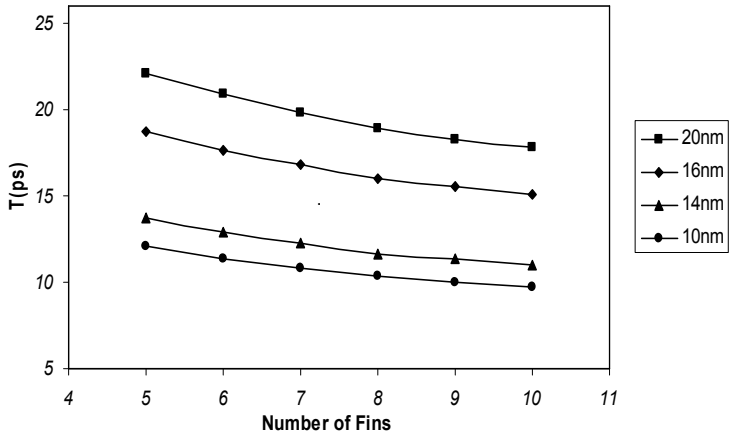

Fig. 7. The impact of the number of fins on the circuit resolution time constant for different technology nodes

Fig. 10 and 11 demonstrate that as the height and thickness of the device fin increase, the time resolving constant τ increases. This might be explained by the fact that increasing these device parameters will significantly increase the total effective width of the devices. As a result, the total node capacitance increases and leads to an increase in the resolving time constant.

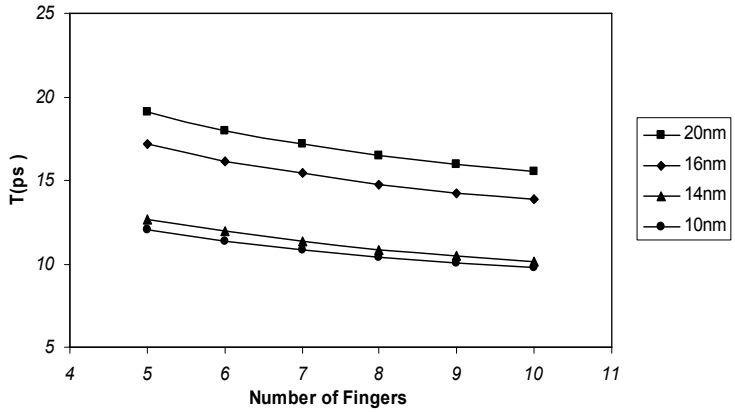

Fig. 8. The impact of the number of device fingers on the resolution time constant for different technology nodes

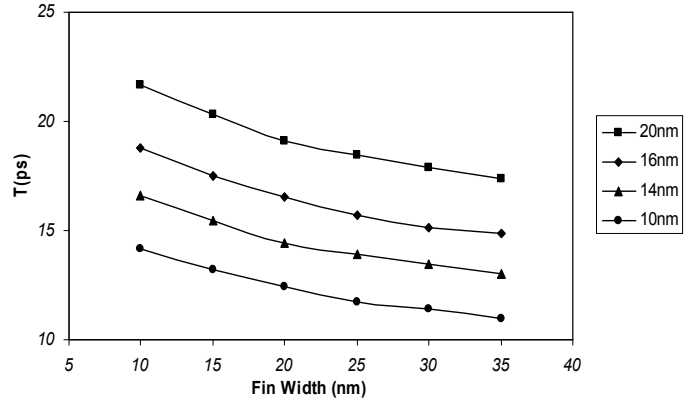

Fig. 9. The impact of fin width on the circuit resolution time constant for different technology nodes

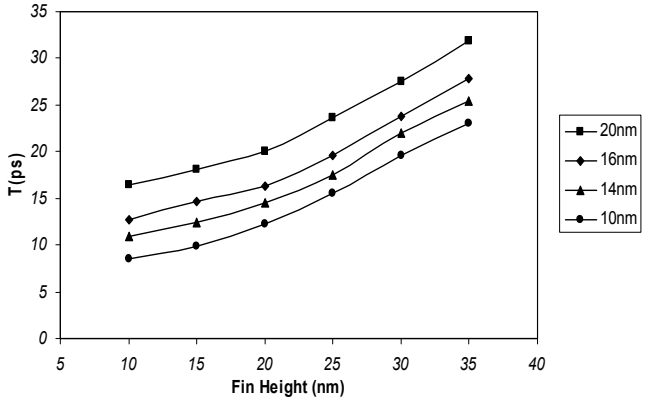

Fig. 10. The impact of fin height on resolution time constant for different technology nodes

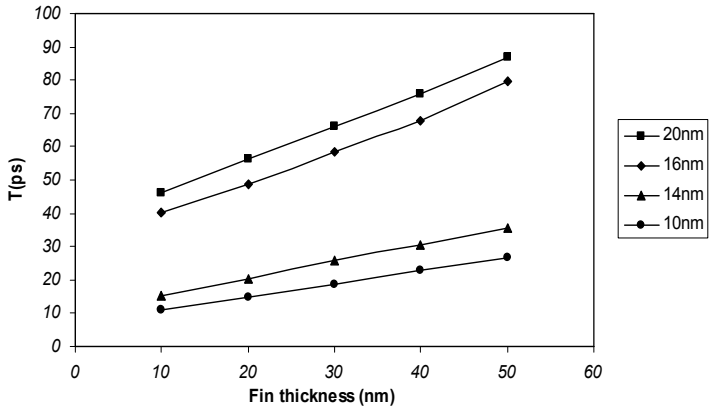

Fig. 11. The impact of the number of device fingers on the resolution time constant for different technology nodes

From the above results it can be seen that using a higher power supply voltage increases the robustness of the circuit to metastability. Moreover, increasing the number of fins and fingers of the MG devices will increase the effective width of the transistors and the effective width of the devise, and greatly improve the robustness of the FF to metastability errors. This can be explained by generally expressing the resolution time constant of a flip flop as in (3) [22]:

$$\tau_i \propto \frac{C_Q}{g_m} \tag{3}$$

where C_Q includes the gate and diffusion capacitances of the metastable flip flop nodes; the coupling capacitance between the gate and the source and drain of the transistors connected to the metastable nodes. g_m is the transconductance of the transistors in the FF near metastability, in which the transistors operate in the linear region. Hence, the transconductance can be approximated by:

$$g_m = k\frac{W}{L}(V_{gs} - V_{th}) \tag{4}$$

Based on (3), increasing the transconductance of devices may decrease the resolution time for a metastable event and thus increase the MTBF value.

In particular, it is possible to improve the robustness of a circuit to metastable events by firstly reducing the total node capacitance. This can be done by firstly using different Flip Flop circuit topologies; and secondly by increasing the driving strength of the devices in order to enhance the total transconductance of the circuit especially for the feedback inverters in the FF. Moreover, both solutions will enhance the circuit performance in terms of delay and dynamic power consumption.

Furthermore, as shown in Fig. 12, the metastability resilience PowerPC flip flop can be strengthened by increasing the core diameter of the all-around gate transistors. This might be explained by the increase of the cylinder diameter which will effectively increase the effective device width; improve the device current strength, and help reduce the likelihood of metastability events in a circuit. It can also be noticed that using smaller gate lengths provides lower time resolving constants.

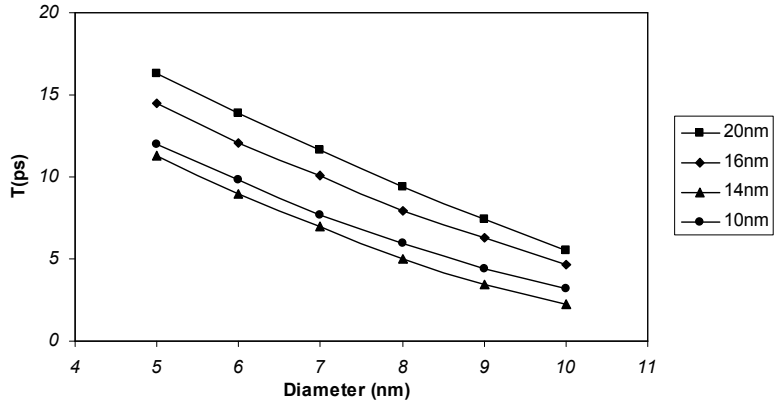

Fig. 12. The effect of the diameter of all-around gate transistors on the circuit resolution time constant for different technology nodes

IV. CONCLUSION

The influence of key design parameters of a MuGFET technology on metastability robustness of a Power PC Flip Flop has been investigated. It was found that the resolution time constant can be reduced by increasing the effective width of the devices to enhance the device transconductance with minimum effect on total capacitance. For instance, this can be done by increasing the number of fins, number of fingers and fin width of the devices. Furthermore, the impact of technology scaling on the metastability behaviour of flip flops was considered. It was shown that using smaller technology nodes provides better metastability resilience. Additionally, a higher improvement in circuit resilience to metastability error can possibly be gained by devices when using larger core diameter and higher voltage power supply. Finally, it was found that increasing the thickness and height of the device fins has a degrading effect on the FF resilience to metastability errors.

The simulation results presented in this paper should prove useful to designers who need to implement metastable immune systems. Future work may include further evaluation and optimization of different Flip Flop architectures based on new materials and device structures.

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